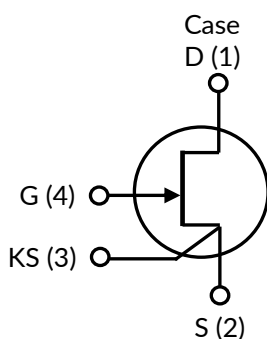


DATASHEET

UJ4N075005K4S

CASE



750V-4.8mΩ SiC Normally-on JFET

Rev. B, June 2024

Description

Qorvo's UJ4N075005K4S is a 750 V, 4.8mΩ high-performance Gen 4 normally-on SiC JFET transistor. This device exhibits ultra-low on resistance ($R_{DS(on)}$) in a TO-247-4L package, making it an ideal fit to address the challenging thermal constraints of solid-state circuit breakers and relay applications. Additionally, the JFET is a robust device technology capable of the high-energy switching required in circuit protection applications.

Features

- ◆ Single digit on-resistance
- ◆ Operating temperature: 175°C (max)
- ◆ High pulse current capability
- ◆ Excellent device robustness
- ◆ Silver-sintered die attach for excellent thermal resistance
- ◆ Short circuit rated
- ◆ RoHS compliant

Typical applications

- ◆ Solid State / Semiconductor Circuit Breaker
- ◆ Solid State / Semiconductor Relay
- ◆ Battery Disconnects
- ◆ Surge Protection
- ◆ Inrush Current Control
- ◆ Induction heating

Part Number	Package	Marking
UJ4N075005K4S	TO-247-4L	UJ4N075005K4S



Maximum Ratings

Parameter	Symbol	Test Conditions	Value	Units
Drain-source voltage	V_{DS}		750	V
Gate-source voltage	V_{GS}	DC	-30 to +3	V
		AC ¹	-30 to +30	V
Continuous drain current ²	I_D	$T_C < 127^\circ\text{C}$	120	A
Pulsed drain current ³	I_{DM}	$T_C = 25^\circ\text{C}$	588	A
Short circuit withstand time	t_{SC}	$V_{DS} = 400\text{V}$, $T_{J(\text{START})} = 175^\circ\text{C}$	5	μs
Power dissipation	P_{tot}	$T_C = 25^\circ\text{C}$	714	W
Maximum junction temperature	$T_{J,max}$		175	$^\circ\text{C}$
Operating and storage temperature	T_J, T_{STG}		-55 to 175	$^\circ\text{C}$
Max. lead temperature for soldering, 1/8" from case for 5 seconds	T_L		250	$^\circ\text{C}$

1. +30V AC rating applies for turn-on pulses <200ns applied with external $R_G > 1\Omega$.

2. Limited by bondwires

3. Pulse width t_p limited by $T_{J,max}$

Thermal Characteristics

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Thermal resistance, junction-to-case	$R_{\theta JC}$			0.16	0.21	$^\circ\text{C/W}$

Electrical Characteristics ($T_J = +25^\circ\text{C}$ unless otherwise specified)

Typical Performance - Static

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Drain-source breakdown voltage	BV_{DS}	$V_{GS} = -20\text{V}$, $I_D = 2\text{mA}$	750			V
Total drain leakage current	I_{DSS}	$V_{DS} = 750\text{V}$, $V_{GS} = -20\text{V}$, $T_J = 25^\circ\text{C}$		13	120	μA
		$V_{DS} = 750\text{V}$, $V_{GS} = -20\text{V}$, $T_J = 175^\circ\text{C}$		65		
Total gate leakage current	I_{GSS}	$V_{GS} = -20\text{V}$, $T_J = 25^\circ\text{C}$		0.1	100	μA
		$V_{GS} = -20\text{V}$, $T_J = 175^\circ\text{C}$		0.3		μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 2\text{V}$, $I_D = 80\text{A}$, $T_J = 25^\circ\text{C}$		4.8		$\text{m}\Omega$
		$V_{GS} = 0\text{V}$, $I_D = 80\text{A}$, $T_J = 25^\circ\text{C}$		5.4	6.6	
		$V_{GS} = 2\text{V}$, $I_D = 80\text{A}$, $T_J = 175^\circ\text{C}$		10.4		
		$V_{GS} = 0\text{V}$, $I_D = 80\text{A}$, $T_J = 175^\circ\text{C}$		11.9		
Gate threshold voltage	$V_{G(th)}$	$V_{DS} = 5\text{V}$, $I_D = 180\text{mA}$	-8.3	-6.0	-3.7	V
Gate resistance	R_G	$f = 1\text{MHz}$, open drain		0.8		Ω

Typical Performance - Dynamic

Parameter	Symbol	Test Conditions	Value			Units
			Min	Typ	Max	
Input capacitance	C_{iss}	$V_{DS} = 400\text{V}$, $V_{GS} = -20\text{V}$ $f = 100\text{kHz}$		3028		pF
Output capacitance	C_{oss}			364		
Reverse transfer capacitance	C_{rss}			360		
Effective output capacitance, energy related	$C_{oss(er)}$	$V_{DS} = 0\text{V}$ to 400V , $V_{GS} = -20\text{V}$		448		pF
C_{OSS} stored energy	E_{oss}	$V_{DS} = 400\text{V}$, $V_{GS} = -20\text{V}$		36		μJ
Total gate charge	Q_G	$V_{DS} = 400\text{V}$, $I_D = 80\text{A}$, $V_{GS} = -18\text{V}$ to 0V		400		nC
Gate-drain charge	Q_{GD}			270		
Gate-source charge	Q_{GS}			60		

Typical Performance Diagrams

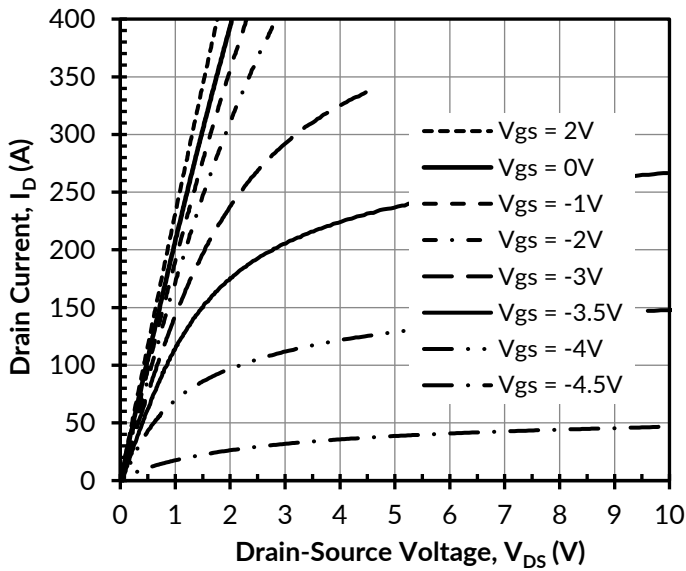


Figure 1. Typical output characteristics at $T_j = -55^\circ\text{C}$, $t_p < 250\mu\text{s}$

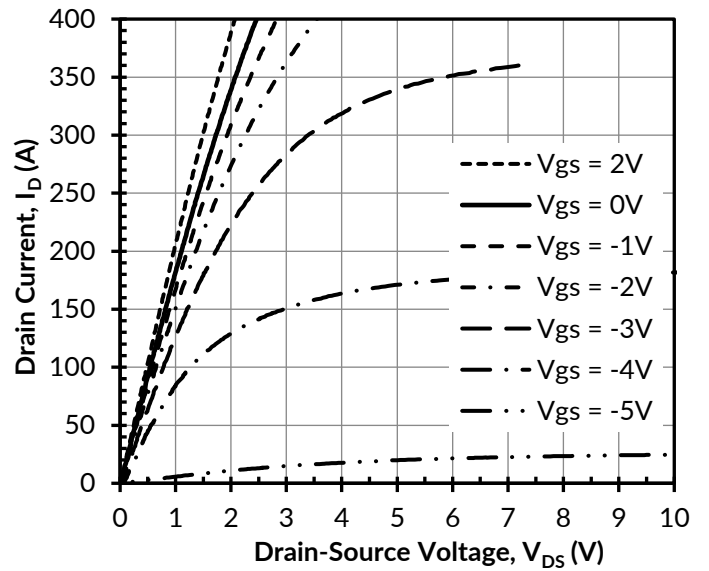


Figure 2. Typical output characteristics at $T_j = 25^\circ\text{C}$, $t_p < 250\mu\text{s}$

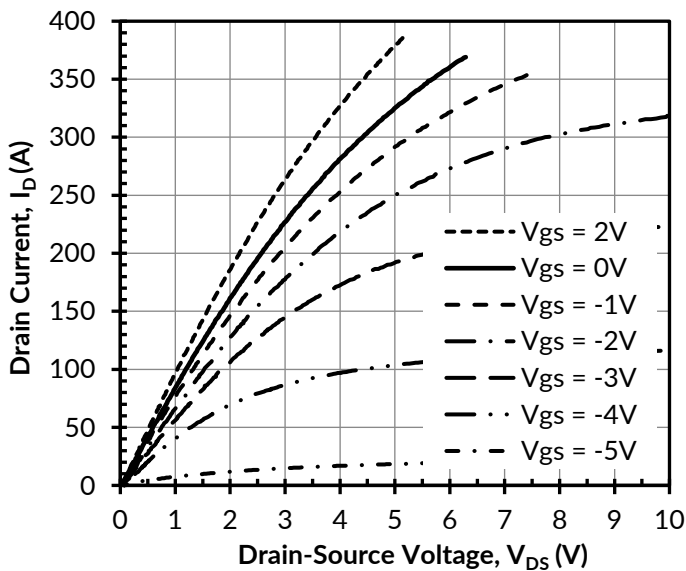


Figure 3. Typical output characteristics at $T_j = 175^\circ\text{C}$, $t_p < 250\mu\text{s}$

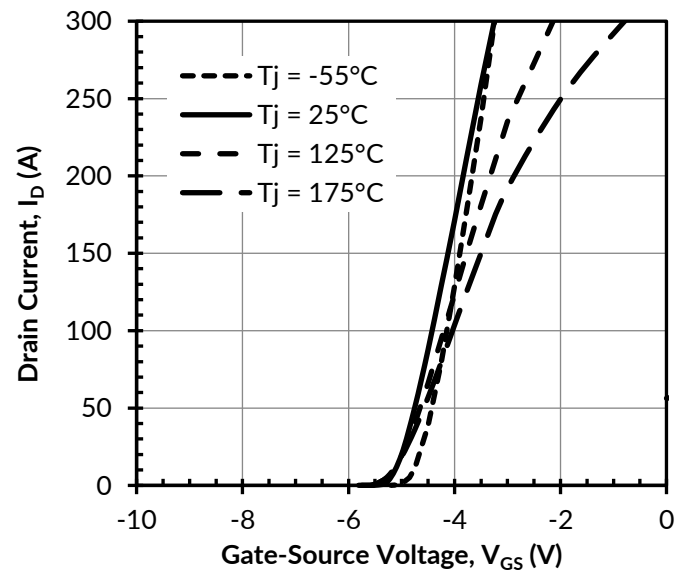


Figure 4. Typical transfer characteristics at $V_{DS} = 5\text{V}$

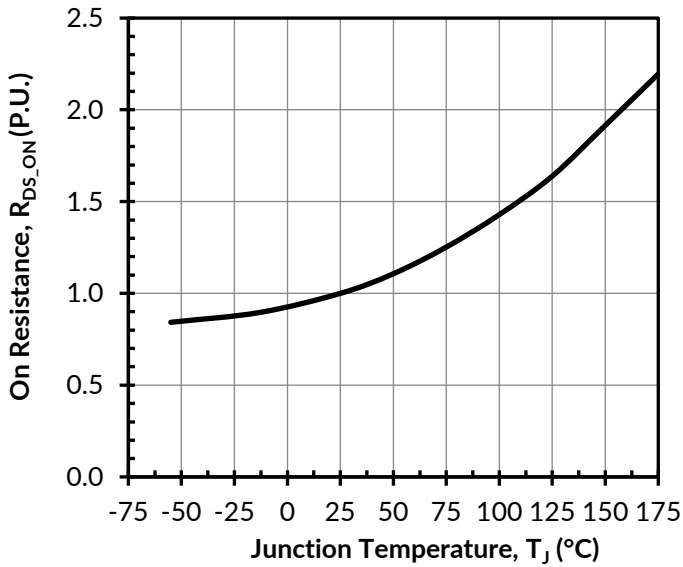


Figure 5. Normalized on-resistance vs. temperature at $V_{GS} = 0V$ and $I_D = 80A$

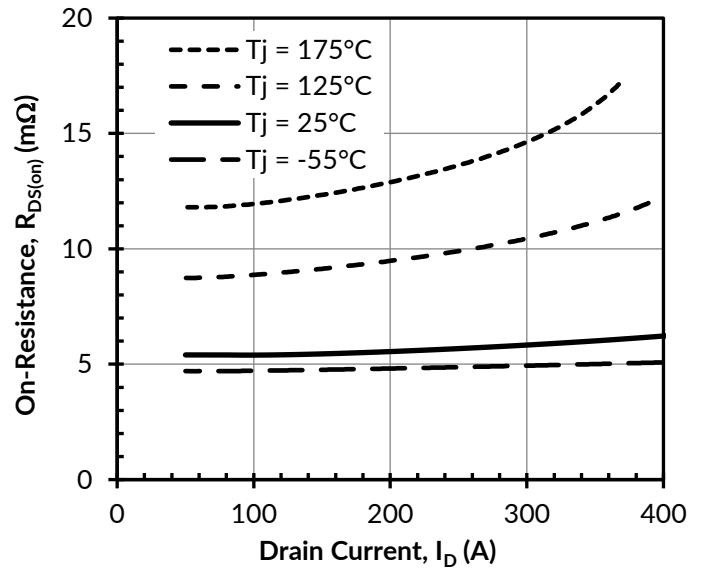


Figure 6. Typical drain-source on-resistances at $V_{GS} = 0V$

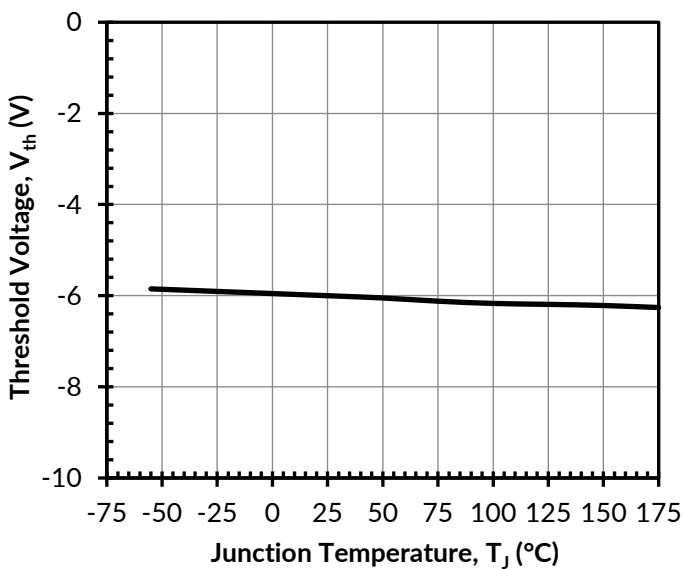


Figure 7. Threshold voltage vs. junction temperature at $V_{DS} = 5V$ and $I_D = 180mA$

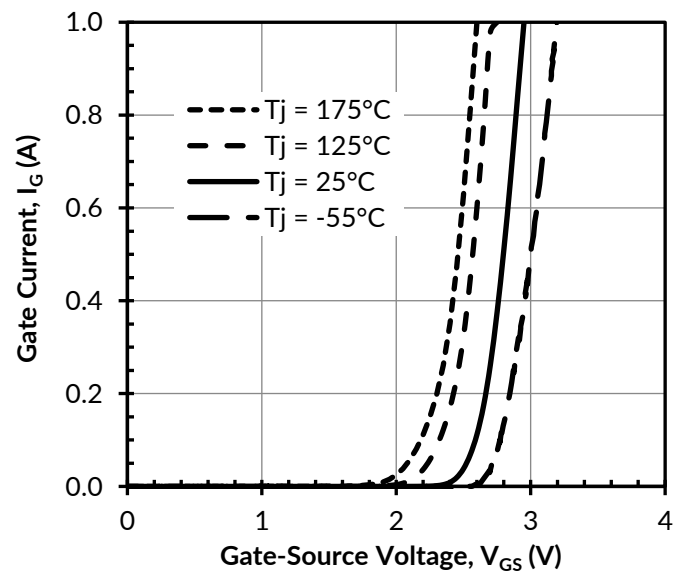


Figure 8. Typical gate forward current at $V_{DS} = 0V$

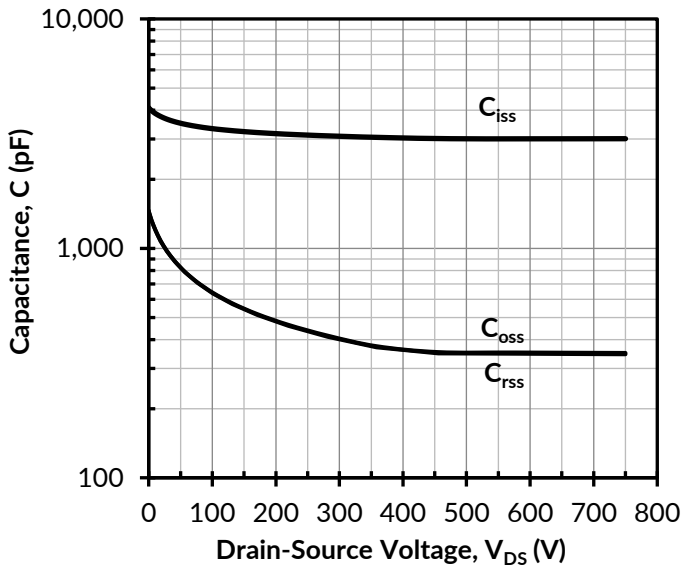


Figure 9. Typical capacitances at $f = 100\text{kHz}$ and $V_{GS} = -20\text{V}$

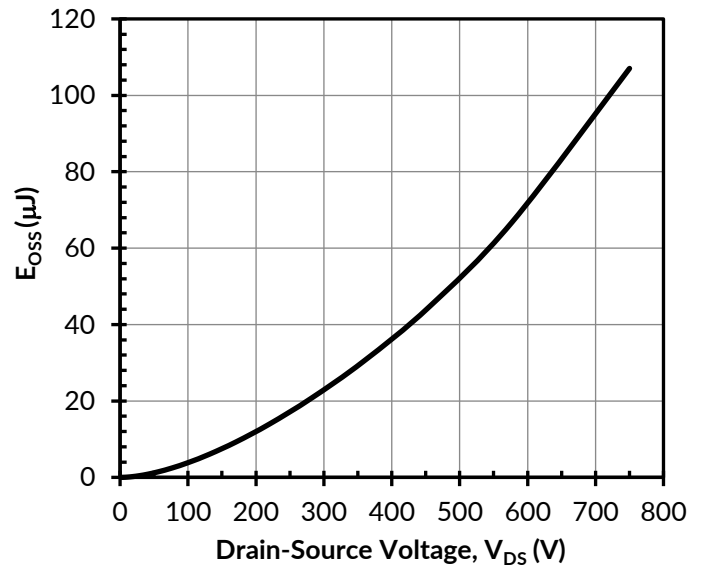


Figure 10. Typical stored energy in C_{OSS} at $V_{GS} = -20\text{V}$

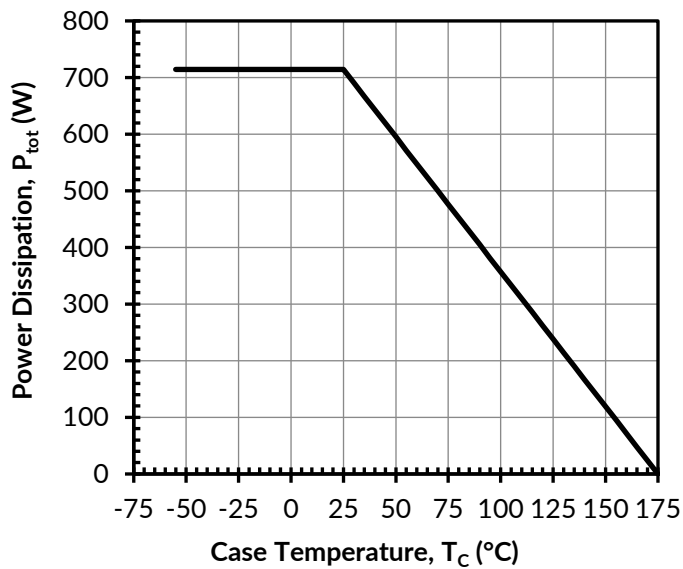


Figure 11. Total power Dissipation

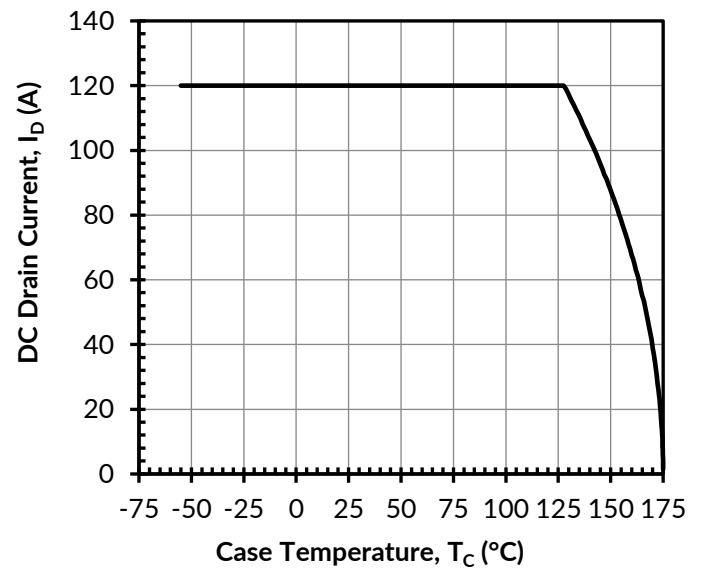


Figure 12. DC drain current derating

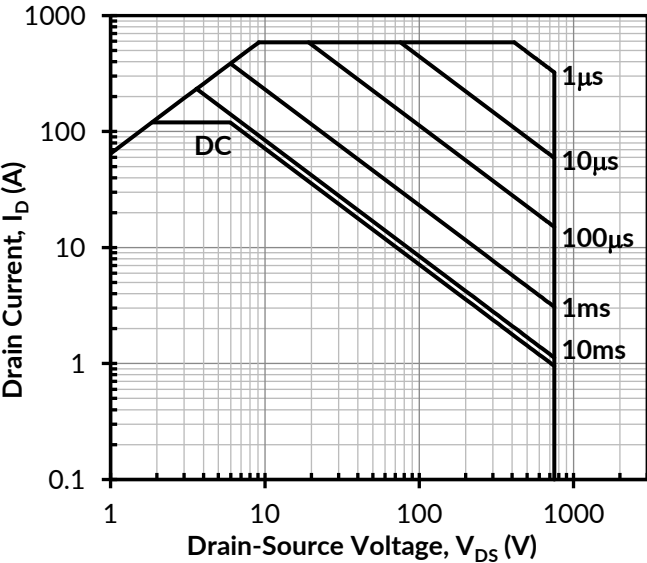


Figure 13. Safe operation area at $T_C = 25^\circ\text{C}$, Parameter t_p

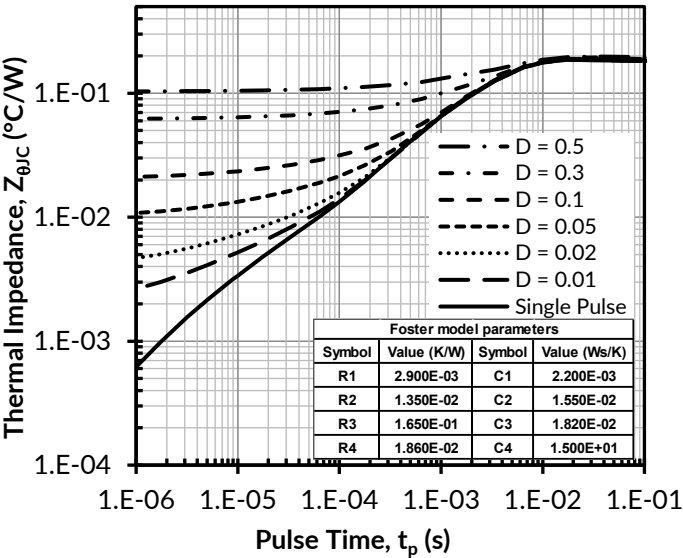


Figure 14. Maximum transient thermal impedance

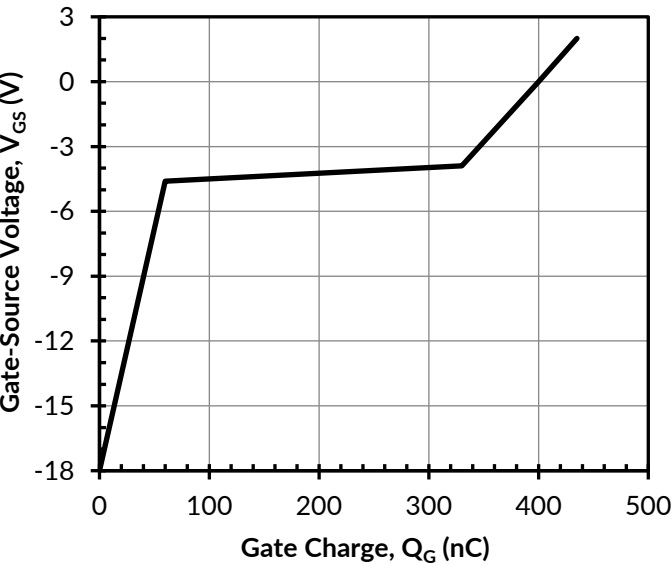


Figure 15. Typical gate charge at $V_{DS} = 400\text{V}$ and $I_D = 80\text{A}$

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