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April 2014

SSU1N50B

520V N-Channel MOSFET

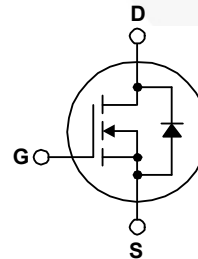
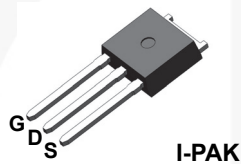
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, power factor correction and electronic lamp ballasts based on half bridge.

Features

- 1.3A, 520V, $R_{DS(on)} = 5.3\Omega$ @ $V_{GS} = 10V$
- Low Gate Charge (Typ. 8.3 nC)
- Low C_{rss} (Typ. 5.5 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability



Absolute Maximum Ratings

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	SSU1N50BTU	Unit
V_{DSS}	Drain-Source Voltage	520	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	1.3	A
	- Continuous ($T_C = 100^\circ\text{C}$)	0.82	A
I_{DM}	Drain Current - Pulsed (Note 1)	5.0	A
V_{GSS}	Gate-Source Voltage	± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	100	mJ
I_{AR}	Avalanche Current (Note 1)	1.3	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	2.6	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	2.5	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	26	W
	- Derate above 25°C	0.21	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	SSU1N50BTU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	4.76	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (*1 in ² Pad of 2-oz Copper), Max	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Minimum Pad of 2-oz Copper), Max.	110	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
SSU1N50BTU	SSU1N50B	I-PAK	Tube	N/A	N/A	70 units

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	520	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.54	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.65\text{ A}$	--	4.1	5.3	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 0.65\text{ A}$	--	1.65	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	260	340	pF
C_{oss}	Output Capacitance		--	25	33	pF
C_{rss}	Reverse Transfer Capacitance		--	5.5	7.2	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 1.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	14	40	ns
t_r	Turn-On Rise Time		--	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time		--	35	80	ns
Q_g	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 1.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	--	8.3	11	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge		--	3.4	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	1.3	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	5.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 1.3 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 1.5 A, dI _F / dt = 100 A/μs	--	230	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.94	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 106\text{ mH}, I_{AS} = 1.5\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 1.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.

Typical Characteristics

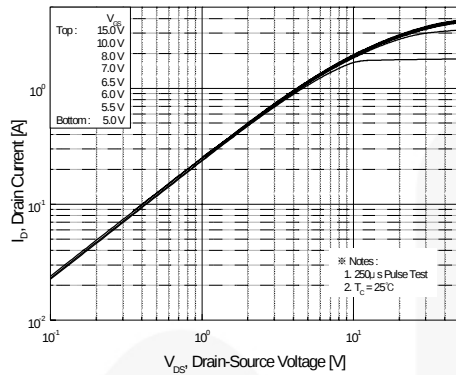


Figure 1. On-Region Characteristics

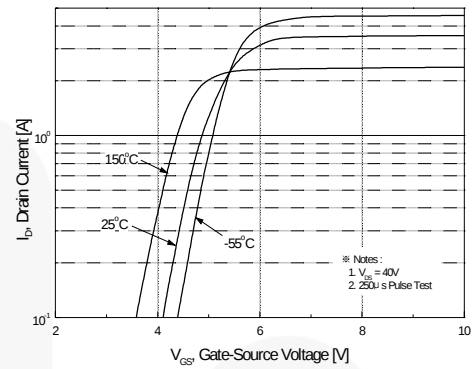


Figure 2. Transfer Characteristics

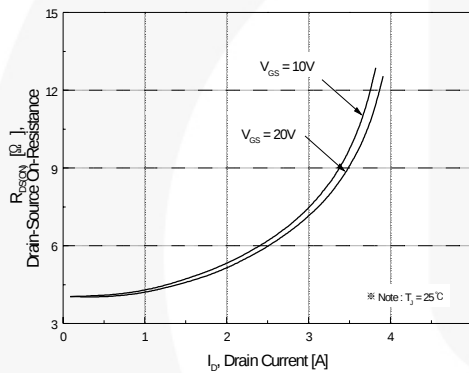


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

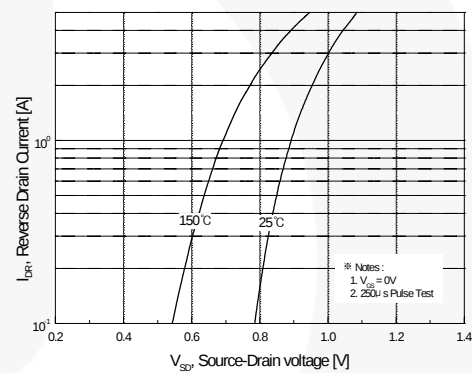


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

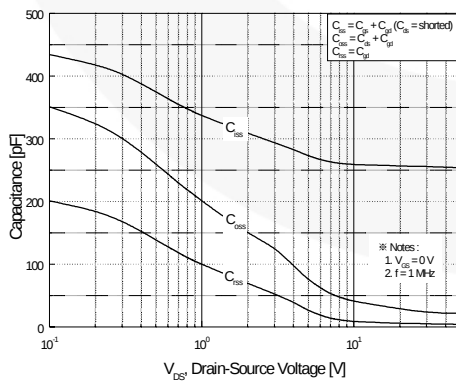


Figure 5. Capacitance Characteristics

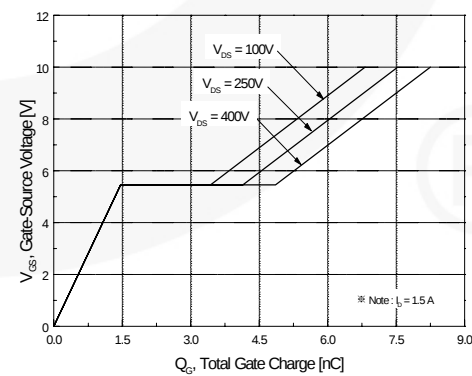


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

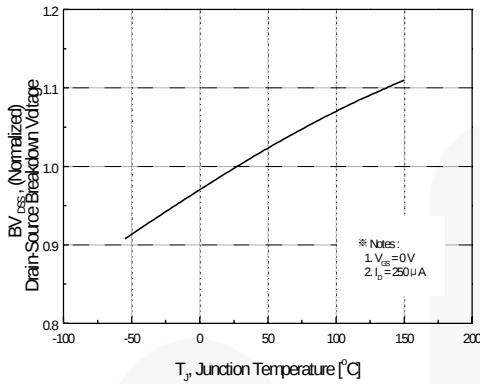


Figure 7. Breakdown Voltage Variation vs Temperature

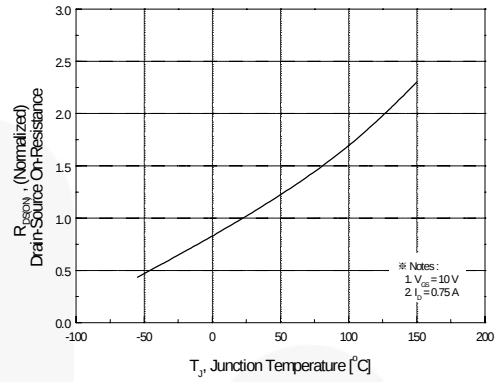


Figure 8. On-Resistance Variation vs Temperature

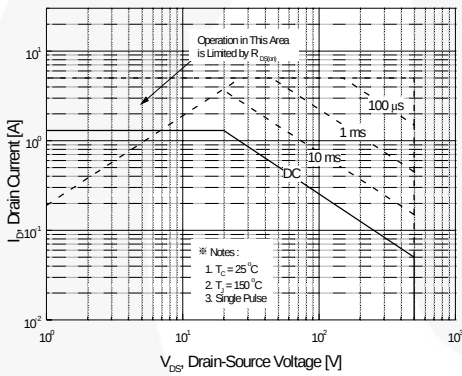


Figure 9. Maximum Safe Operating Area

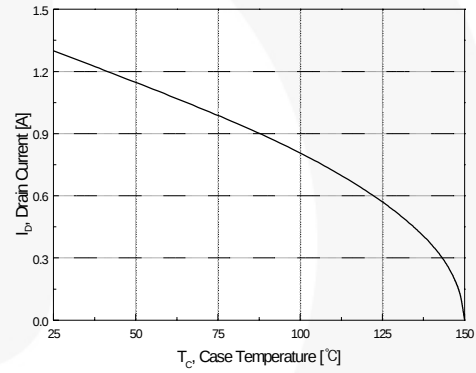


Figure 10. Maximum Drain Current vs Case Temperature

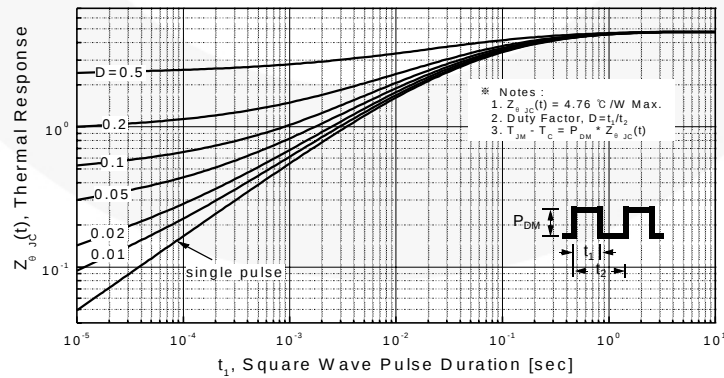


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

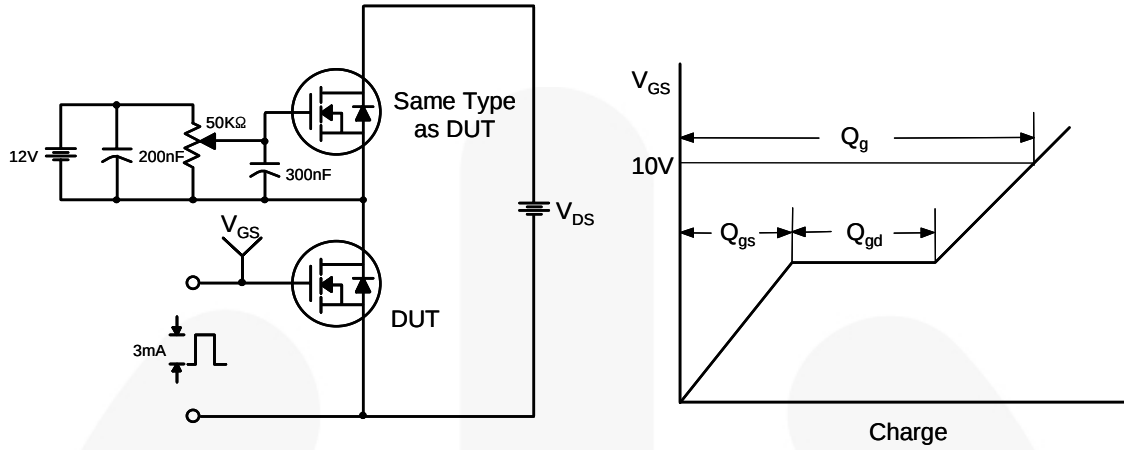


Figure 13. Resistive Switching Test Circuit & Waveforms

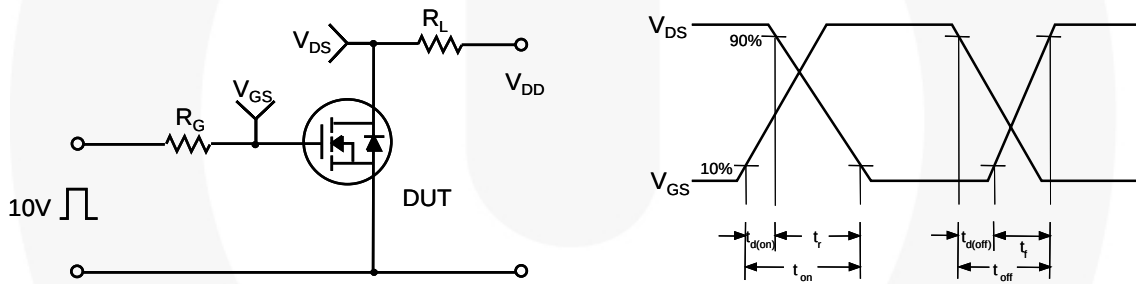


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

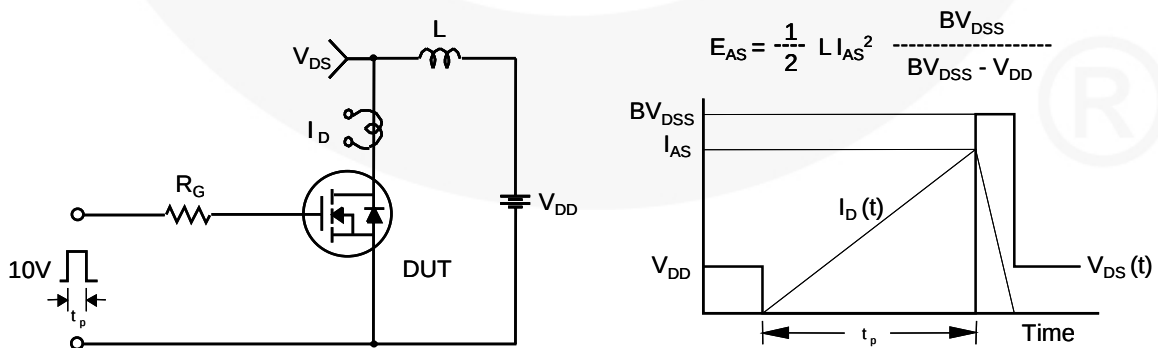
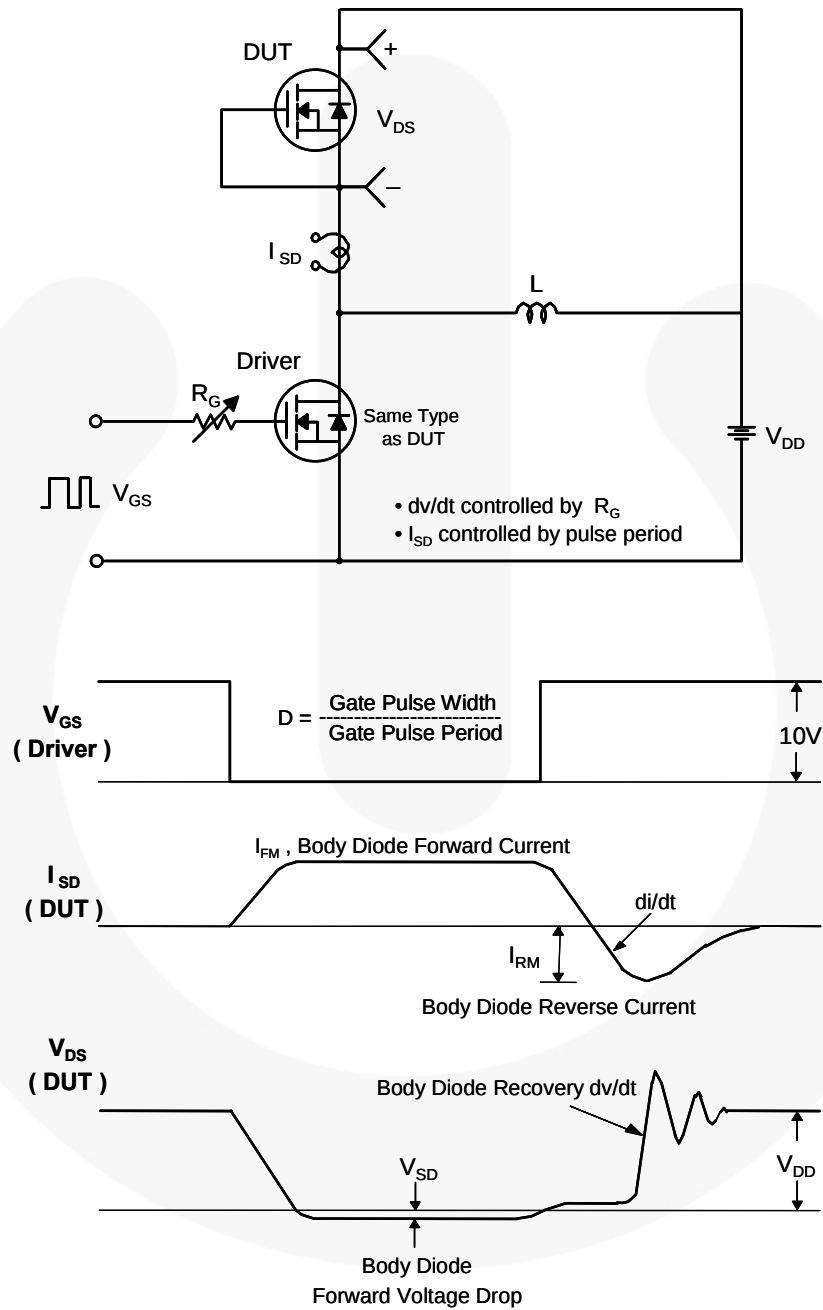
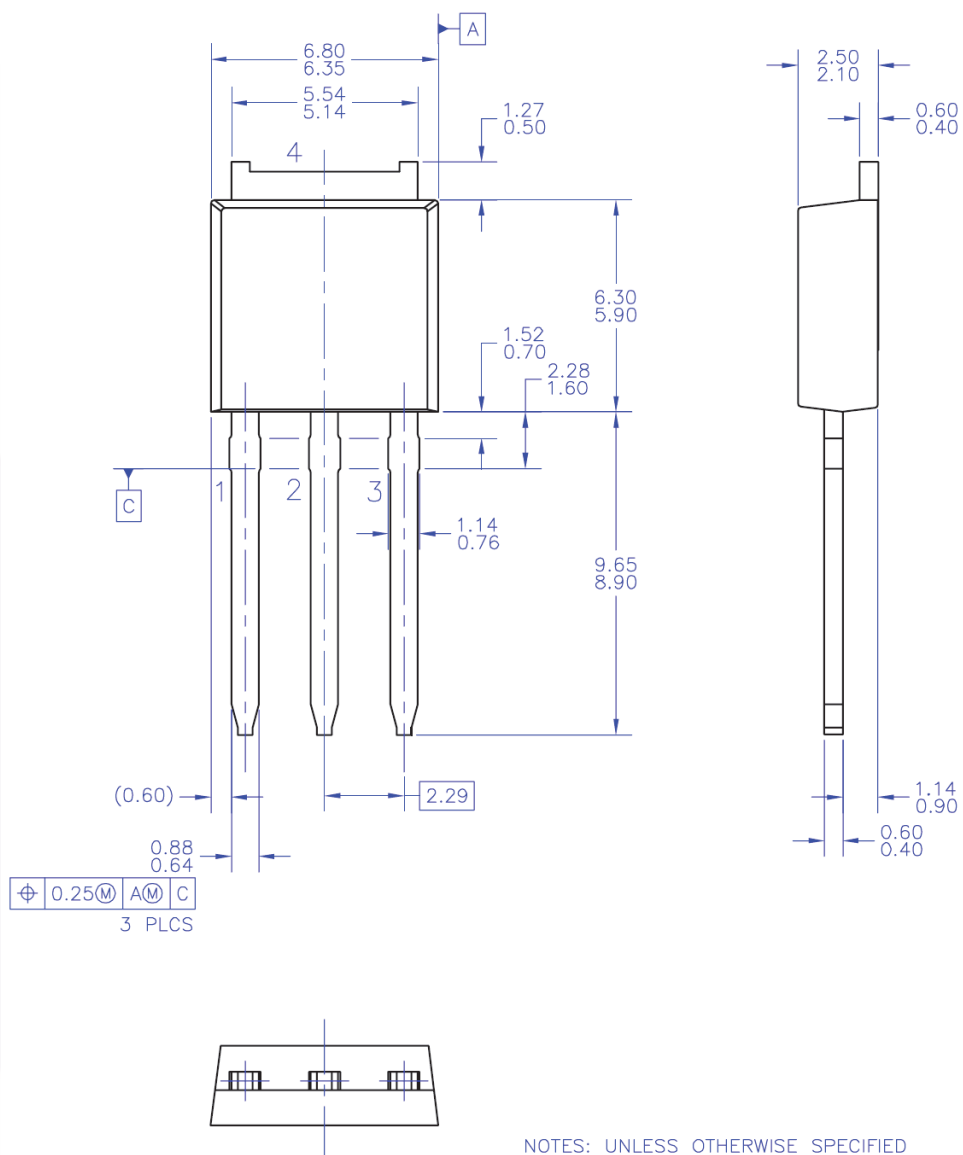


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions



TO251A03REVA

Figure 16. TO251 (I-PAK), Molded, 3-Lead

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