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SSN1N45B

N-Channel B-FET

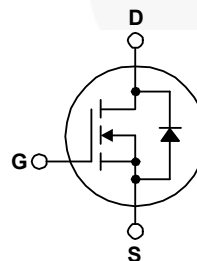
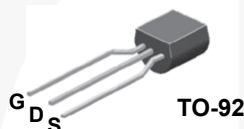
450 V, 0.5 A, 4.25 Ω

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic ballasts based on half bridge configuration.

Features

- 0.5 A, 450 V, $R_{DS(on)} = 4.25 \Omega @ V_{GS} = 10 \text{ V}$
- Low Gate Charge (typical 6.5 nC)
- Low C_{rss} (typical 6.5 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- Gate-Source Voltage $\pm 50\text{V}$ Guaranteed



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	SSN1N45BTA	Unit
V_{DSS}	Drain-Source Voltage	450	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	0.5	A
	- Continuous ($T_C = 100^\circ\text{C}$)	0.32	A
I_{DM}	Drain Current - Pulsed (Note 1)	4.0	A
V_{GSS}	Gate-Source Voltage	± 50	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	108	mJ
I_{AR}	Avalanche Current (Note 1)	0.5	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	0.25	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	5.5	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$)	0.9	W
	Power Dissipation ($T_L = 25^\circ\text{C}$)	2.5	W
	- Derate above 25°C	0.02	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	SSN1N45BTA	Unit
$R_{\theta JL}$	Thermal Resistance, Junction-to-Lead, Max. (Note 5a)	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. (Note 5b)	140	$^\circ\text{C/W}$

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
SSN1N45BTA	1N45B	TO-92	AMMO	N/A	N/A	2000 units

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	450	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.5	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 450\text{ V}, V_{GS} = 0\text{ V}$	--	--	10	μA
		$V_{DS} = 360\text{ V}, T_C = 125^\circ\text{C}$	--	--	100	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 50\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -50\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.3	3.0	3.7	V
		$V_{DS} = V_{GS}, I_D = 250\text{ mA}$	3.5	4.2	4.9	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 0.25\text{ A}$	--	3.4	4.25	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 0.25\text{ A}$	--	0.7	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	185	240	pF
C_{oss}	Output Capacitance		--	29	40	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 225\text{ V}, I_D = 0.5\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4)	--	7.5	25	ns
t_r	Turn-On Rise Time		--	21	50	ns
$t_{d(off)}$	Turn-Off Delay Time		--	23	55	ns
t_f	Turn-Off Fall Time		--	36	80	ns
Q_g	Total Gate Charge	$V_{DS} = 360\text{ V}, I_D = 0.5\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4)	--	6.5	8.5	nC
Q_{gs}	Gate-Source Charge		--	0.9	--	nC
Q_{gd}	Gate-Drain Charge		--	3.2	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	0.5	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	4.0	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.5 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 0.5 A,	--	102	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs	--	0.26	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. $L = 75\text{ mH}, I_{AS} = 1.6\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\text{ }\Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 0.5\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature.
5. a) Reference point of the $R_{\theta JA}$ is the drain lead.
b) When mounted on 3"x4.5" FR-4 PCB without any pad copper in a still air environment.
($R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance. $R_{\theta CA}$ is determined by the user's board design)

Typical Characteristics

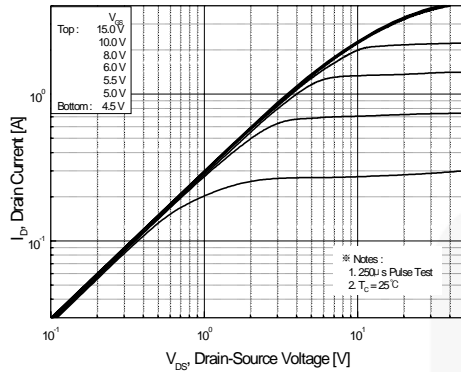


Figure 1. On-Region Characteristics

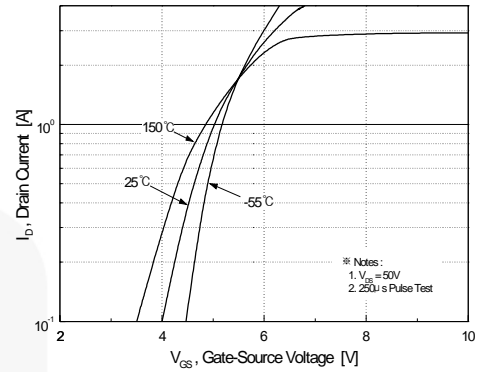


Figure 2. Transfer Characteristics

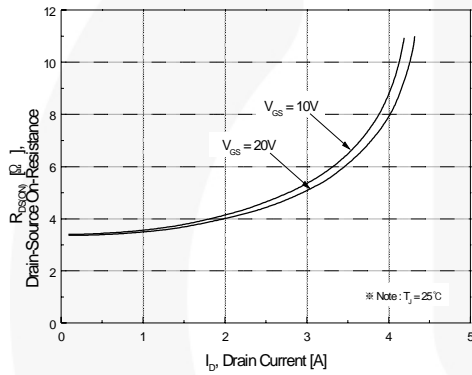


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

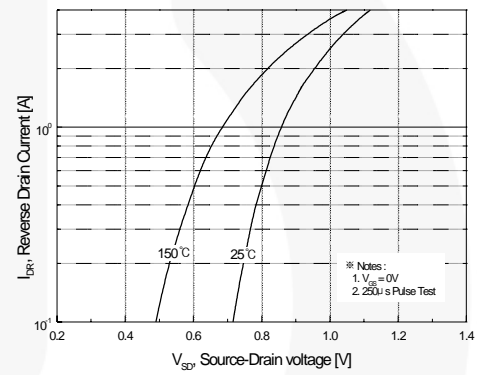


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

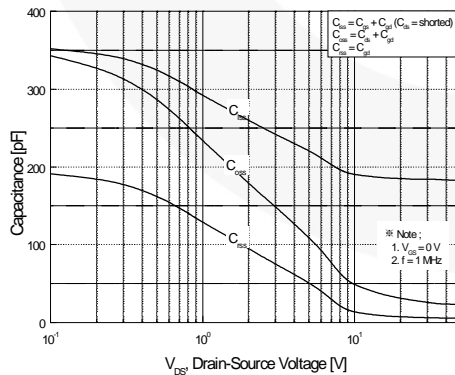


Figure 5. Capacitance Characteristics

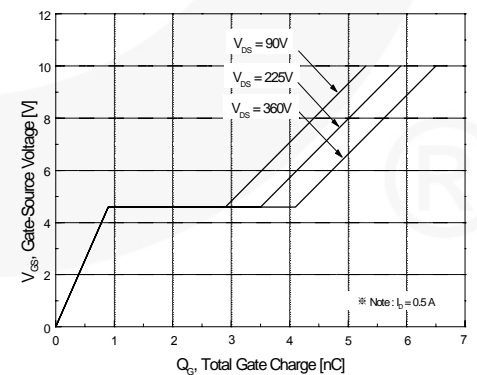


Figure 6. Gate Charge Characteristics

Typical Characteristics (continued)

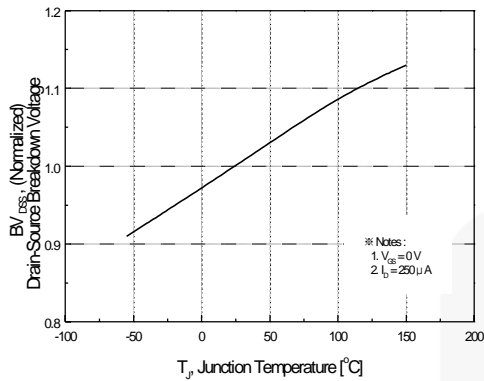


Figure 7. Breakdown Voltage Variation vs. Temperature

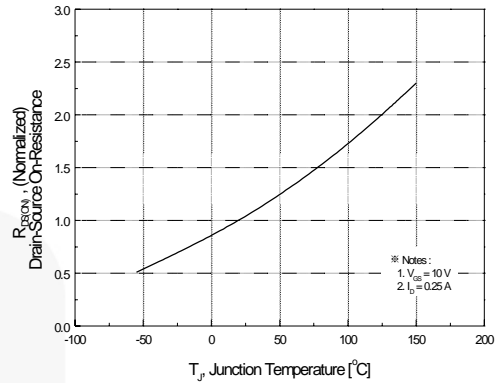


Figure 8. On-Resistance Variation vs. Temperature

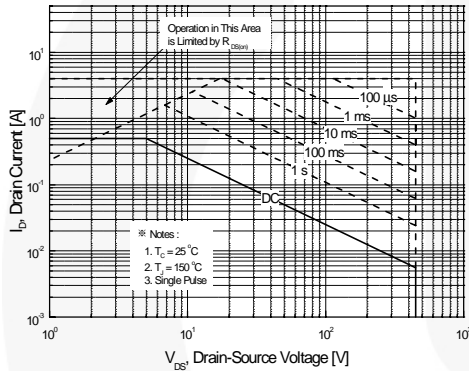


Figure 9. Maximum Safe Operating Area

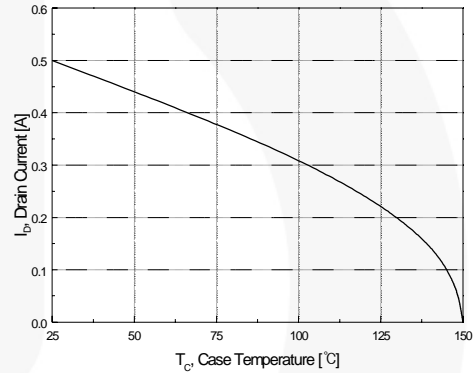


Figure 10. Maximum Drain Current vs. Case Temperature

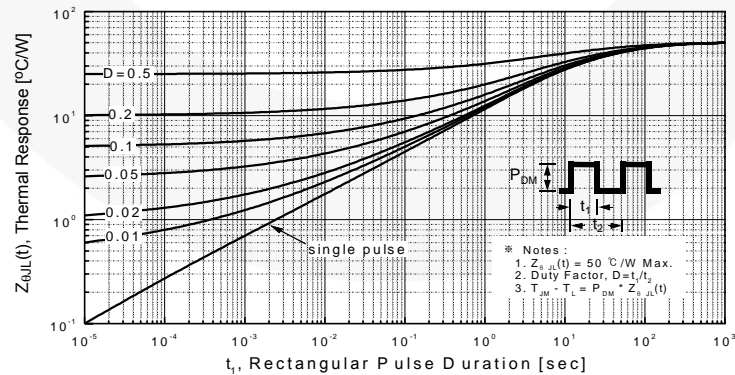


Figure 11. Transient Thermal Response Curve

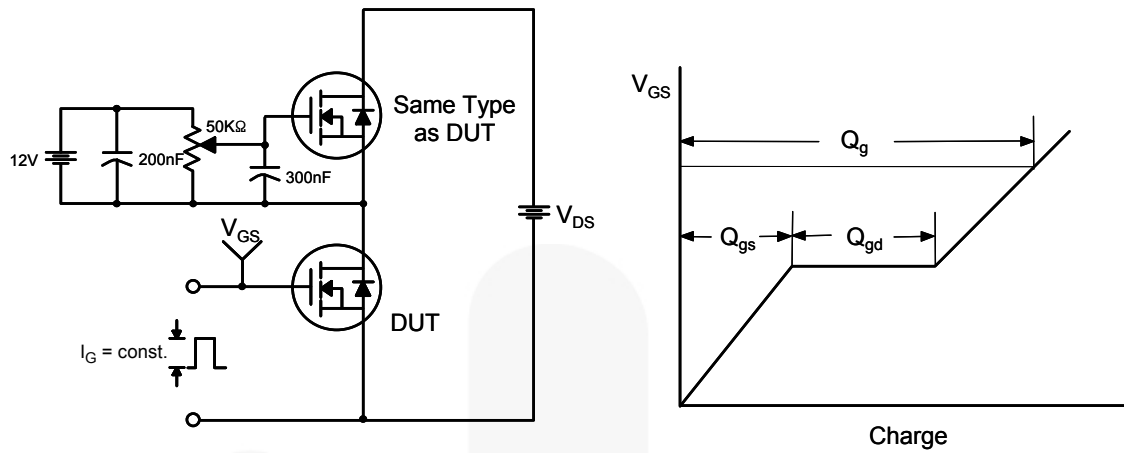


Figure 12. Gate Charge Test Circuit & Waveform

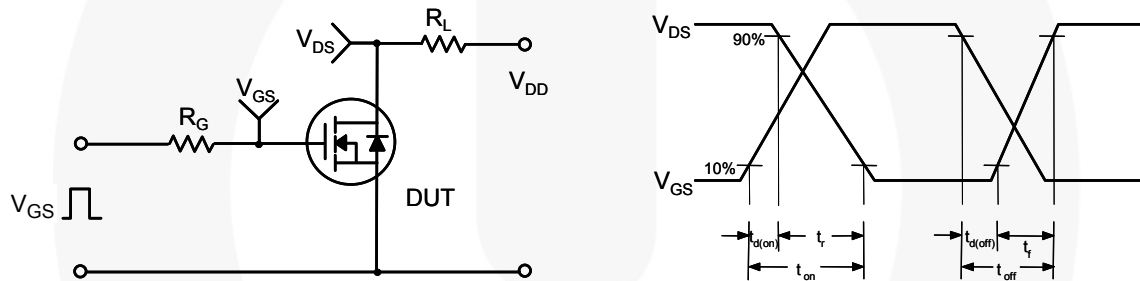


Figure 13. Resistive Switching Test Circuit & Waveforms

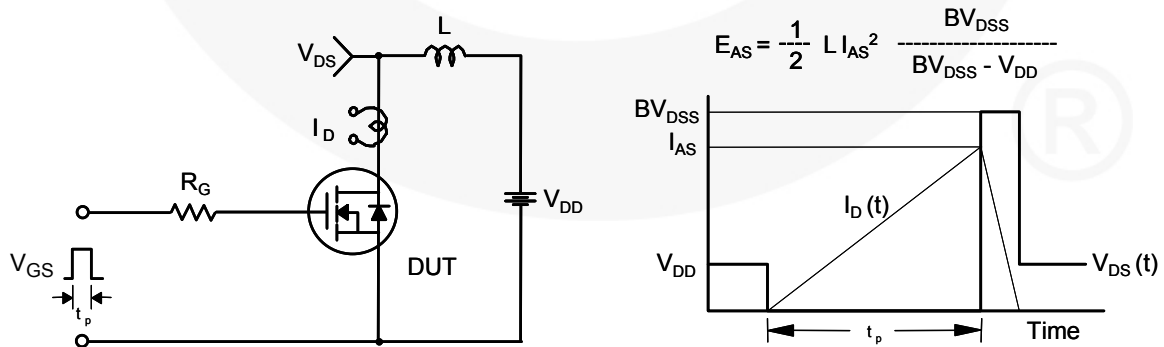
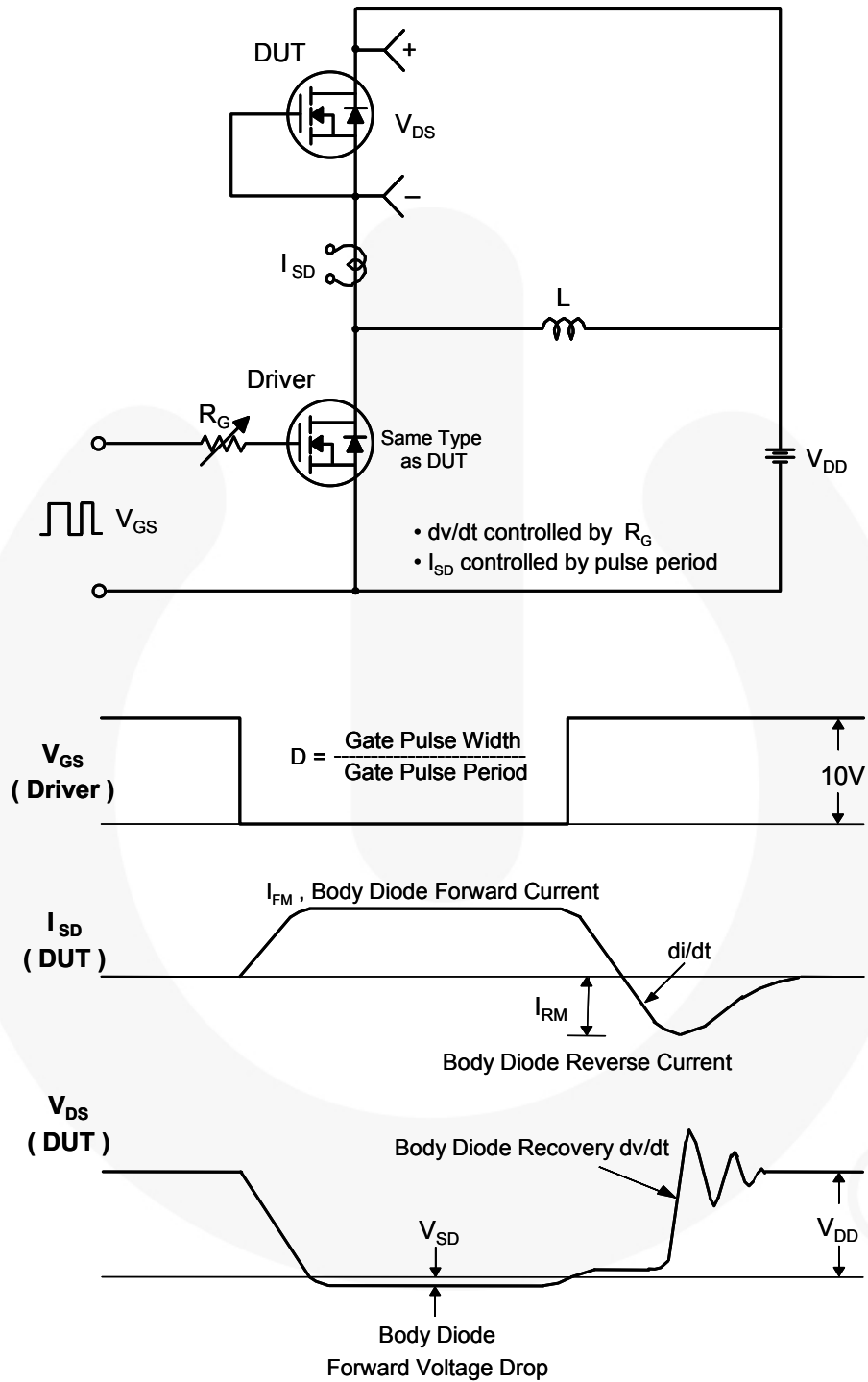


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5M-2009.
D. DRAWING FILENAME: MKT-ZA03FREV3.
E. FAIRCHILD SEMICONDUCTOR.

Figure 16. TO92, Molded, 3-Lead, 0.200 In Line Spacing LD Form (J61Z Option)

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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