SRV05-4

ESD Protection Diode Array
Low Clamping Voltage

The SRV05−4MR6 surge protection is designed to protect high speed data lines from ESD, EFT, and lighting.

Features

- Protects 4 I/O Lines
- Low Working Voltage: 5 V
- Low Clamping Voltage
- Low Capacitance (<5 pF) for High Speed Interfaces
- Transient Protection for High Speed Lines to:
  IEC61000−4−2 (ESD) ±15 kV (air), ±8 kV (contact)
  IEC61000−4−4 (EFT) 40 A
  IEC61000−4−5 (Lightning) 12 A
- TSOP−6 is Footprint Compatible with SOT−23 6 Lead, SC−59 6 Lead and SC−74
- UL Flammability Rating of 94 V−0
- This is a Pb−Free Device

Typical Applications

- High Speed Communication Line Protection
- USB 1.1 and 2.0 Power and Data Line Protection
- Digital Video Interface (DVI)
- Monitors and Flat Panel Displays

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Power Dissipation 8 x 20 μs @ T_A = 25°C (Note 1)	P_{pk}	300	W
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000−4−2 Air (ESD) IEC 61000−4−2 Contact (ESD)	ESD	16000 400 30000 30000	V
IEC 61000−4−4 (5/50 ns)	EFT	40	A
IEC 61000−4−5 (8 x 20 μs)	−	12	A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Non−repetitive current pulse per Figure 5 (Pin 5 to Pin 2)

See Application Note AND8308/D for further description of survivability specs.

ON Semiconductor®

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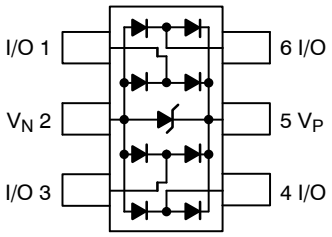
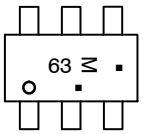
LOW CAPACITANCE SURGE PROTECTION ARRAY 300 WATTS PEAK POWER 6 VOLTS

PIN CONFIGURATION AND SCHEMATIC



TSOP−6
CASE 318G
PLASTIC

MARKING DIAGRAM



63 = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)
*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping
SRV05−4MR6T1G	TSOP−6 (Pb−Free)	3000/Tape & Reel

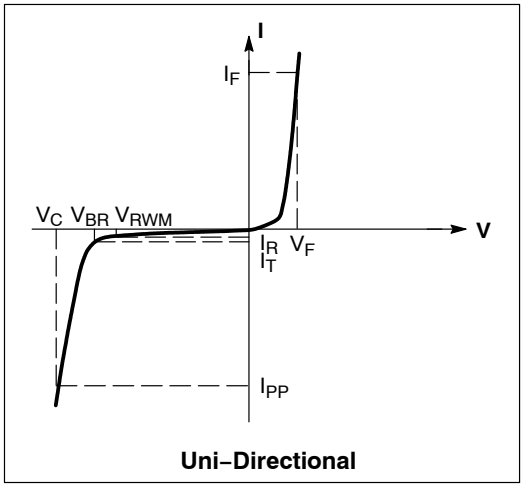
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current
I_F	Forward Current
V_F	Forward Voltage @ I_F
P_{pk}	Peak Power Dissipation
C	Capacitance @ V_R = 0 and f = 1.0 MHz

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	(Note 2)			5.0	V
Breakdown Voltage	V_{BR}	I_T=1 mA, (Note 3)	6.0			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V			5.0	μA
Clamping Voltage	V_C	I_{PP} = 1 A (Note 4)			12.5	V
Clamping Voltage	V_C	I_{PP} = 5 A (Note 4)			17.5	V
Junction Capacitance	C_J	V_R = 0 V, f=1 MHz between I/O Pins and GND		3.0	5.0	pF
Junction Capacitance	C_J	V_R = 0 V, f=1 MHz between I/O Pins		1.5	3.0	pF
Clamping Voltage	V_C	Per IEC 61000−4−2 (Note 5)	Figure 1 and 2			V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Surge protection devices are normally selected according to the working peak reverse voltage (V_{RWM}), which should be equal or greater than the DC or continuous peak operating voltage level.
3. V_{BR} is measured at pulse test current I_T.
4. Non−repetitive current pulse per Figure 5 (Any I/O Pin to Ground)
5. For test procedure see Figures 3 and 4 and Application Note AND8307/D.

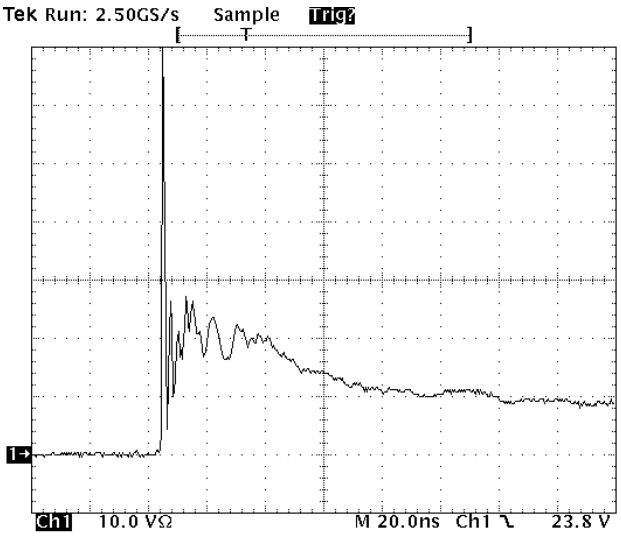


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

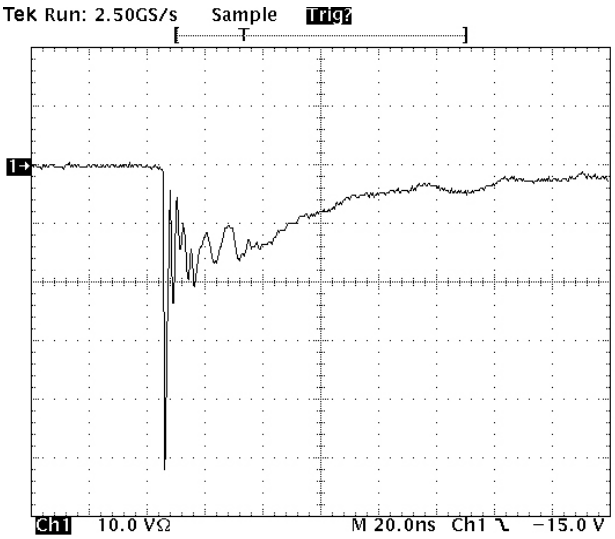


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

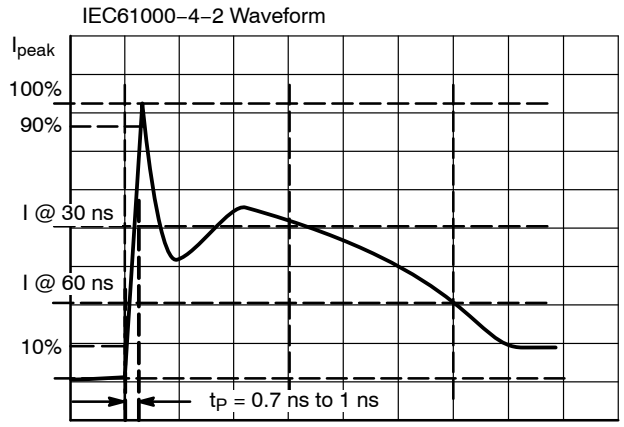


Figure 3. IEC61000−4−2 Spec

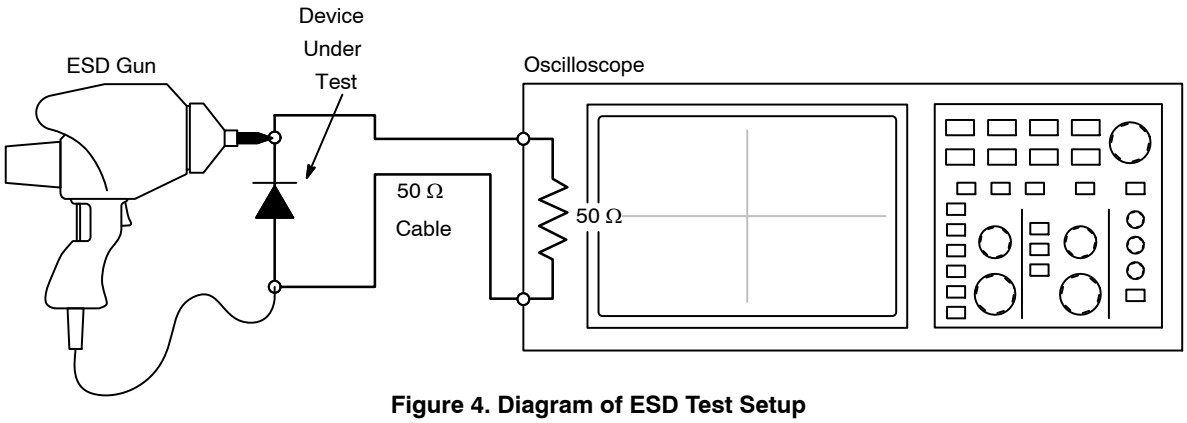


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

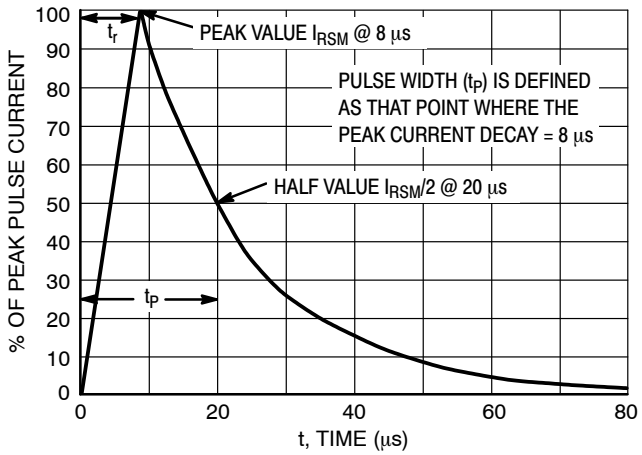


Figure 5. 8 x 20 μs Pulse Waveform

TYPICAL PERFORMANCE CURVES

(T_J = 25°C unless otherwise noted)

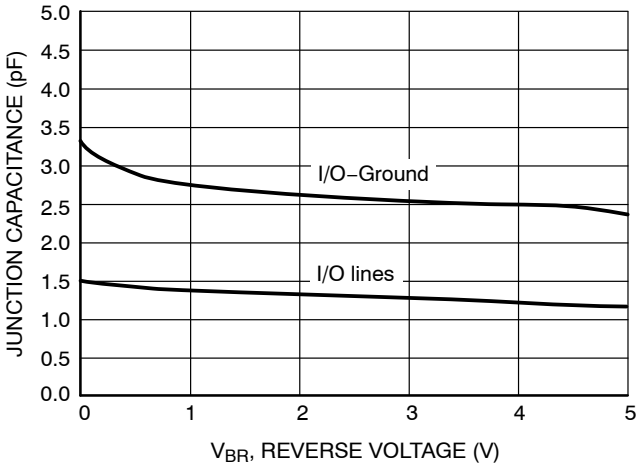


Figure 6. Junction Capacitance vs Reverse Voltage

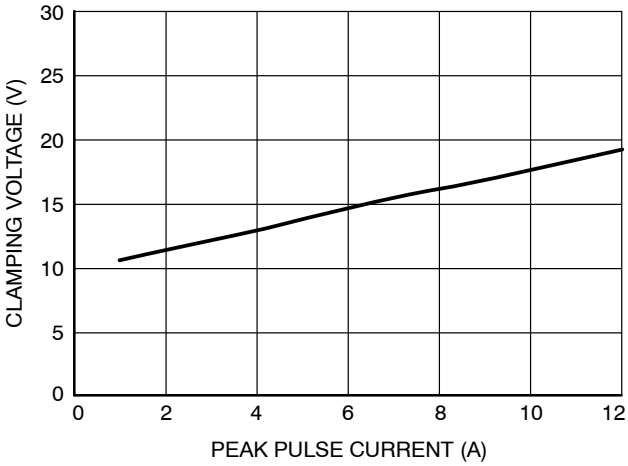


Figure 7. Clamping Voltage vs. Peak Pulse Current (8 x 20 μs Waveform)

APPLICATIONS INFORMATION

The new SRV05−4MR6 is a low capacitance surge protection diode array designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD events or transient overvoltage conditions. Because of its low capacitance, it can be used in high speed I/O data lines. The integrated design of the SRV05−4MR6 offers surge rated, low capacitance steering diodes and a surge protection diode integrated in a single package (TSOP−6). If a transient condition occurs, the steering diodes will drive the transient to the positive rail of the power supply or to ground. The surge protection device protects the power line against overvoltage conditions to avoid damage to the power supply and any downstream components.

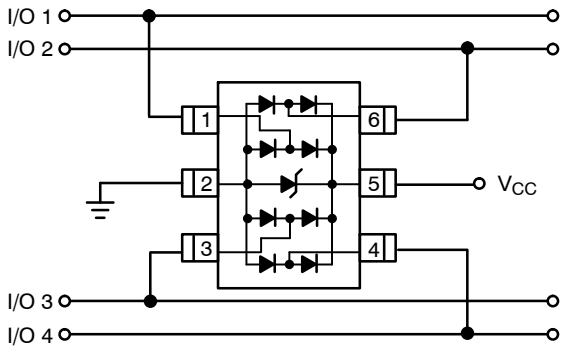
SRV05−4MR6 Configuration Options

The SRV05−4MR6 is able to protect up to four data lines against transient overvoltage conditions by driving them to a fixed reference point for clamping purposes. The steering diodes will be forward biased whenever the voltage on the protected line exceeds the reference voltage (Vf or V_{CC} + Vf). The diodes will force the transient current to bypass the sensitive circuit.

Data lines are connected at pins 1, 3, 4 and 6. The negative reference is connected at pin 2. These pins must be connected directly to ground by using a ground plane to minimize the PCB's ground inductance. It is very important to reduce the PCB trace lengths as much as possible to minimize parasitic inductances.

Option 1

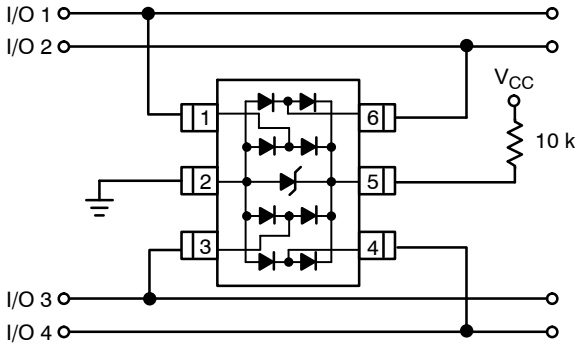
Protection of four data lines and the power supply using V_{CC} as reference.



For this configuration, connect pin 5 directly to the positive supply rail (V_{CC}), the data lines are referenced to the supply voltage. The internal surge protection diode prevents overvoltage on the supply rail. Biasing of the steering diodes reduces their capacitance.

Option 2

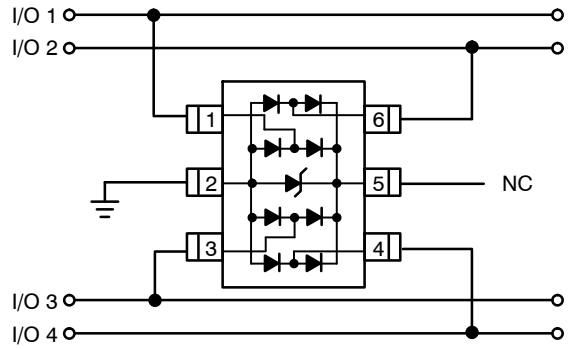
Protection of four data lines with bias and power supply isolation resistor.



The SRV05−4MR6 can be isolated from the power supply by connecting a series resistor between pin 5 and V_{CC}. A 10 kΩ resistor is recommended for this application. This will maintain a bias on the internal surge protection and steering diodes, reducing their capacitance.

Option 3

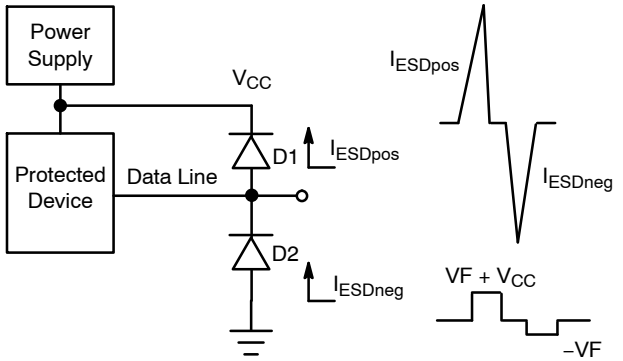
Protection of four data lines using the internal surge protection diode as reference.



In applications lacking a positive supply reference or those cases in which a fully isolated power supply is required, the internal surge protection can be used as the reference. For these applications, pin 5 is not connected. In this configuration, the steering diodes will conduct whenever the voltage on the protected line exceeds the working voltage of the surge protection plus one diode drop ($V_C = V_f + V_{RWM}$).

ESD Protection of Power Supply Lines

When using diodes for data line protection, referencing to a supply rail provides advantages. Biasing the diodes reduces their capacitance and minimizes signal distortion. Implementing this topology with discrete devices does have disadvantages. This configuration is shown below:



Looking at the figure above, it can be seen that when a positive ESD condition occurs, diode D1 will be forward biased while diode D2 will be forward biased when a negative ESD condition occurs. For slower transient conditions, this system may be approximated as follows:

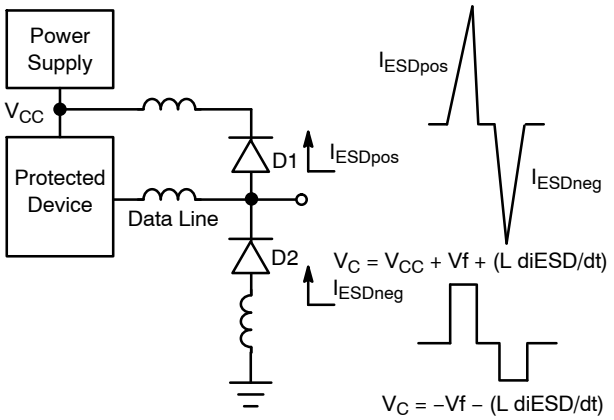
For positive pulse conditions:

$Vc = V_{CC} + Vf_{D1}$

For negative pulse conditions:

$Vc = -Vf_{D2}$

ESD events can have rise times on the order of some number of nanoseconds. Under these conditions, the effect of parasitic inductance must be considered. A pictorial representation of this is shown below.



An approximation of the clamping voltage for these fast transients would be:

For positive pulse conditions:

$Vc = V_{CC} + Vf + (L\ di_{ESD}/dt)$

For negative pulse conditions:

$Vc = -Vf - (L\ di_{ESD}/dt)$

As shown in the formulas, the clamping voltage (Vc) not only depends on the Vf of the steering diodes but also on the $L\ d_{iESD}/dt$ factor. A relatively small trace inductance can result in hundreds of volts appearing on the supply rail. This endangers both the power supply and anything attached to that rail. This highlights the importance of good board layout. Taking care to minimize the effects of parasitic inductance will provide significant benefits in transient immunity.

Even with good board layout, some disadvantages are still present when discrete diodes are used to suppress ESD events across datalines and the supply rail. Discrete diodes with good transient power capability will have larger die and therefore higher capacitance. This capacitance becomes problematic as transmission frequencies increase. Reducing capacitance generally requires reducing die size. These small die will have higher forward voltage characteristics at typical ESD transient current levels. This voltage combined with the smaller die can result in device failure.

The ON Semiconductor SRV05−4MR6 was developed to overcome the disadvantages encountered when using discrete diodes for ESD protection. This device integrates a surge protection diode within a network of steering diodes.

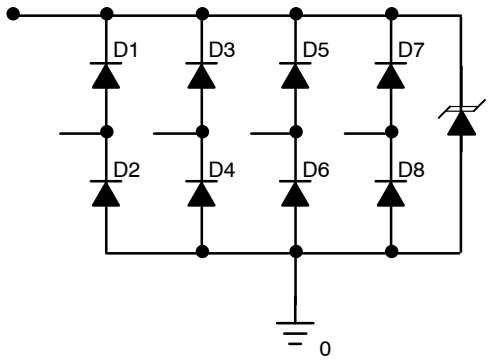
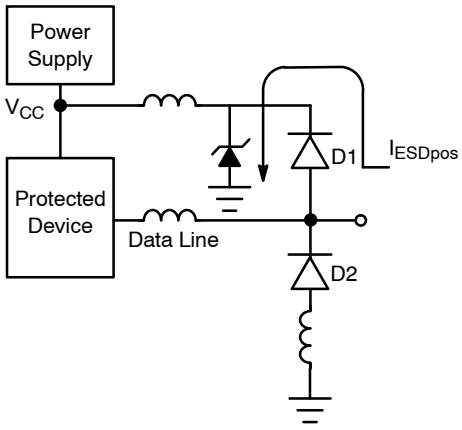


Figure 8. SRV05−4MR6 Equivalent Circuit

During an ESD condition, the ESD current will be driven to ground through the surge protection diode as shown below.



The resulting clamping voltage on the protected IC will be: $Vc = VF + V_{RWM}$.

The clamping voltage of the surge protection diode is provided in Figure 7 and depends on the magnitude of the ESD current. The steering diodes are fast switching devices with unique forward voltage and low capacitance characteristics.

TYPICAL APPLICATIONS

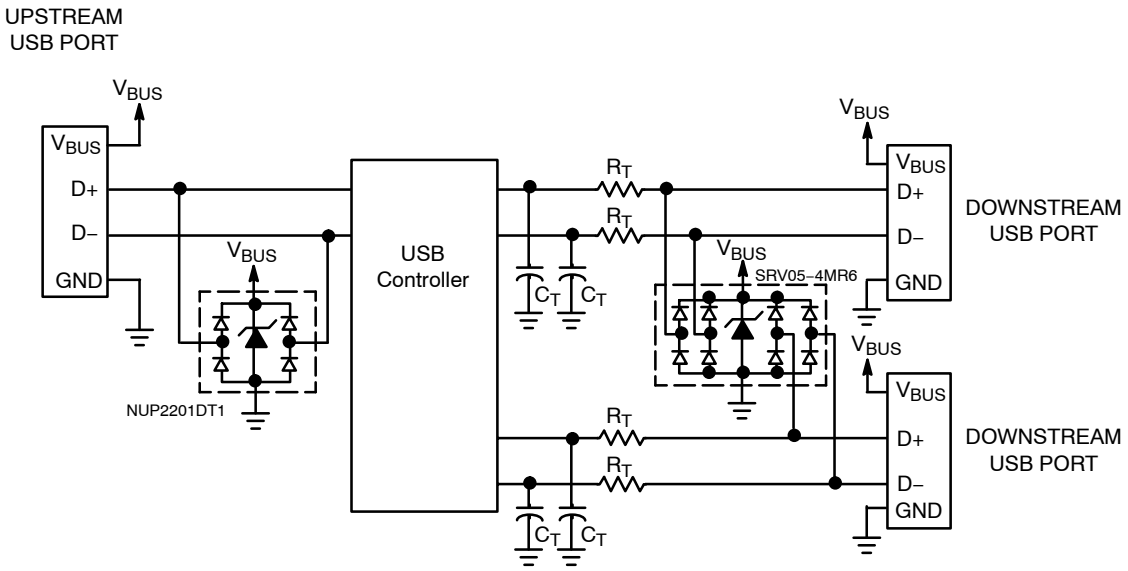


Figure 9. ESD Protection for USB Port

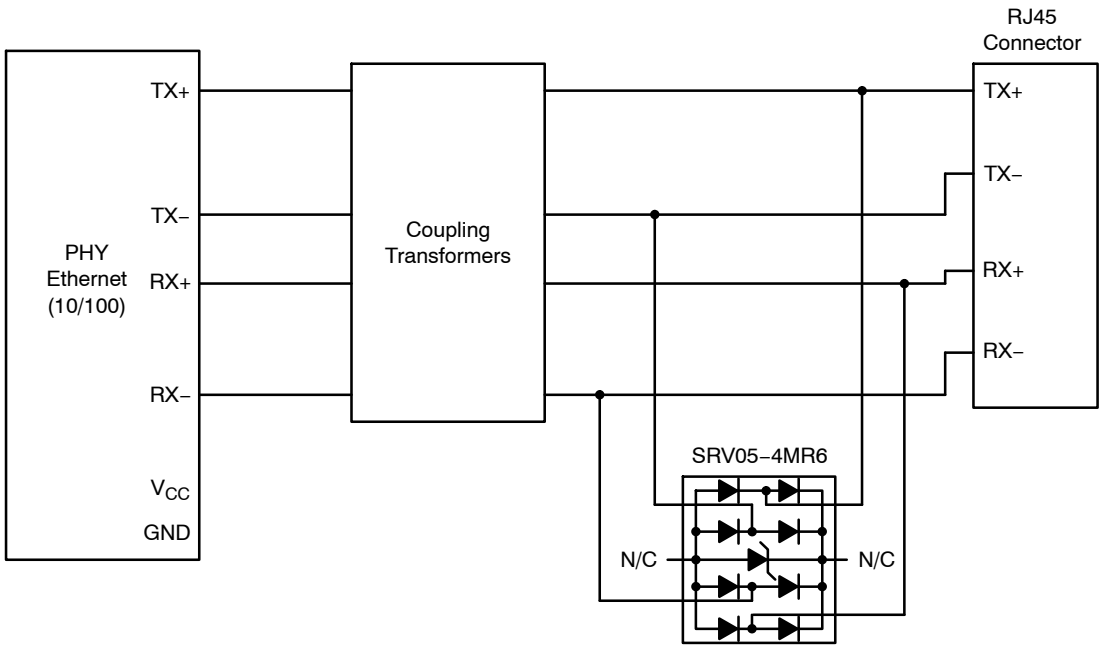


Figure 10. Protection for Ethernet 10/100 (Differential mode)

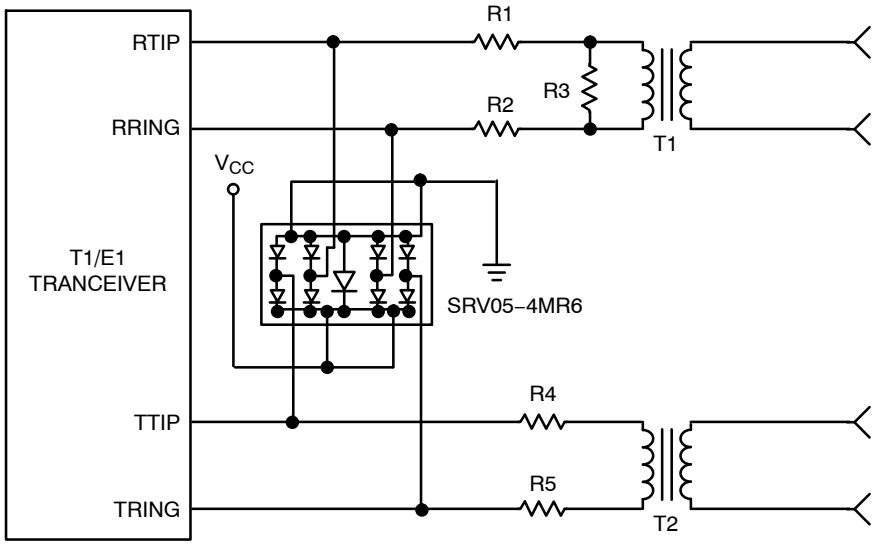


Figure 11. TI/E1 Interface Protection

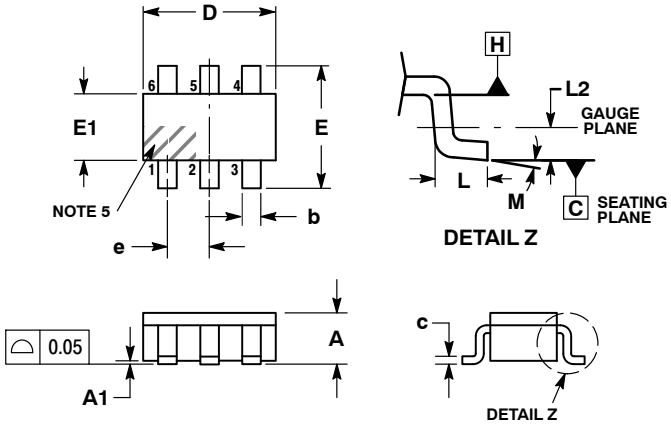
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

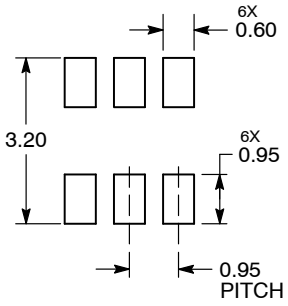
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

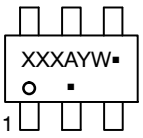
RECOMMENDED SOLDERING FOOTPRINT*



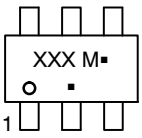
DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present.

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DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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onsemi Website: www.onsemi.com

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Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

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