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FEATURES

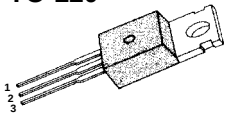
- Avalanche Rugged Technology
- Rugged Gate Oxide Technology
- Lower Input Capacitance
- Improved Gate Charge
- 175°C Operating Temperature
- Extended Safe Operating Area
- Lower Leakage Current : -10 μA (Max.) @ V_{DS} = -100V
- Low R_{DS(ON)} : 0.225 Ω (Typ.)

$BV_{DSS} = -100\text{ V}$

$R_{DS(on)} = 0.3\ \Omega$

$I_D = -10.5\text{ A}$

TO-220



1.Gate 2. Drain 3. Source

Absolute Maximum Ratings

Symbol	Characteristic	Value	Units
V _{DSS}	Drain-to-Source Voltage	-100	V
I _D	Continuous Drain Current (T _C =25°C)	-10.5	A
	Continuous Drain Current (T _C =100°C)	-7.5	
I _{DM}	Drain Current-Pulsed ①	-42	A
V _{GS}	Gate-to-Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy ②	368	mJ
I _{AR}	Avalanche Current ①	-10.5	A
E _{AR}	Repetitive Avalanche Energy ①	6.6	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-6.5	V/ns
P _D	Total Power Dissipation (T _C =25°C)	66	W
	Linear Derating Factor	0.44	W/°C
T _J , T _{STG}	Operating Junction and Storage Temperature Range	- 55 to +175	°C
T _L	Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5-seconds	300	

Thermal Resistance

Symbol	Characteristic	Typ.	Max.	Units
R _{θJC}	Junction-to-Case	--	2.27	°C/W
R _{θCS}	Case-to-Sink	0.5	--	
R _{θJA}	Junction-to-Ambient	--	62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise specified)

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
BV_{DSS}	Drain-Source Breakdown Voltage	-100	--	--	V	$V_{GS}=0V, I_D=-250\mu A$
$\Delta BV/\Delta T_J$	Breakdown Voltage Temp. Coeff.	--	-0.1	--	$V/^\circ\text{C}$	$I_D=-250\mu A$ See Fig 7
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	--	-4.0	V	$V_{DS}=-5V, I_D=-250\mu A$
I_{GSS}	Gate-Source Leakage, Forward	--	--	-100	nA	$V_{GS}=-20V$
	Gate-Source Leakage, Reverse	--	--	100		$V_{GS}=20V$
I_{DSS}	Drain-to-Source Leakage Current	--	--	-10	μA	$V_{DS}=-100V$
		--	--	-100		$V_{DS}=-80V, T_C=150^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-State Resistance	--	--	0.3	Ω	$V_{GS}=-10V, I_D=-5.3A$ ④
g_{fs}	Forward Transconductance	--	5.5	--	S	$V_{DS}=-40V, I_D=-5.3A$ ④
C_{iss}	Input Capacitance	--	800	1035	pF	$V_{GS}=0V, V_{DS}=-25V, f=1\text{MHz}$ See Fig 5
C_{oss}	Output Capacitance	--	160	240		
C_{rss}	Reverse Transfer Capacitance	--	60	90		
$t_{d(on)}$	Turn-On Delay Time	--	13	35	ns	$V_{DD}=-50V, I_D=-10.5A,$ $R_G=12\Omega$ See Fig 13 ④⑤
t_r	Rise Time	--	22	55		
$t_{d(off)}$	Turn-Off Delay Time	--	45	100		
t_f	Fall Time	--	25	60		
Q_g	Total Gate Charge	--	30	38	nC	$V_{DS}=-80V, V_{GS}=-10V,$ $I_D=-10.5A$ See Fig 6 & Fig 12 ④⑤
Q_{gs}	Gate-Source Charge	--	5.4	--		
Q_{gd}	Gate-Drain("Miller") Charge	--	12.2	--		

Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Typ.	Max.	Units	Test Condition
I_S	Continuous Source Current	--	--	-10.5	A	Integral reverse pn-diode in the MOSFET
I_{SM}	Pulsed-Source Current ①	--	--	-42		
V_{SD}	Diode Forward Voltage ④	--	--	-4.0	V	$T_J=25^\circ\text{C}, I_S=-10.5A, V_{GS}=0V$
t_{rr}	Reverse Recovery Time	--	120	--	ns	$T_J=25^\circ\text{C}, I_F=-10.5A$
Q_{rr}	Reverse Recovery Charge	--	0.53	--	μC	$di_F/dt=100A/\mu s$ ④

Notes ;

- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature
 ② $L=5.0\text{mH}, I_{AS}=-10.5A, V_{DD}=-25V, R_G=27\Omega^*,$ Starting $T_J=25^\circ\text{C}$
 ③ $I_{SD}\leq -10.5A, di/dt\leq 400A/\mu s, V_{DD}\leq BV_{DSS},$ Starting $T_J=25^\circ\text{C}$
 ④ Pulse Test : Pulse Width = $250\mu s,$ Duty Cycle $\leq 2\%$
 ⑤ Essentially Independent of Operating Temperature

Fig 1. Output Characteristics

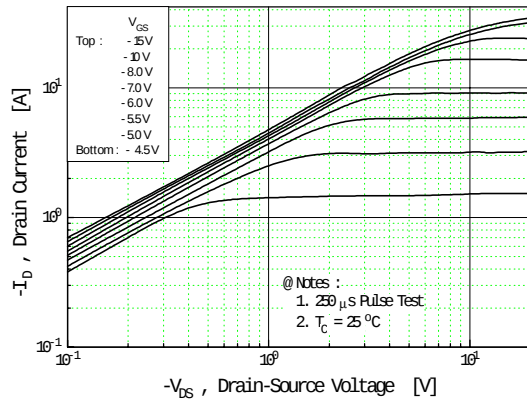


Fig 2. Transfer Characteristics

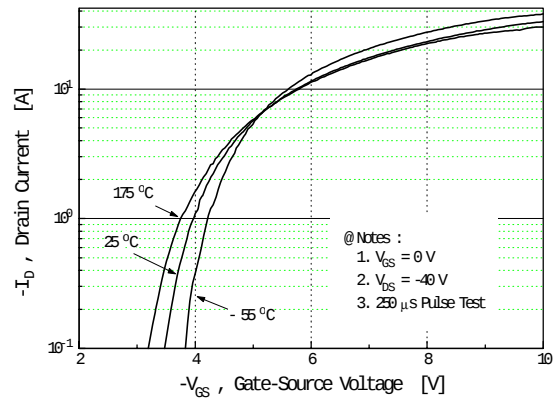


Fig 3. On-Resistance vs. Drain Current

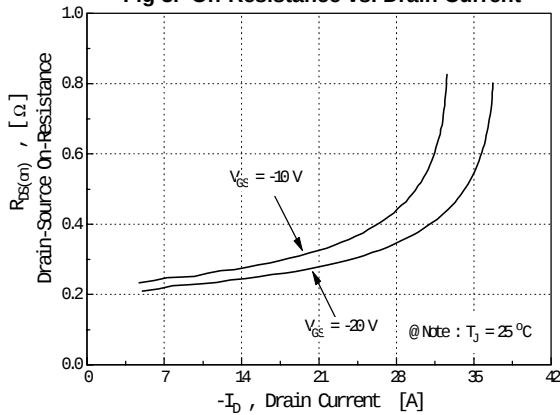


Fig 4. Source-Drain Diode Forward Voltage

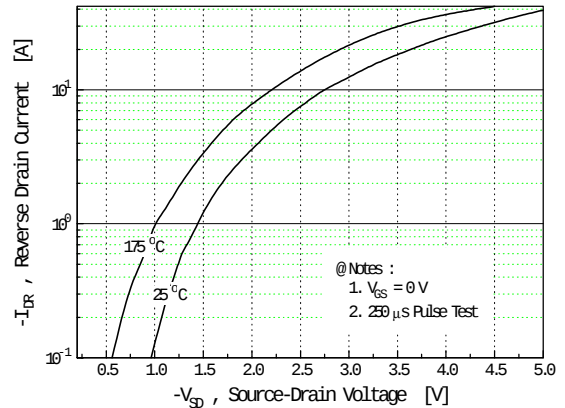


Fig 5. Capacitance vs. Drain-Source Voltage

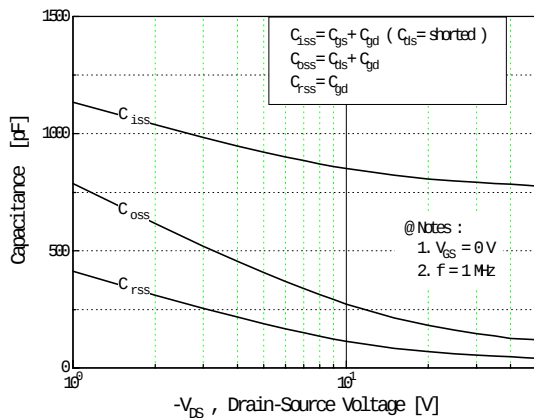


Fig 6. Gate Charge vs. Gate-Source Voltage

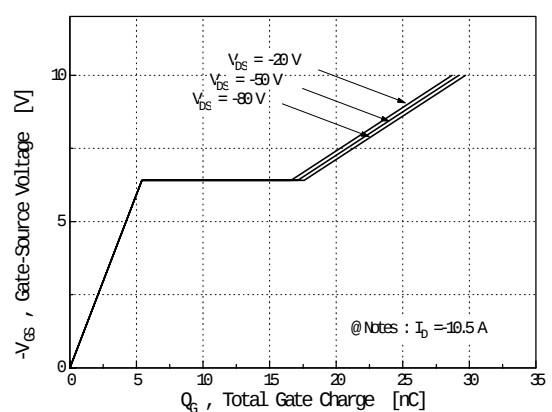


Fig 7. Breakdown Voltage vs. Temperature

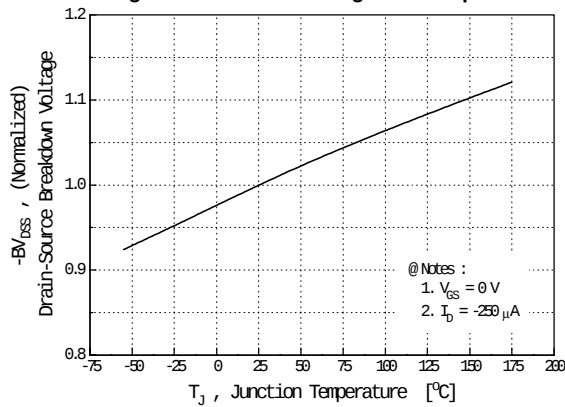


Fig 8. On-Resistance vs. Temperature

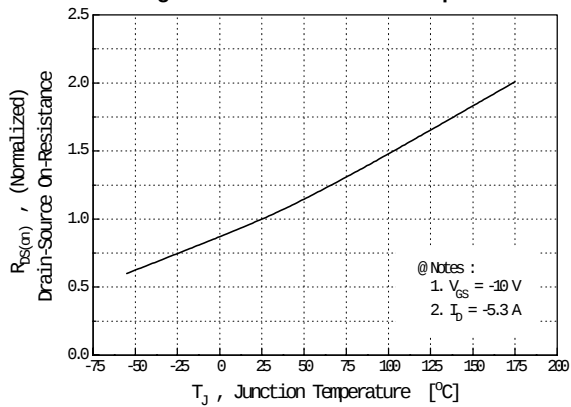


Fig 9. Max. Safe Operating Area

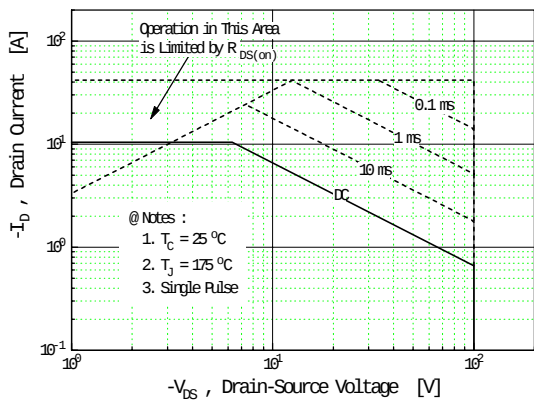


Fig 10. Max. Drain Current vs. Case Temperature

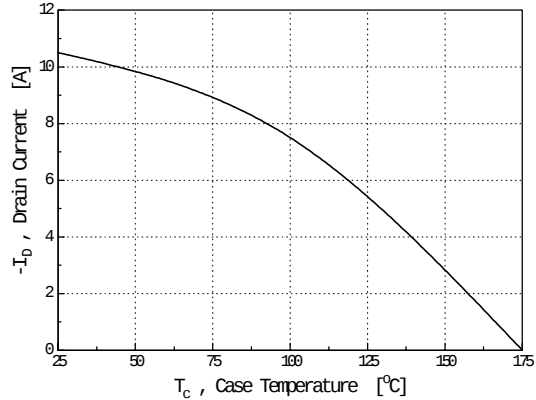


Fig 11. Thermal Response

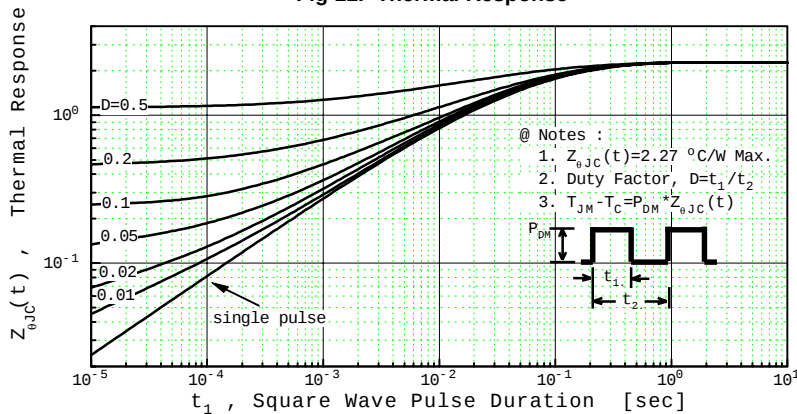


Fig 12. Gate Charge Test Circuit & Waveform

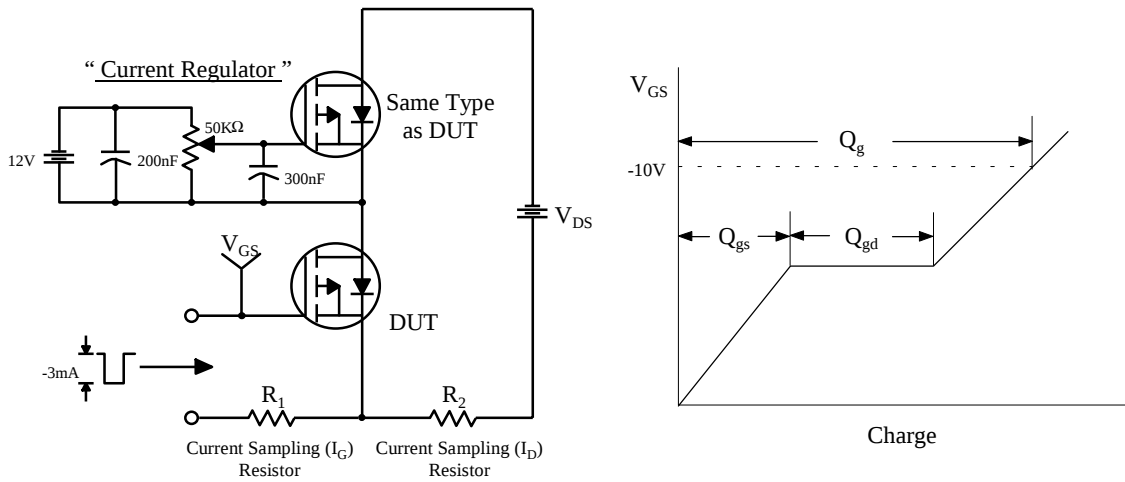


Fig 13. Resistive Switching Test Circuit & Waveforms

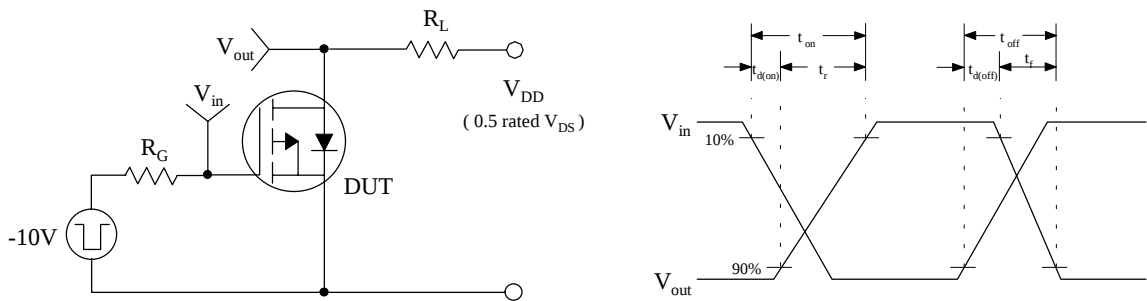


Fig 14. Unclamped Inductive Switching Test Circuit & Waveforms

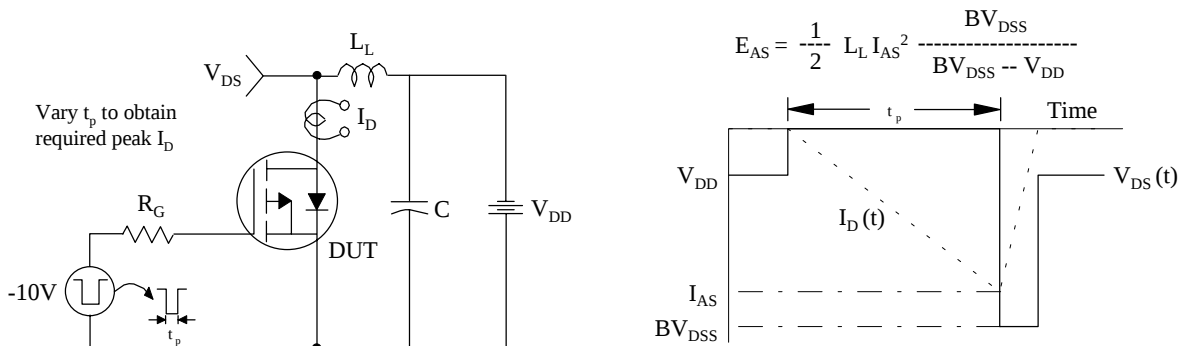
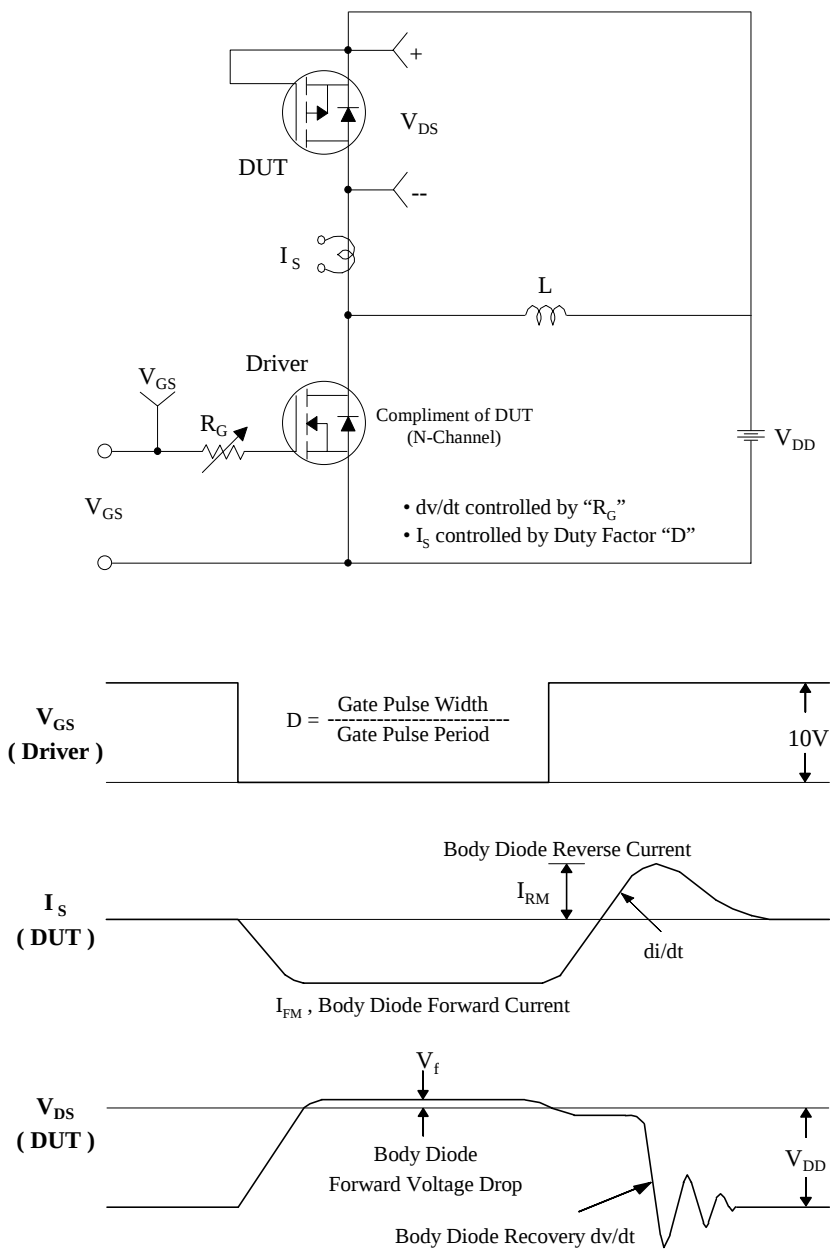


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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