

PZTA96ST1G

High Voltage Transistor

PNP Silicon

Features

- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	-450	Vdc
Collector-Base Voltage	V_{CBO}	-450	Vdc
Emitter-Base Voltage	V_{EBO}	-5.0	Vdc
Collector Current	I_C	-500	mAdc
Total Power Dissipation Up to $T_A = 25^\circ\text{C}$ (Note 1)	P_D	1.5	W
Storage Temperature Range	T_{stg}	-65 to +150	°C
Junction Temperature	T_J	150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 in².

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	83.3	°C

2. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 in².

ELECTRICAL CHARACTERISTICS (Note 3)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector-Emitter Breakdown Voltage ($I_C = -1.0$ mAdc, $I_B = 0$)	$V_{(BR)CEO}$	-450	-	Vdc
Collector-Emitter Breakdown Voltage ($I_C = -100$ µAdc, $I_E = 0$)	$V_{(BR)CBO}$	-450	-	Vdc
Emitter-Base Breakdown Voltage ($I_E = -10$ µAdc, $I_C = 0$)	$V_{(BR)EBO}$	-5.0	-	Vdc
Collector-Base Cutoff Current ($V_{CB} = -400$ Vdc, $I_E = 0$)	I_{CBO}	-	-0.1	µAdc
Emitter-Base Cutoff Current ($V_{BE} = -4.0$ Vdc, $I_C = 0$)	I_{EBO}	-	-0.1	µAdc

ON CHARACTERISTICS

DC Current Gain (Note 4) ($I_C = -10$ mAdc, $V_{CE} = -10$ Vdc)	h_{FE}	50	150	-
Saturation Voltages ($I_C = -20$ mAdc, $I_B = -2.0$ mAdc) ($I_C = -20$ mAdc, $I_B = -2.0$ mAdc)	$V_{CE(\text{sat})}$ $V_{BE(\text{sat})}$	-	-0.6 -1.0	Vdc

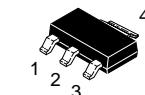
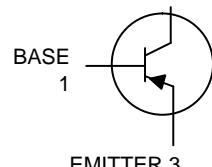
3. $T_A = 25^\circ\text{C}$ unless otherwise noted.
4. Pulse Test: Pulse Width ≤ 300 µs; Duty Cycle = 2.0%.



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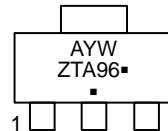
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COLLECTOR 2,4



SOT-223 (TO-261)
CASE 318E
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
PZTA96ST1G	SOT-223 (Pb-Free)	1000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

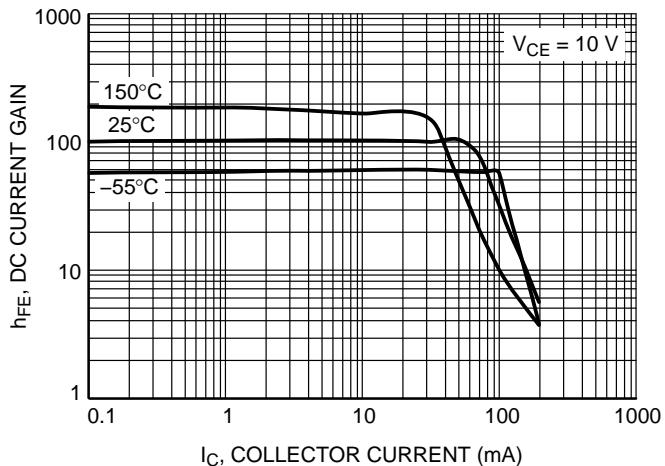


Figure 1. DC Current Gain

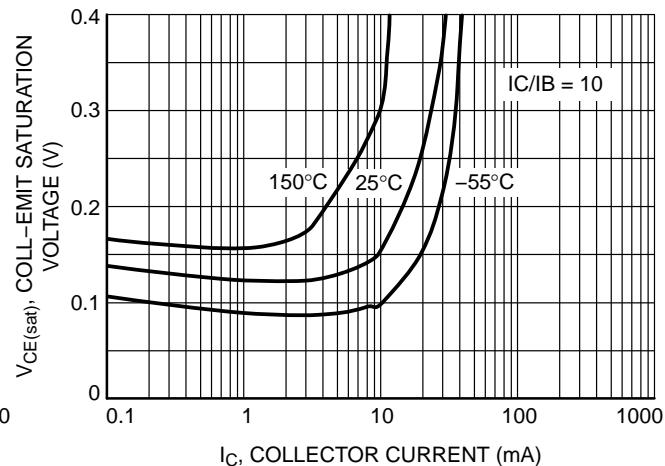


Figure 2. Collector-Emitter Saturation Voltage

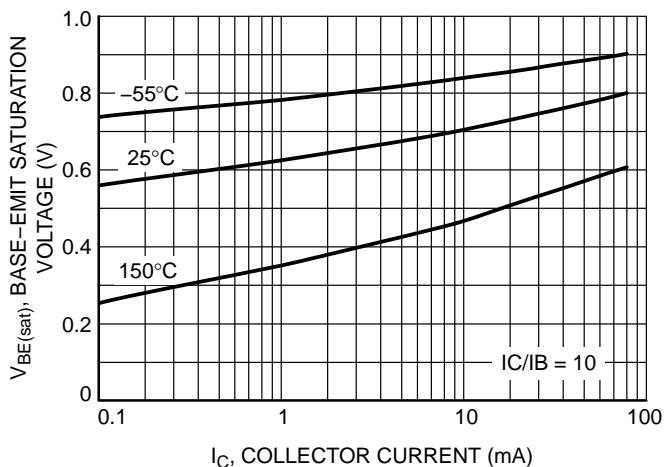


Figure 3. Base-Emitter Saturation Voltage

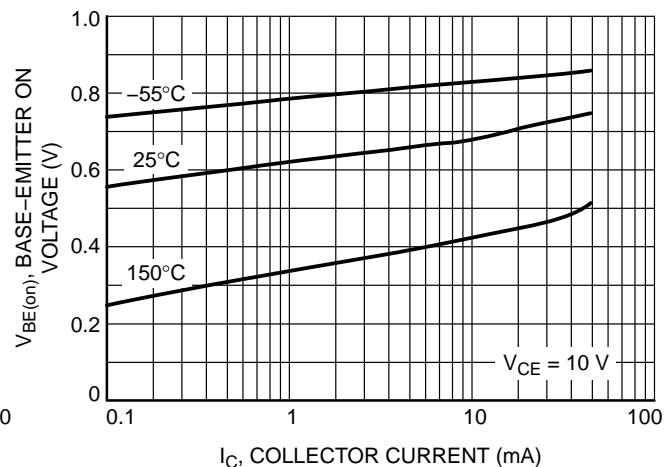


Figure 4. Base-Emitter "On" Voltage

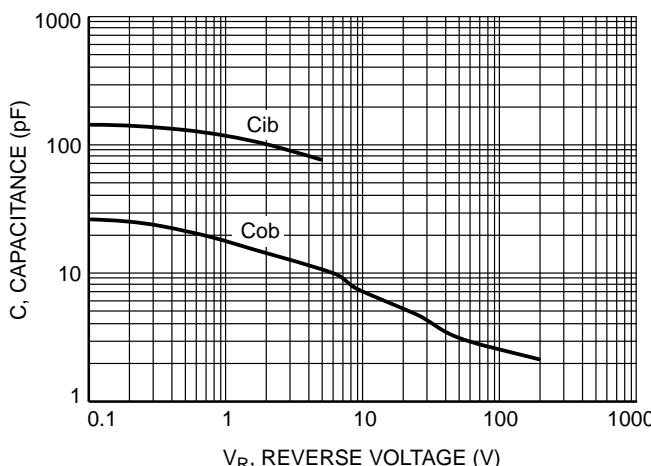


Figure 5. Capacitances

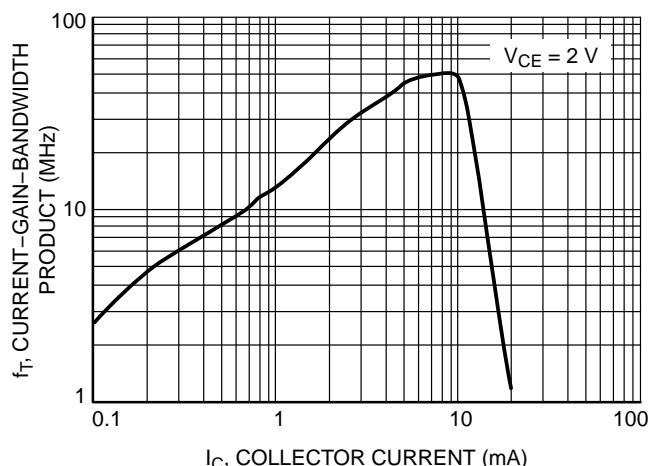


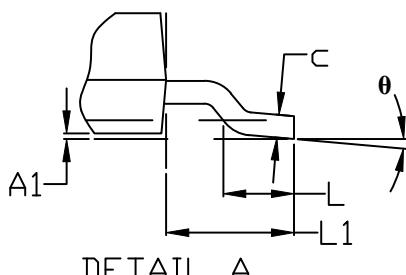
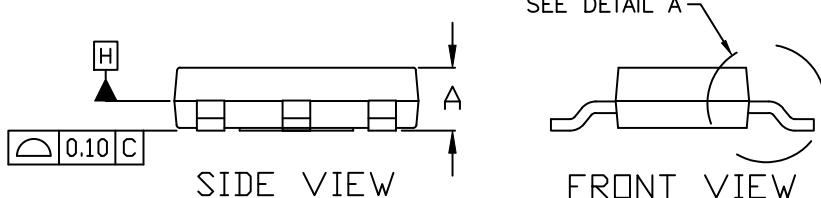
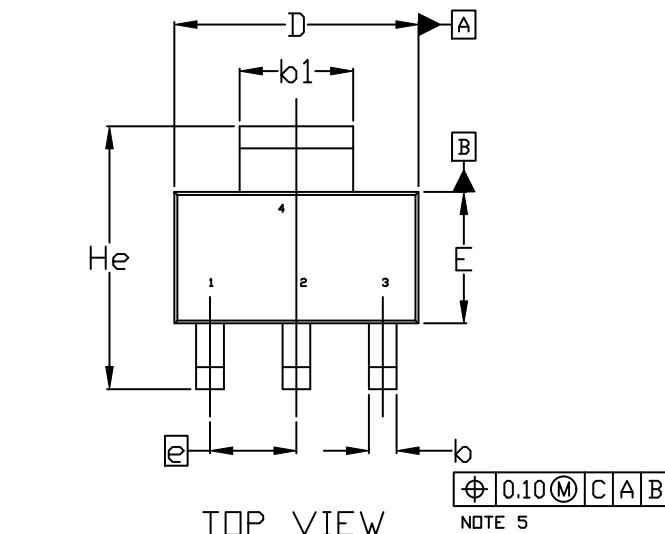
Figure 6. Current-Gain-Bandwidth Product



SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

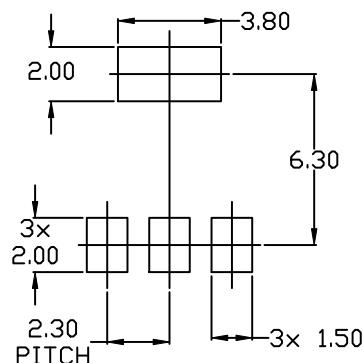
DATE 02 OCT 2018



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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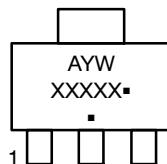
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. Emitter 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location

Y = Year

W = Work Week

XXXXX = Specific Device Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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