



# LV0221CS

CMOS IC

## Front Monitor OE-IC for Optical Pickups

ON Semiconductor®

http://onsemi.com

### Overview

The LV0221CS is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0221CS is small size and type CSP packages.

### Functions

- PIN photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-6dB to +6dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.

### Specifications

**Maximum Ratings** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}$		6	V
Allowable power dissipation	Pd1	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (about 80%), $T_a=75^\circ\text{C}$	136	mW
	Pd2	Glass epoxy one-side substrate 55mm × 45mm × 0.8mm Copper foil area (head: about 85% Tail: about 90%), $T_a=75^\circ\text{C}$	100	mW
Operating temperature	$T_{opr}$		-20 to +85	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-40 to +100	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

**Recommended Operating Conditions** at  $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	$V_{CC}$		4.5	5	5.5	V
Output load capacitance	$C_O$		12	20	33	pF
Output load resistance	$Z_O$		3			$\text{k}\Omega$

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## Electrical Characteristics at $T_a = 25^\circ\text{C}$ , $V_{CC} = 5\text{V}$ , $RL = 6\text{k}\Omega$ , $CL = 20\text{pF}$

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	$I_{CC}$			18	23.4	mA
Sleep current	$I_{S\text{lp}}$			1	mA	
Output voltage when shielded	$V_C$	At shielding	1.8	2.0	2.2	V
Output offset voltage	$V_{ofs}$	At shielding, voltage between VOP-VON	-30	0	30	mV
Temperature dependence of offset voltage *1	$V_{ofs}$	$T_a = -10$ to $+85^\circ\text{C}$	-60	0	60	$\mu\text{V}/^\circ\text{C}$
Optical output voltage *1	VLC	Low Gain, $\lambda = 780\text{nm}$ , $G = 0\text{dB}$	0.21	0.262	0.31	$\text{mV}/\mu\text{W}$
Voltage between VOP-VON	VLD	Low Gain, $\lambda = 650\text{nm}$ , $G = 0\text{dB}$	0.22	0.275	0.33	$\text{mV}/\mu\text{W}$
	VLB	Low Gain, $\lambda = 405\text{nm}$ , $G = 0\text{dB}$	0.14	0.172	0.21	$\text{mV}/\mu\text{W}$
	VMC	Middle Gain, $\lambda = 780\text{nm}$ , $G = 0\text{dB}$	0.66	0.83	0.99	$\text{mV}/\mu\text{W}$
	VMD	Middle Gain, $\lambda = 650\text{nm}$ , $G = 0\text{dB}$	0.70	0.87	1.05	$\text{mV}/\mu\text{W}$
	VMB	Middle Gain, $\lambda = 405\text{nm}$ , $G = 0\text{dB}$	0.43	0.54	0.65	$\text{mV}/\mu\text{W}$
	VHC	High Gain, $\lambda = 780\text{nm}$ , $G = 0\text{dB}$	1.97	2.46	2.95	$\text{mV}/\mu\text{W}$
	VHD	High Gain, $\lambda = 650\text{nm}$ , $G = 0\text{dB}$	2.07	2.58	3.10	$\text{mV}/\mu\text{W}$
	VHB	High Gain, $\lambda = 405\text{nm}$ , $G = 0\text{dB}$	1.29	1.62	1.94	$\text{mV}/\mu\text{W}$
Light output voltage adjustment range *1	G	G=0dB reference, absolute value of adjustment width	5.5	6.0	6.5	dB
D range *1	VoD	Voltage between VOP-VON	1700	2200		mV
Frequency characteristics *1, *2	FcC	-3dB(1MHz reference), $\lambda = 780\text{nm}$ Light input = $40\mu\text{W}(\text{DC}) + 20\mu\text{W}(\text{AC})$	50	75		MHz
	FcD	-3dB(1MHz reference), $\lambda = 650\text{nm}$ Light input = $40\mu\text{W}(\text{DC}) + 20\mu\text{W}(\text{AC})$	60	85		MHz
	FcB	-3dB(1MHz reference), $\lambda = 405\text{nm}$ Light input = $40\mu\text{W}(\text{DC}) + 20\mu\text{W}(\text{AC})$	60	85		MHz
Settling time *1	Tset			15		ns
Response time *1	Tr, Tf	$V_o = 0.9V_{\text{p-p}}$ , output level 10 to 90% $f_c = 10\text{MHz}$ , duty=50%			10	ns
Overshoot *1	Ovst	$V_o = 0.9V_{\text{p-p}}$			15	%
Undershoot *1	Unst	$V_o = 0.9V_{\text{p-p}}$			15	%
Linearity *1	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)	-1	0	1	%
Light-output voltage temperature dependence Voltage between VOP-VON *1, *3	TC	$\lambda = 780\text{nm}$ , $25^\circ\text{C}$ reference	10	13	16	%
	TD	$\lambda = 650\text{nm}$ , $25^\circ\text{C}$ reference	0	3	6	%
	TB	$\lambda = 405\text{nm}$ , $25^\circ\text{C}$ reference	0	3	6	%
Light-output voltage spectral sensitivity Voltage between VOP-VON *1	Vf	$\lambda = 785\text{nm} \pm 10\text{nm}$	-0.8		0.1	$\%/\text{nm}$
		$\lambda = 660\text{nm} \pm 10\text{nm}$	-0.4		0.4	$\%/\text{nm}$
		$\lambda = 405\text{nm} \pm 10\text{nm}$	0		1.2	$\%/\text{nm}$
Step-step voltage ratio *1	DG	$(V_n - V_{n-1}) / V_n \times 100 * 4$ Deviation from the ideal curve of above equation	-3	0	3	%

Item with \*1 mark indicate the design reference value.

Item with \*2 mark indicate the frequency characteristics when VOP and VON are applied individually.

The frequency characteristics are for the case of High / Middle / Low gain and for the case when the output voltage adjustment range is -6 to +6dB

Item with \*3 mark indicates the temperature dependence for the case of High / Middle / Low gain and for the case when the temperature is 25 to  $85^\circ\text{C}$  for the output voltage adjustment range of -6 to +6dB

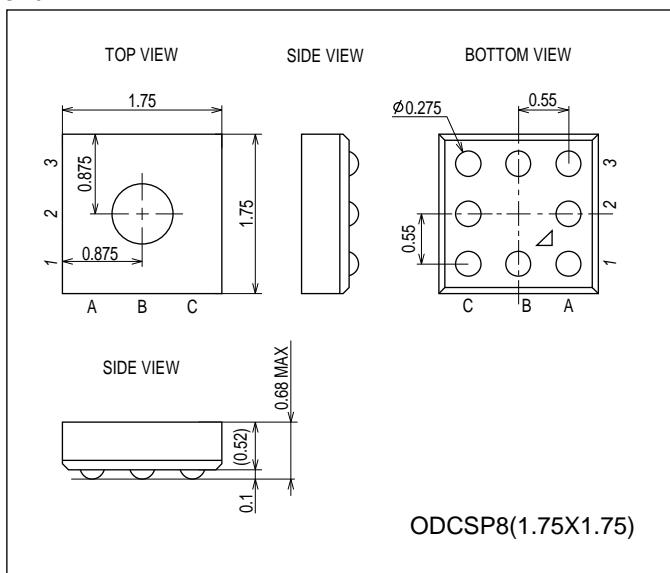
$V_n$  in Item with \*4 mark is  $V_n = (\text{sensitivity} / 2) \times 5400 / (5400-16 \times \text{GCAstep}) \times \text{light intensity} (\mu\text{W})$

GCA = Gain Control Amplifier

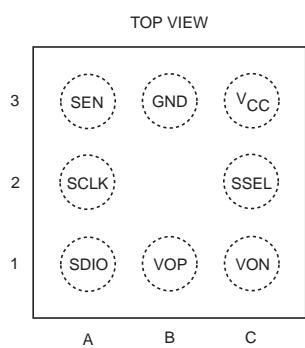
## Package Dimensions

unit : mm (typ)

3402

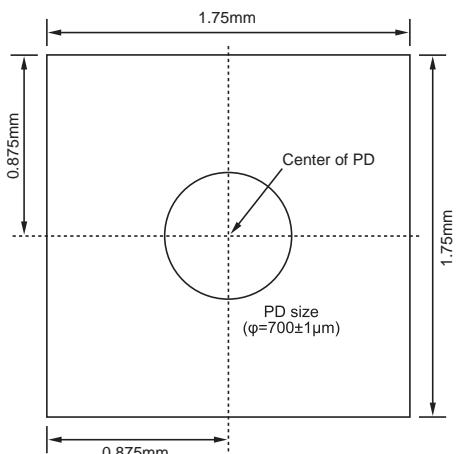


## Pin Assignment



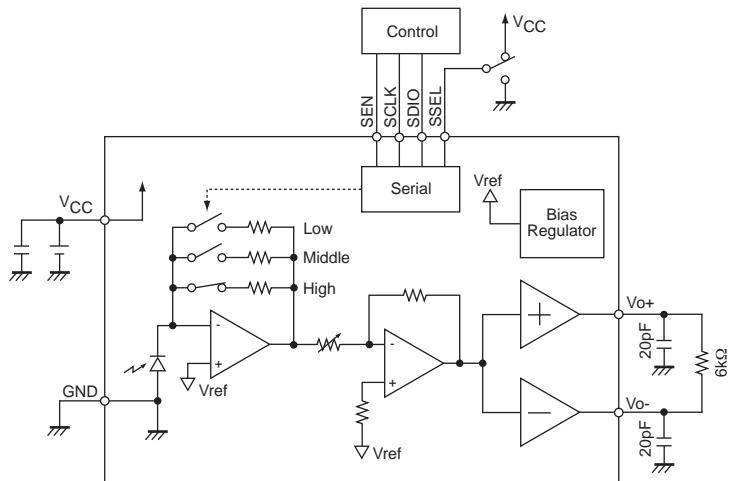
Pin No.	Pin name	Function
1A	SDIO	Serial communication Data pin
1B	VOP	Positive side output pin
1C	VON	Negative side output pin
2A	SCLK	Serial communication Clock pin
2C	SSEL	Register selection pin SSEL = Low, Open : Address 00 to 0Fh used SSEL = High : Address 10 to 1Fh used
3A	SEN	Serial communication Enable pin
3B	GND	GND pin
3C	V <sub>CC</sub>	Power supply voltage pin

## PD assignment



\*PD size for reference to be used for design

## Block diagram and Test circuit diagram



## Register table

Enable selection of the register group from the SSEL pin.

**SSEL = Low, Open**

	Address	7	6	5	4	3	2	1	0	
Name	00h	<b>POWER</b>			<b>IV GAIN SEL</b>			<b>GAIN SEL</b>		
Default		00			00			00		
Value		11: Power on 00 01 10: Sleep			00 01: High 10: Middle 11: Low			00 01: BD 10: DVD 11: CD		
<b>BD GAIN</b>										
Default	01h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
<b>DVD GAIN</b>										
Default	02h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
<b>CD GAIN</b>										
Default	03h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
Name	0Eh	<b>TEST1 (*1)</b>								
Name	0Fh	<b>TEST2 (*1)</b>								

**SSEL = High**

	Address	7	6	5	4	3	2	1	0	
Name	10h	<b>POWER</b>			<b>IV GAIN SEL</b>			<b>GAIN SEL</b>		
Default		00			00			00		
Value		11: Power on 00 01 10: Sleep			00 01: High 10: Middle 11: Low			00 01: BD 10: DVD 11: CD		
<b>BD GAIN</b>										
Default	11h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
<b>DVD GAIN</b>										
Default	12h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
<b>CD GAIN</b>										
Default	13h	1	1	1	1	1	1	1	1	
Value		00000000 to 11111111								
Name	1Eh	<b>TEST1 (*1)</b>								
Name	1Fh	<b>TEST2 (*1)</b>								

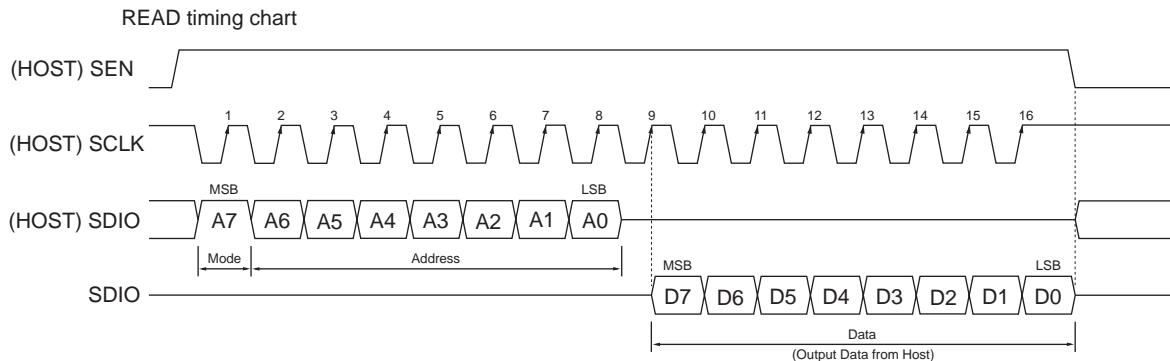
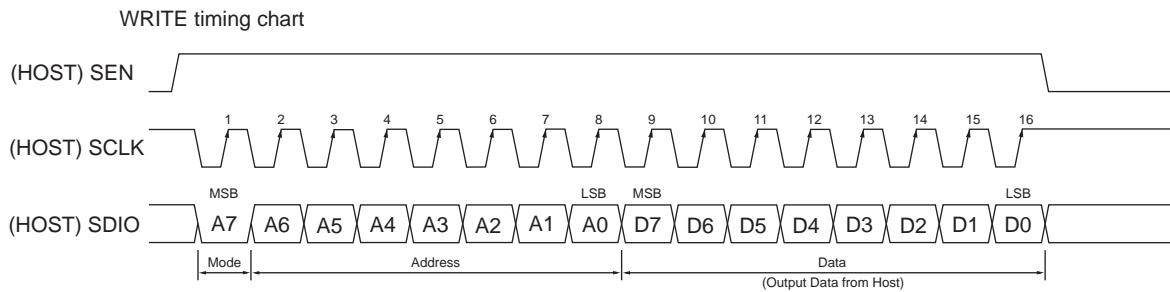
\*1 TEST1 and TEST2 are either the time when power is applied or “00000000” is set. Do not attempt to change “00000000” during operation.

“00000000” is returned when reading is made.

\*2 No problem in terms of operation occurs even when writing is made to the address 04h to 0Dh and 14h to 1Dh.

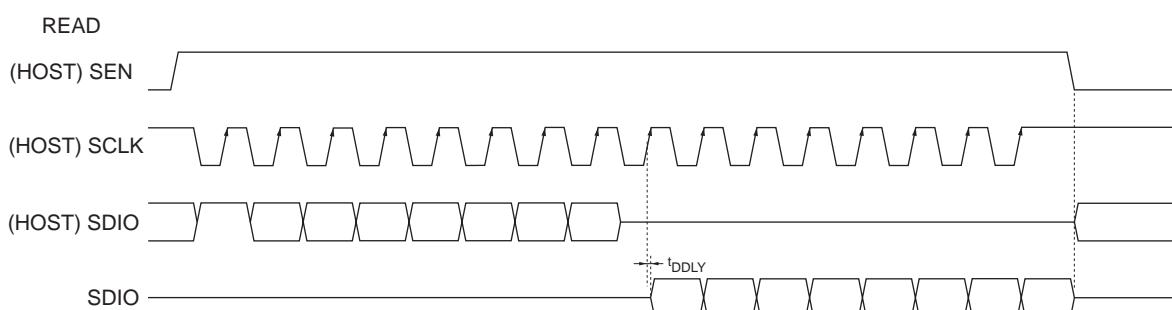
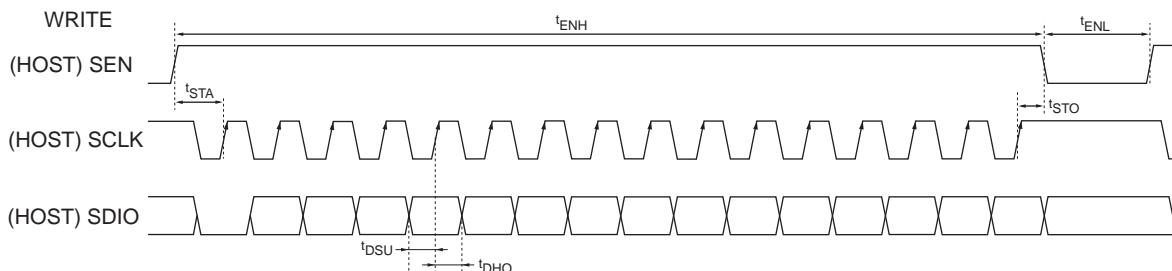
“00000000” is returned when this address is read.

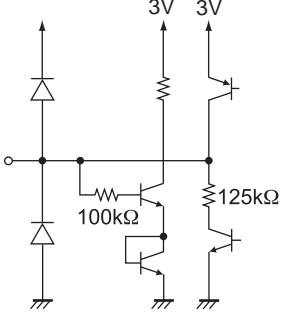
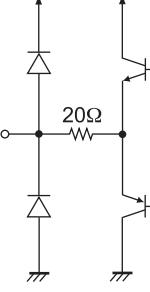
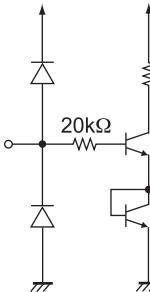
## Serial protocol



SDIO pin load / CL=20pF (The table below shows the design reference value.)

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency Write	$f_{SCL}$	0		10	MHz
SCL clock frequency Read	$f_{SCL}$	0		4	MHz
SDIO data setup time	$t_{DSU}$	50			ns
SDIO data hold time	$t_{DHO}$	50			ns
SDIO output delay	$t_{DDLY}$		10	80	ns
SEN "H" period	$t_{ENH}$	1.6			$\mu$ s
SEN "L" period	$t_{ENL}$	200			ns
SCL rise time after SEN rise	$t_{STA}$	60			ns
SEN fall time after final SCL rise	$t_{STO}$	100			ns
Serial input "H" voltage	$V_{IH}$	2.4			V
Serial input "L" voltage	$V_{IL}$			0.6	V
SDIO output "H" voltage	$V_{OH}$	2.5	2.9	3.3	V
SDIO output "L" voltage	$V_{OL}$	0	0.3	0.8	V



Pin	Type	Equivalent circuit diagram
SDIO	Input Output	
VOP VON	Output	
SCLK SSEL SEN	Input	

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