MOSFET – Power, Single N-Channel
80 V, 2.8 mΩ, 131.5 A
NVMJST2D6N08H

V$_{(BR)DSS}$	R$_{DS(ON)}$ MAX	I$_D$ MAX
80 V	2.8 mΩ @ 10 V	131.5 A

Features

- Small Footprint (5x7 mm) for Compact Design
- Low R$_{DS(on)}$ to Minimize Conduction Losses
- Low Q$_G$ and Capacitance to Minimize Driver Losses
- TCPAK57 Top Cool Package (TCPAK10)
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

D (6,7,8,9,10,TOP)

G (1)

S (2,3,4,5)

N−CHANNEL MOSFET

TCPAK10 5.1x7.5
CASE 760AG

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise noted)

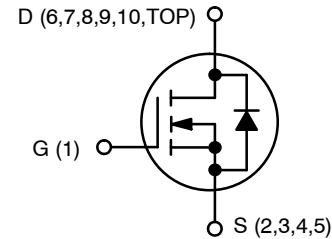| Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V$_{DSS}$	80	V
Gate−to−Source Voltage			V$_{GS}$	±20	V
Continuous Drain Current R$_{θJC}$ (Notes 1, 3)	Steady State	T$_C$ = 25°C	I$_D$	131.5	A
		T$_C$ = 100°C		93	
Power Dissipation R$_{θJC}$ (Note 1)		T$_C$ = 25°C	P$_D$	116	W
		T$_C$ = 100°C		58	
Continuous Drain Current R$_{θJA}$ (Notes 1, 2, 3)	Steady State	T$_A$ = 25°C	I$_D$	28	A
		T$_A$ = 100°C		20	
Power Dissipation R$_{θJA}$ (Notes 1, 2)		T$_A$ = 25°C	P$_D$	5.3	W
		T$_A$ = 100°C		2.6	
Pulsed Drain Current	T$_A$ = 25°C, t$_p$ = 10 μs		I$_{DM}$	900	A
Operating Junction and Storage Temperature Range			T$_J$, T$_{stg}$	−55 to +175	°C
Source Current (Body Diode)			I$_S$	97	A
Single Pulse Drain−to−Source Avalanche Energy (I$_{L(pk)}$ = 12.2 A)			E$_{AS}$	757	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T$_L$	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

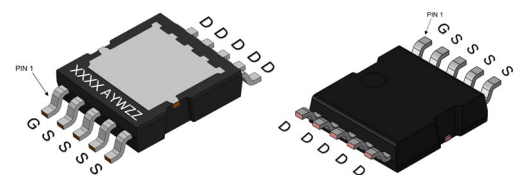### THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction−to−Case – Steady State	R$_{θJC}$	0.27	°C/W
Junction−to−Ambient – Steady State (Note 2)	R$_{θJA}$	28.5	
Junction−to−Drain Lead	Ψ$_{JL}$	4.72	
Junction−to−Source Lead	Ψ$_{JL}$	5.07	
Junction−to−Heatsink Top (Note 2)	Ψ$_{JH}$	1.29	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM

D D D D D

XXXX AYWZZ

PIN 1

G S S S S

XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMJST2D6N08H

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				3.84		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25 °C			10	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−7.16		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 50 A		2.2	2.8	mΩ
Forward Transconductance	g_{FS}	V_{DS} =5 V, I_D = 50 A			164		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 40 V			4405		pF
Output Capacitance	C_{OSS}				645		
Reverse Transfer Capacitance	C_{RSS}				25		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 64 V; I_D = 75 A			68		nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 10 V, V_{DS} = 64 V; I_D = 75 A			11		
Gate−to−Source Charge	Q_{GS}				18		
Gate−to−Drain Charge	Q_{GD}				16		
Plateau Voltage	V_{GP}				4.6		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 64 V, I_D = 75 A, R_G = 2.5 Ω			20		ns
Rise Time	t_r				26		
Turn−Off Delay Time	$t_{d(OFF)}$				42		
Fall Time	t_f				9.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.82	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			61		ns
Charge Time	t_a				36		
Discharge Time	t_b				25		
Reverse Recovery Charge	Q_{RR}				84		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
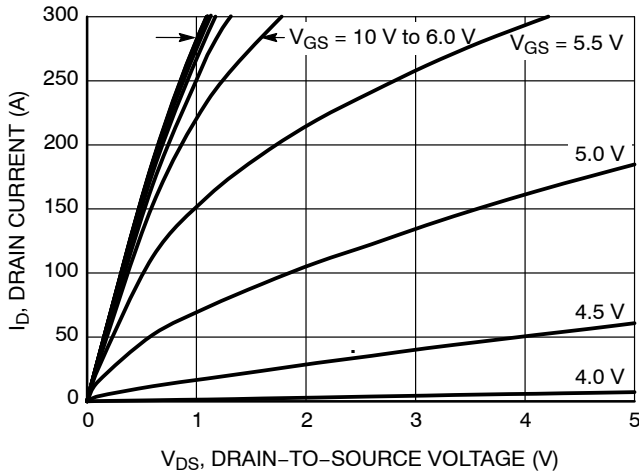
TYPICAL CHARACTERISTICS

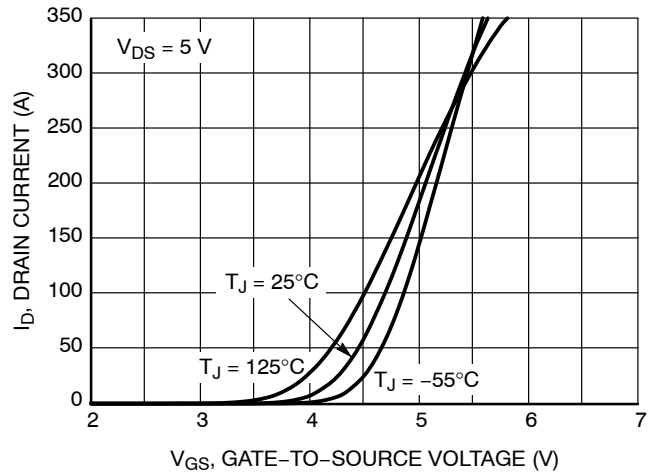**Figure 1. On−Region Characteristics**
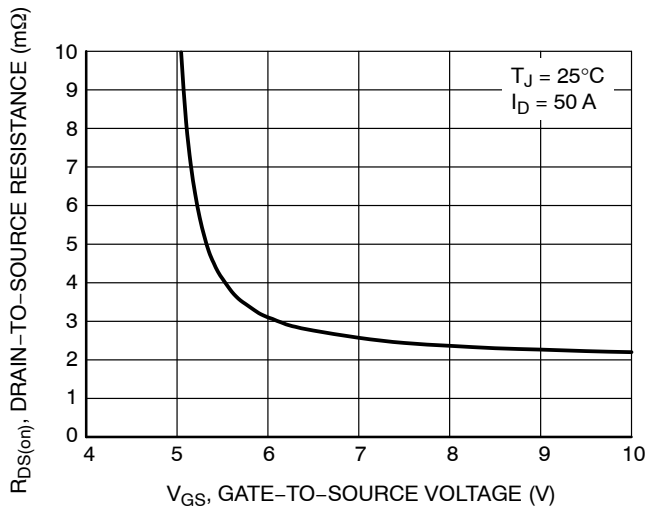

Figure 2. Transfer Characteristics

Figure 3. On−Resistance vs. Gate-to−Source Voltage
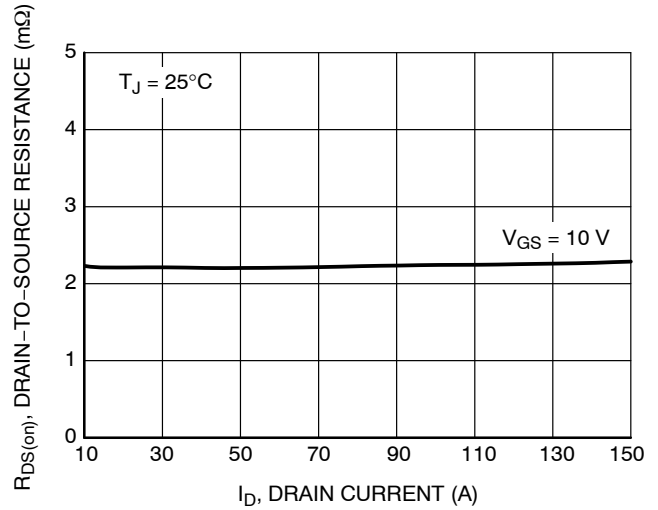

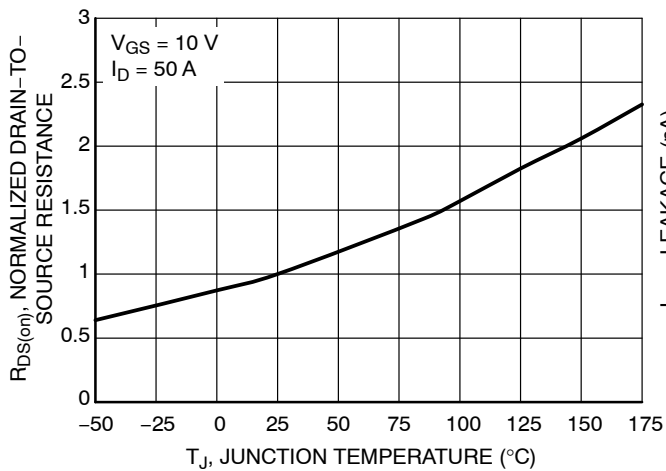**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

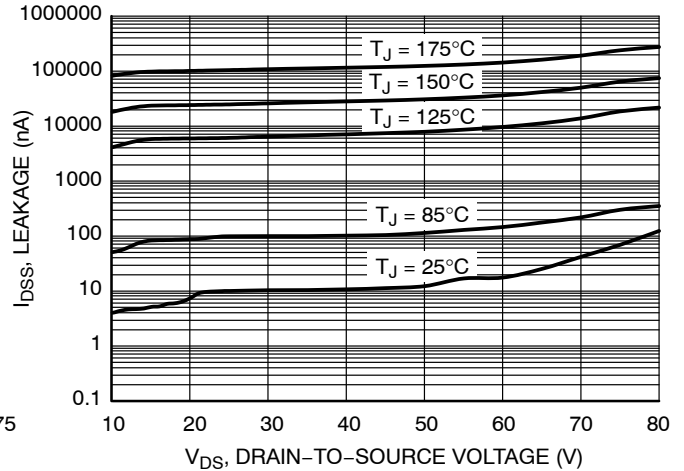**Figure 5. On−Resistance Variation with Temperature**

Figure 6. Drain−to−Source Leakage Current vs. Voltage
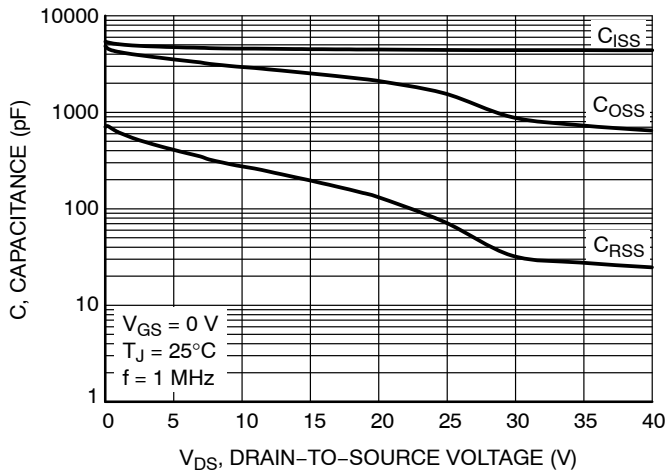
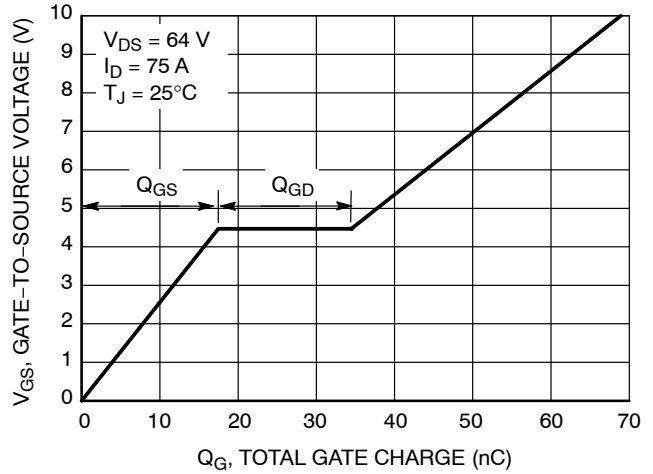## TYPICAL CHARACTERISTICS

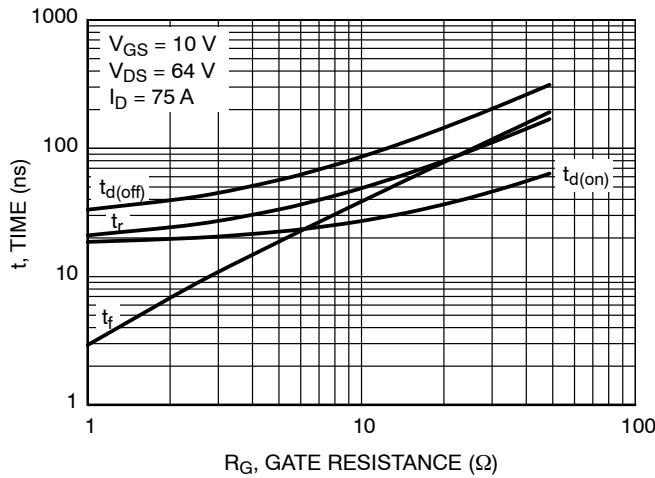**Figure 7. Capacitance Variation**

Figure 8. Gate−to−Source vs. Total Charge

Figure 9. Resistive Switching Time Variation vs. Gate Resistance
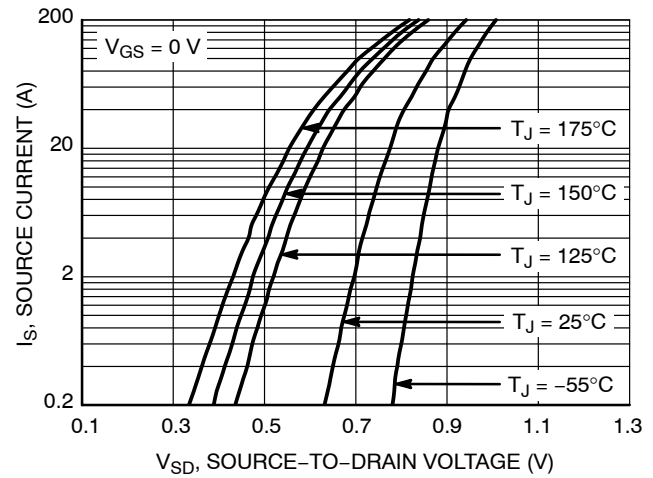
Figure 10. Diode Forward Voltage vs. Current
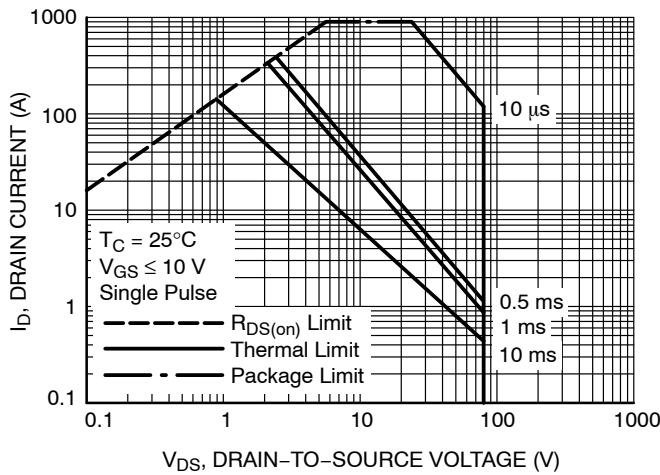
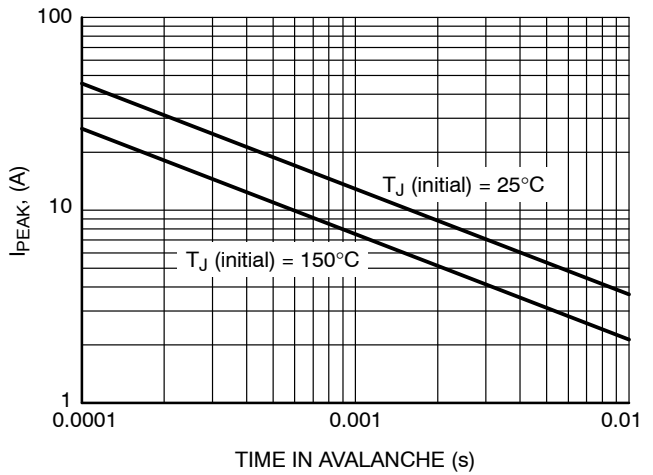**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

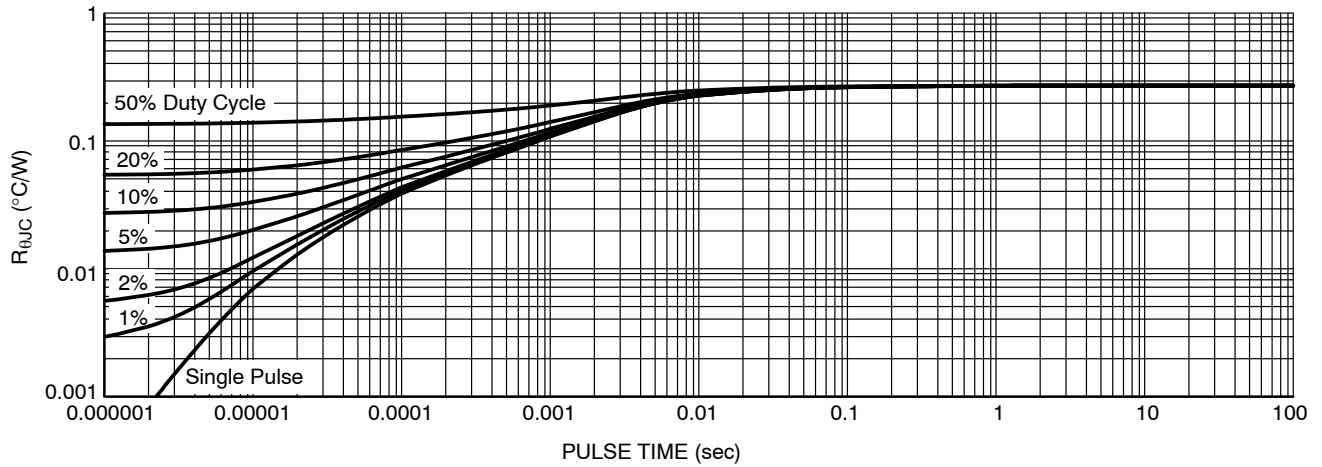**Figure 12. I_{PEAK} vs. Time in Avalanche**

TYPICAL CHARACTERISTICS

Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NVMJST2D6N08HTXG	2D68H	TCPAK10 5.1x7.5 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMJST2D6N08H

PACKAGE DIMENSIONS

TCPAK10 5.1x7.5, 1.0P
CASE 760AG
ISSUE D

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. UNIT DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.
6. LAND PAD UNDER THE PACKAGE BODY IS FOR MECHANICAL SUPPORT ONLY. SOLDER CONNECTION IS NOT REQUIRED.
7. DIMENSION A1 IS THE LEAD STAND-OFF FROM THE BOTTOM SURFACE OF THE PACKAGE BODY.

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.30	1.35	1.45
A1	-0.05	0.00	0.05
A2	1.30	1.35	1.40
b	0.36	0.41	0.46
c	0.16	0.21	0.26
D	5.00	5.10	5.20
D1	4.02	4.12	4.22
D2	0.30	0.40	0.50
D3	0.14 REF		
E	7.40	7.50	7.60
E1	5.20	5.30	5.40
E2	3.47	3.57	3.67
E3	0.30	0.40	0.50
E4	0.17 REF		
E5	4.82 REF		
e	1.00 BSC		
e1	0.50 BSC		
k	1.03 REF		
L	0.49	0.69	0.89
L1	0.90	1.10	1.30
L2	0.25 BSC		
Q	0.60	0.65	0.70
Θ	0°	2.5°	5°

TOP VIEW

SIDE VIEW

BOTTOM VIEW

LAND PAD RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DETAIL 'A'

NVMJST2D6N08H

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
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