NVMFS5A160PLZ

MOSFET – Power, Single P-Channel

-60 V, -100 A, 7.7 mΩ

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- NVMFS5A160PLZWF: Wettable Flank Option for Enhanced Optical Inspection
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

SPECIFICATION MAXIMUM RATINGS (T_J = 25°C unless otherwise noted) (Notes 1, 2, 3)

Symbol	Parameter			Value	Unit
V_{DSS}	Drain to Source Voltage			−60	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Continuous Drain, Current $R_{\theta JC}$, (Notes 1, 3)	Steady State	T_C = 25°C	−100	A
P_D	Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	200	W
I_D	Continuous Drain: Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	−15	A
P_D	Power Dissipation $R_{\theta JA}$ (Note 1, 2)		T_A = 25°C	3.8	W
I_{DP}	Pulsed Drain Current	PW ≤ 10 μs, duty cycle ≤ 1%		−400	A
T_J, T_{STG}	Operating Junction and Storage Temperature			−55 to +175	°C
I_S	Source Current (Body Diode)			−100	A
E_{AS}	Single Pulse Drain to Source Avalanche Energy (L= 1.0 mH, $I_{L(pk)}$ = −26 A)			335	mJ
T_L	Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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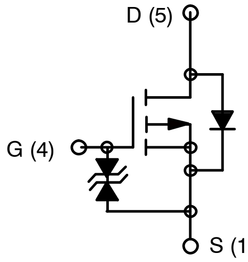
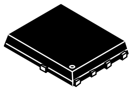
V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
−60 V	7.7 mΩ @ −10 V	−100 A
	10.5 mΩ @ −4.5 V	



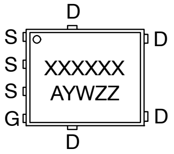
1 : Source
2 : Source
3 : Source
4 : Gate
5 : Drain

P-CHANNEL MOSFET



DFN5
(SO−8FL)

MARKING DIAGRAM



XXXXXX	= Specific Device Code 5A160L(NVMFS5A160PLZ) 160LWF(NVMFS5A160PLZWF)
A	= Assembly Location
Y	= Year
W	= Work Week
ZZ	= Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 7 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction to Case Steady State	0.75	°C/W
$R_{\theta JA}$	Junction to Ambient Steady State (Note 3)	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

July, 2019 − Rev. 0

Publication Order Number:
NVMFS5A160PLZ/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain to Source Breakdown Voltage	I_D = −1 mA, V_{GS} = 0 V		−60			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −60 V, V_{GS} = 0 V	T_J = 25°C			−1.0	μA
			T_J = 100°C (Note 4)			−100	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±16 V, V_{DS} = 0 V				±10	μA
ON CHARACTERISTICS (Note 5)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = −10 V, I_D = −1 mA		−1.2		−2.6	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = −10 V	I_D = −50 A		5.8	7.7	mΩ
		V_{GS} = −4.5 V	I_D = −50 A		7.3	10.5	
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −50 A			119		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{iss}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz V_{DS} = −20 V,			7700		pF
C_{oss}	Output Capacitance				720		
C_{rss}	Reverse Transfer Capacitance				540		
$Q_{g(tot)}$	Total Gate Charge	V_{GS} = −10 V, I_D = −50 A V_{DS} = −36 V,			160		nC
Q_{gs}	Gate to Source Charge				24		
Q_{gd}	Gate to Drain Charge				45		
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(on)}$	Turn-On Delay Time	V_{DS} = −36 V, I_D = −50 A, V_{GS} = −10 V, R_G = 50 Ω			50		ns
t_r	Rise Time				690		
$t_{d(off)}$	Turn-Off Delay Time				645		
t_f	Fall Time				643		
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = −50 A			−0.83	−1.5	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = −50 A di/dt = 100 A/μs			93		ns
Q_{rr}	Reverse Recovery Charge				218		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at T_J = 100 °C. Product is not tested to this condition in production.
5. Pulse Test: pulse width ≤ 300μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

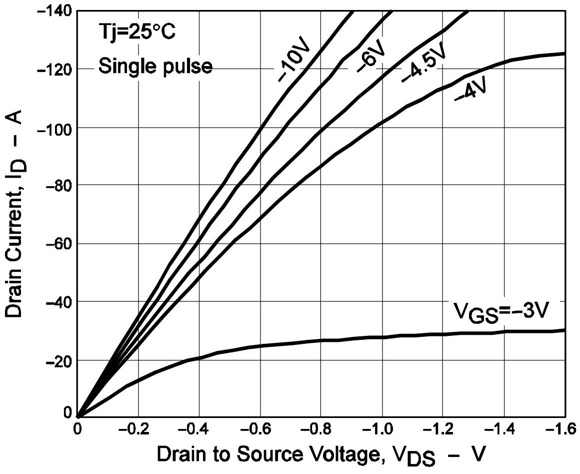


Figure 1. I_D – V_{DS}

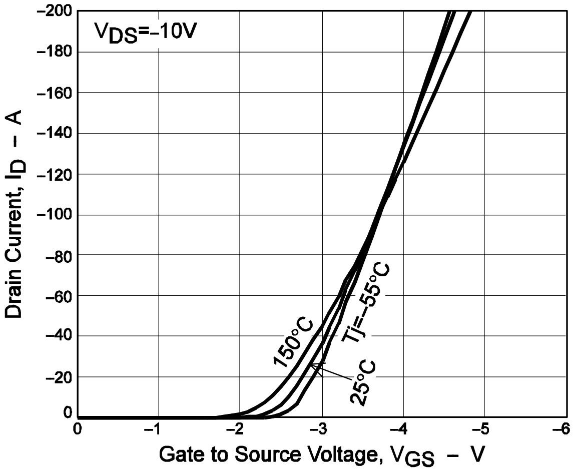


Figure 2. I_D – V_{GS}

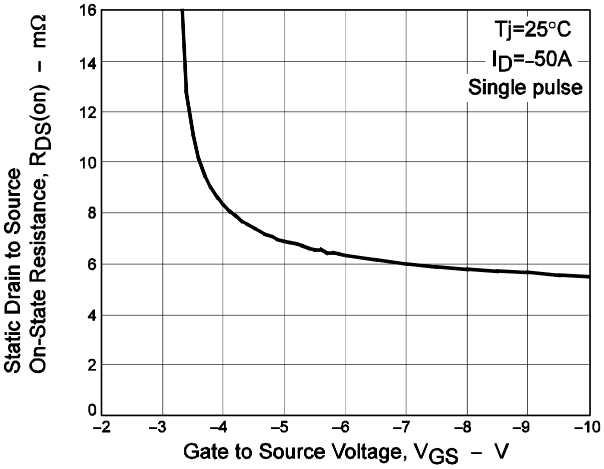


Figure 3. $R_{DS(on)}$ – V_{GS}

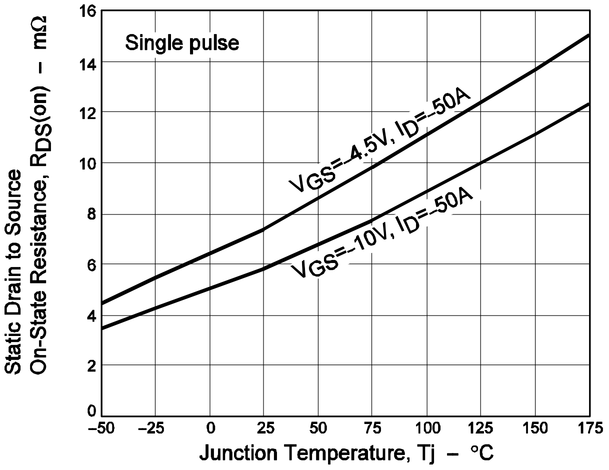


Figure 4. $R_{DS(on)}$ – T_J

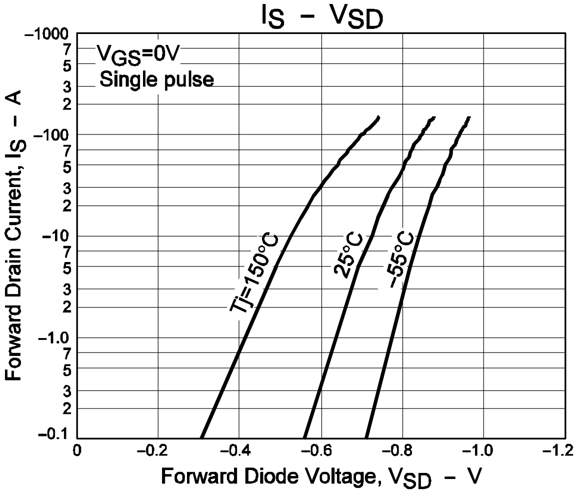


Figure 5. I_S – V_{SD}

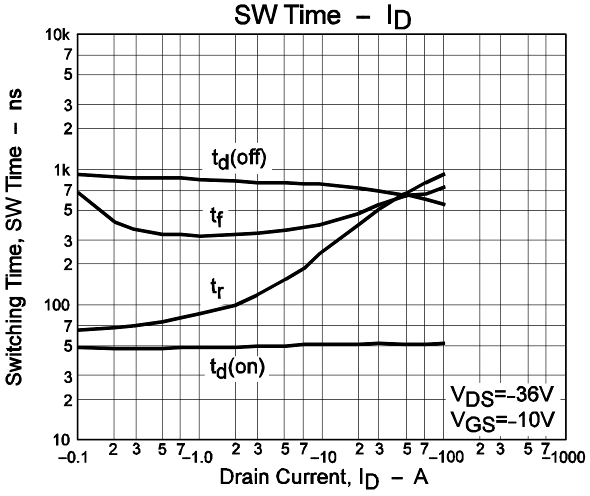


Figure 6. SW Time – I_D

TYPICAL CHARACTERISTICS

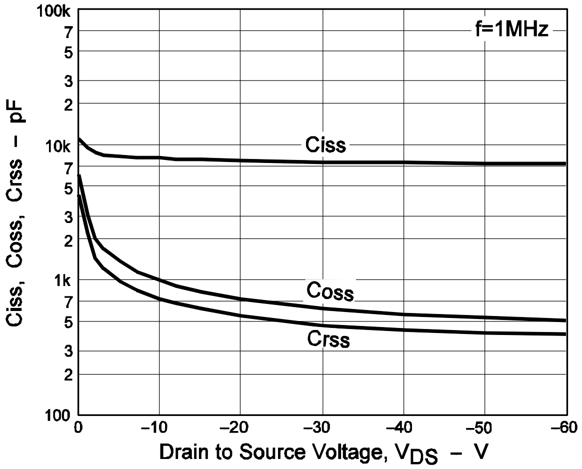


Figure 7. Ciss, Coss, Crss – V_{DS}

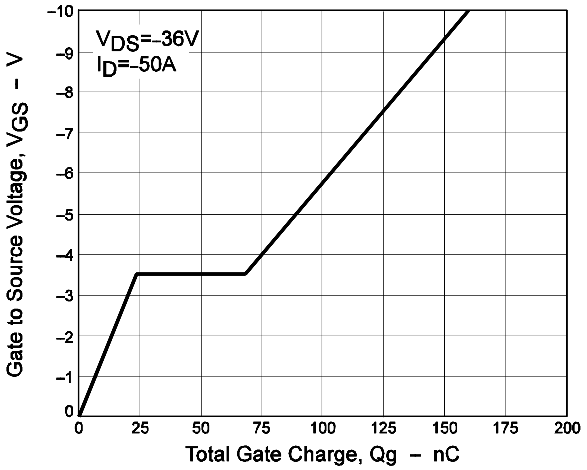


Figure 8. V_{GS} – Qg

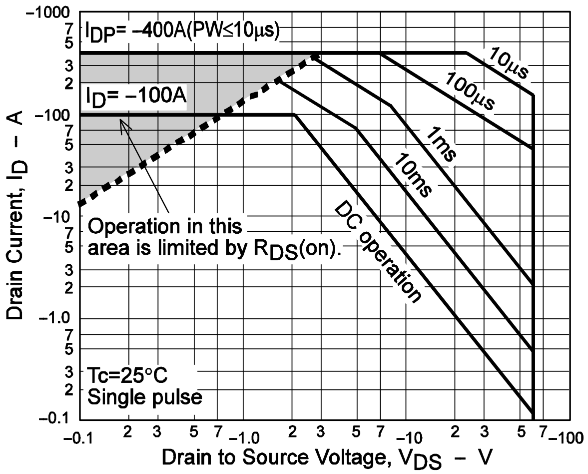


Figure 9. SOA

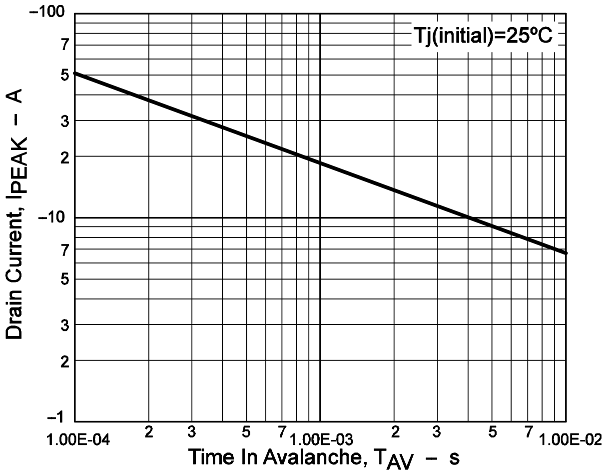


Figure 10. I_{PEAK} – T_{AV}

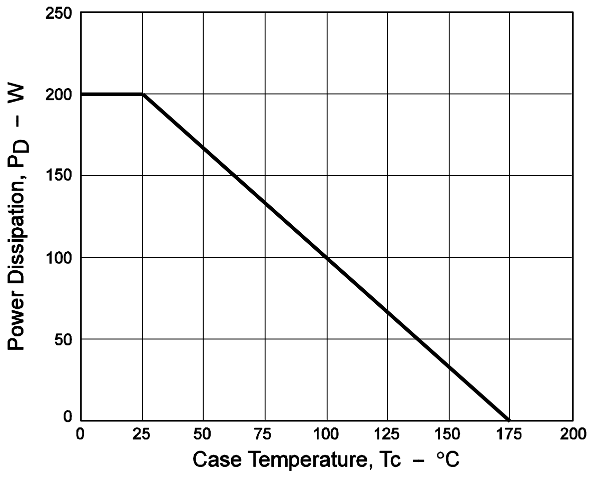


Figure 11. P_D – T_C

TYPICAL CHARACTERISTICS

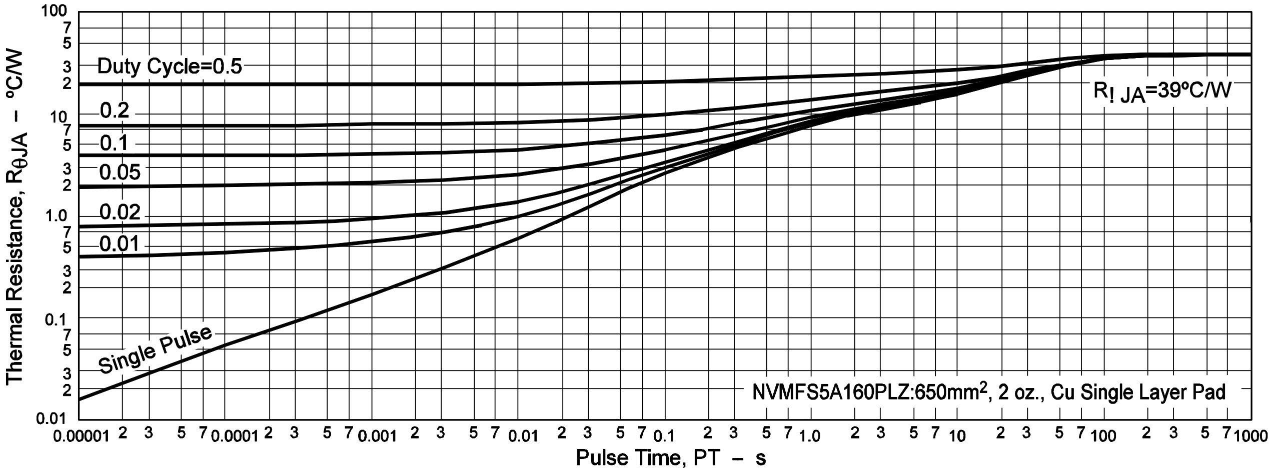


Figure 12. $R_{\theta JA}$ – Pulse Time

ORDERING INFORMATION

Device	Marking	Package	Shipping (Qty / Packing)†
NVMFS5A160PLZT1G	5A160L	DFN5 5x6, 1.27P (SO−8FL) (Pb-Free)	1.500 / Tape & Reel
NVMFS5A160PLZWFT1G	160LWF	DFN5 5x6, 1.27P (SO−8FL) (Pb-Free, Wettable Flanks)	1.500 / Tape & Reel
NVMFS5A160PLZT3G	5A160L	DFN5 5x6, 1.27P (SO−8FL) (Pb-Free)	5.000 / Tape & Reel
NVMFS5A160PLZWFT3G	160LWF	DFN5 5x6, 1.27P (SO−8FL) (Pb-Free, Wettable Flanks)	5.000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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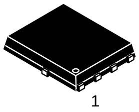


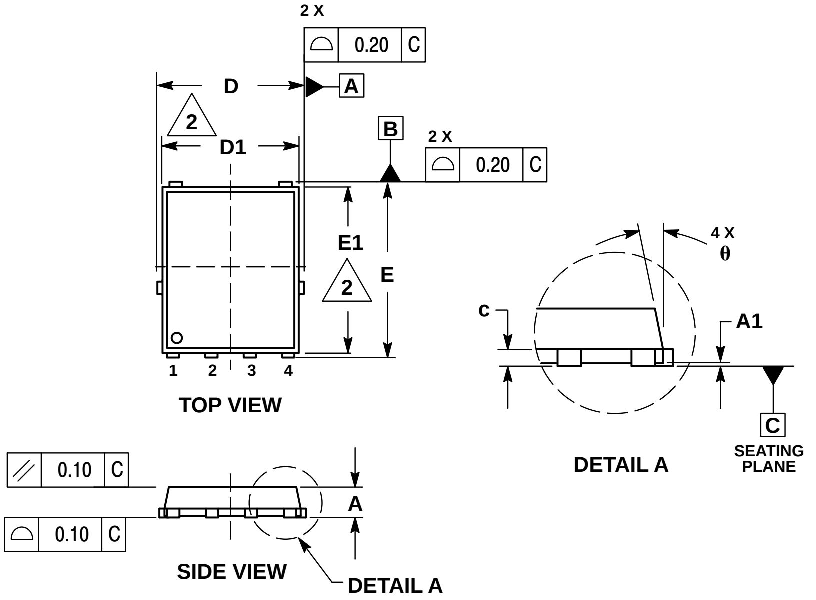
SCALE 2:1

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

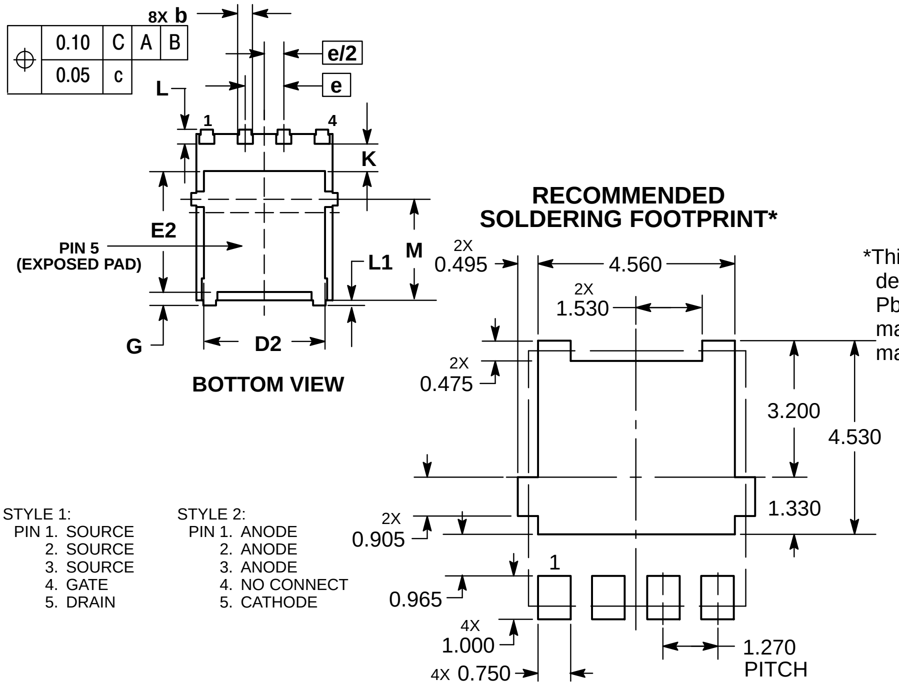
DIM	MILLIMETERS MIN	MILLIMETERS NOM	MILLIMETERS MAX
A	0.90	1.00	1.10
A1	0.00	−−−	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	−−−	12 °



TOP VIEW

DETAIL A

SIDE VIEW



BOTTOM VIEW

RECOMMENDED SOLDERING FOOTPRINT*

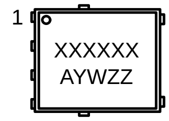
DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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