

NUP2301MW6T1G, SZNUP2301MW6T1G

Low Capacitance Diode Array for ESD Protection in Two Data Lines

NUP2301MW6T1G is a micro-integrated device designed to provide protection for sensitive components from possible harmful electrical transients; for example, ESD (electrostatic discharge).

Features

- Low Capacitance (2.0 pf Maximum Between I/O Lines)
- Single Package Integration Design
- Provides ESD Protection for JEDEC Standards JESD22
Machine Model = Class C
Human Body Model = Class 3B
- Protection for IEC61000-4-2 (Level 4)
8.0 kV (Contact)
15 kV (Air)
- Ensures Data Line Speed and Integrity
- Fewer Components and Less Board Space
- Direct the Transient to Either Positive Side or to the Ground
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device*

Applications

- T1/E1 Secondary IC Protection
- T3/E3 Secondary IC Protection
- HDSL, IDSL Secondary IC Protection
- Video Line Protection
- Microcontroller Input Protection
- Base Stations
- I²C Bus Protection



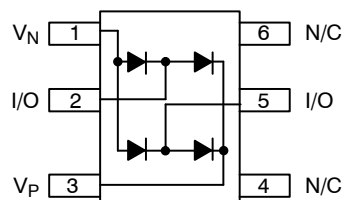
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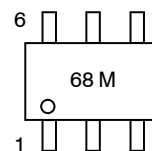


SC-88
CASE 419B
STYLE 23

PIN CONFIGURATION AND SCHEMATIC



MARKING DIAGRAM



68 = Specific Device Code
M = Date Code

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|--------------------|------------------------|
| NUP2301MW6T1G | SC-88 (Pb-Free) | 3,000 / Tape & Reel |
| SZNUP2301MW6T1G | SC-88 (Pb-Free) | 3,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAXIMUM RATINGS (Each Diode) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|-----------------|-------------------|------|
| Reverse Voltage | V_R | 70 | Vdc |
| Forward Current | I_F | 200 | mAdc |
| Peak Forward Surge Current | $I_{FM(surge)}$ | 500 | mAdc |
| Repetitive Peak Reverse Voltage | V_{RRM} | 70 | V |
| Average Rectified Forward Current (Note 1) (Averaged over any 20 ms Period) | $I_{F(AV)}$ | 715 | mA |
| Repetitive Peak Forward Current | I_{FRM} | 450 | mA |
| Non-Repetitive Peak Forward Current $t = 1.0 \mu\text{s}$ $t = 1.0 \text{ ms}$ $t = 1.0 \text{ S}$ | I_{FSM} | 2.0 1.0 0.5 | A |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $FR-5 = 1.0 \times 0.75 \times 0.062 \text{ in.}$

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|--|-----------------|-------------|--------------------|
| Thermal Resistance Junction-to-Ambient | $R_{\theta JA}$ | 625 | $^\circ\text{C/W}$ |
| Lead Solder Temperature Maximum 10 Seconds Duration | T_L | 260 | $^\circ\text{C}$ |
| Junction Temperature | T_J | -55 to +150 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to +150 | $^\circ\text{C}$ |

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (Each Diode)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|----------------|--------|-----|-----|-----|------|
|----------------|--------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | |
|---|------------|------------------|------------------|----------------------------|-----------------|
| Reverse Breakdown Voltage ($I_{(BR)} = 100 \mu\text{A}$) | $V_{(BR)}$ | 70 | – | – | Vdc |
| Reverse Voltage Leakage Current ($V_R = 70 \text{ Vdc}$) ($V_R = 25 \text{ Vdc}$, $T_J = 150^\circ\text{C}$) ($V_R = 70 \text{ Vdc}$, $T_J = 150^\circ\text{C}$) | I_R | – – – | – – – | 2.5 30 50 | μAdc |
| Capacitance (between I/O pins) ($V_R = 0 \text{ V}$, $f = 1.0 \text{ MHz}$) | C_D | – | 1.0 | 2.0 | pF |
| Capacitance (between I/O pin and ground) ($V_R = 0 \text{ V}$, $f = 1.0 \text{ MHz}$) | C_D | – | 1.6 | 3 | pF |
| Forward Voltage ($I_F = 1.0 \text{ mAdc}$) ($I_F = 10 \text{ mAdc}$) ($I_F = 50 \text{ mAdc}$) ($I_F = 150 \text{ mAdc}$) | V_F | – – – – | – – – – | 715 855 1000 1250 | mVdc |

2. $FR-5 = 1.0 \times 0.75 \times 0.062 \text{ in.}$

3. Alumina = $0.4 \times 0.3 \times 0.024 \text{ in.}$ 99.5% alumina.

4. Include SZ-prefix devices where applicable.

NUP2301MW6T1G, SZNUP2301MW6T1G

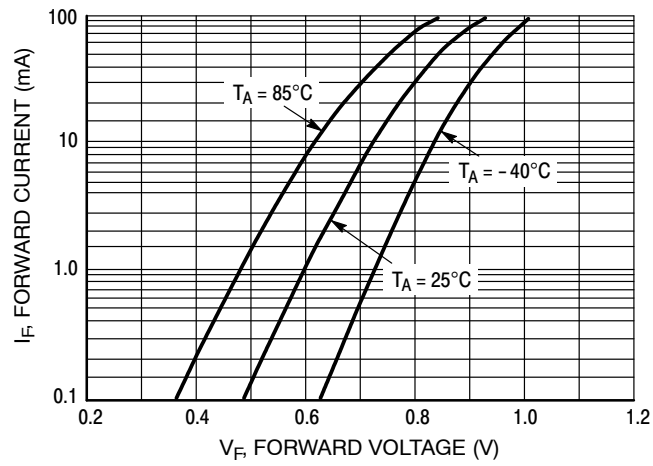


Figure 1. Forward Voltage

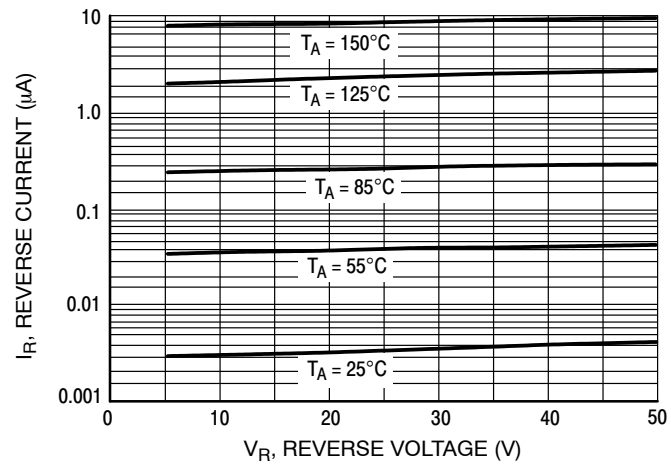


Figure 2. Leakage Current

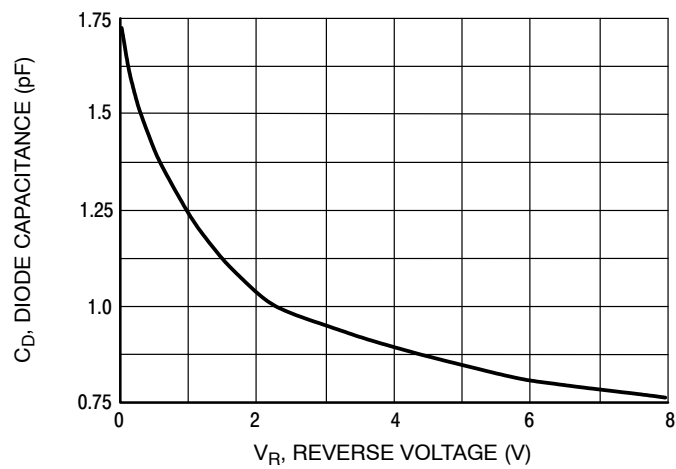


Figure 3. Capacitance

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

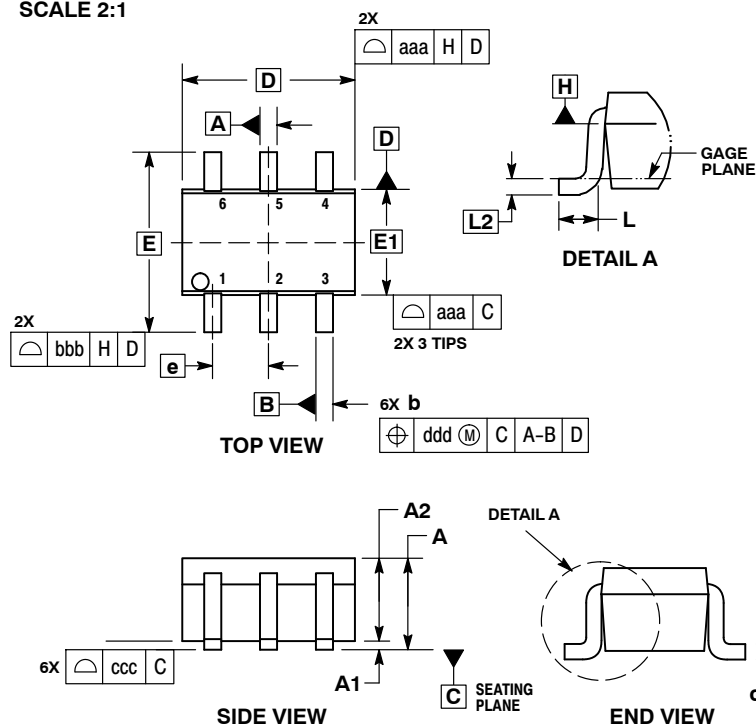
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SCALE 2:1

SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

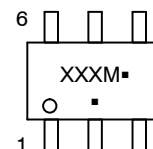
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- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
 4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
 5. DATUMS A AND B ARE DETERMINED AT DATUM H.
 6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
 7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

| DIM | MILLIMETERS | | | INCHES | | |
|-----|-------------|------|------|-----------|-------|-------|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | --- | --- | 1.10 | --- | --- | 0.043 |
| A1 | 0.00 | --- | 0.10 | 0.000 | --- | 0.004 |
| A2 | 0.70 | 0.90 | 1.00 | 0.027 | 0.035 | 0.039 |
| b | 0.15 | 0.20 | 0.25 | 0.006 | 0.008 | 0.010 |
| C | 0.08 | 0.15 | 0.22 | 0.003 | 0.006 | 0.009 |
| D | 1.80 | 2.00 | 2.20 | 0.070 | 0.078 | 0.086 |
| E | 2.00 | 2.10 | 2.20 | 0.078 | 0.082 | 0.086 |
| E1 | 1.15 | 1.25 | 1.35 | 0.045 | 0.049 | 0.053 |
| e | 0.65 BSC | | | 0.026 BSC | | |
| L | 0.26 | 0.36 | 0.46 | 0.010 | 0.014 | 0.018 |
| L2 | 0.15 BSC | | | 0.006 BSC | | |
| aaa | 0.15 | | | 0.006 | | |
| bbb | 0.30 | | | 0.012 | | |
| ccc | 0.10 | | | 0.004 | | |
| ddd | 0.10 | | | 0.004 | | |

GENERIC MARKING DIAGRAM*



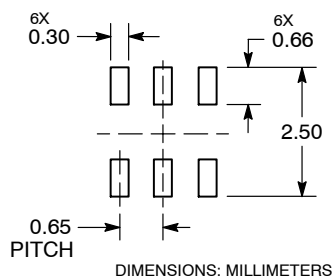
XXX = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SC-88/SC70-6/SOT-363
CASE 419B-02
ISSUE Y

DATE 11 DEC 2012

| | | | | | |
|--|--|---|---|---|---|
| STYLE 1: PIN 1. EMITTER 2 2. BASE 2 3. COLLECTOR 1 4. EMITTER 1 5. BASE 1 6. COLLECTOR 2 | STYLE 2: CANCELLED | STYLE 3: CANCELLED | STYLE 4: PIN 1. CATHODE 2. CATHODE 3. COLLECTOR 4. EMITTER 5. BASE 6. ANODE | STYLE 5: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 6: PIN 1. ANODE 2 2. N/C 3. CATHODE 1 4. ANODE 1 5. N/C 6. CATHODE 2 |
| STYLE 7: PIN 1. SOURCE 2 2. DRAIN 2 3. GATE 1 4. SOURCE 1 5. DRAIN 1 6. GATE 2 | STYLE 8: CANCELLED | STYLE 9: PIN 1. EMITTER 2 2. EMITTER 1 3. COLLECTOR 1 4. BASE 1 5. BASE 2 6. COLLECTOR 2 | STYLE 10: PIN 1. SOURCE 2 2. SOURCE 1 3. GATE 1 4. DRAIN 1 5. DRAIN 2 6. GATE 2 | STYLE 11: PIN 1. CATHODE 2 2. CATHODE 2 3. ANODE 1 4. CATHODE 1 5. CATHODE 1 6. ANODE 2 | STYLE 12: PIN 1. ANODE 2 2. ANODE 2 3. CATHODE 1 4. ANODE 1 5. ANODE 1 6. CATHODE 2 |
| STYLE 13: PIN 1. ANODE 2. N/C 3. COLLECTOR 4. EMITTER 5. BASE 6. CATHODE | STYLE 14: PIN 1. VREF 2. GND 3. GND 4. IOUT 5. VEN 6. VCC | STYLE 15: PIN 1. ANODE 1 2. ANODE 2 3. ANODE 3 4. CATHODE 3 5. CATHODE 2 6. CATHODE 1 | STYLE 16: PIN 1. BASE 1 2. EMITTER 2 3. COLLECTOR 2 4. BASE 2 5. EMITTER 1 6. COLLECTOR 1 | STYLE 17: PIN 1. BASE 1 2. EMITTER 1 3. COLLECTOR 2 4. BASE 2 5. EMITTER 2 6. COLLECTOR 1 | STYLE 18: PIN 1. VIN1 2. VCC 3. VOUT2 4. VIN2 5. GND 6. VOUT1 |
| STYLE 19: PIN 1. IOUT 2. GND 3. GND 4. V CC 5. V EN 6. V REF | STYLE 20: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR | STYLE 21: PIN 1. ANODE 1 2. N/C 3. ANODE 2 4. CATHODE 2 5. N/C 6. CATHODE 1 | STYLE 22: PIN 1. D1 (i) 2. GND 3. D2 (i) 4. D2 (c) 5. VBUS 6. D1 (c) | STYLE 23: PIN 1. Vn 2. CH1 3. Vp 4. N/C 5. CH2 6. N/C | STYLE 24: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE |
| STYLE 25: PIN 1. BASE 1 2. CATHODE 3. COLLECTOR 2 4. BASE 2 5. EMITTER 6. COLLECTOR 1 | STYLE 26: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1 | STYLE 27: PIN 1. BASE 2 2. BASE 1 3. COLLECTOR 1 4. EMITTER 1 5. EMITTER 2 6. COLLECTOR 2 | STYLE 28: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN | STYLE 29: PIN 1. ANODE 2. ANODE 3. COLLECTOR 4. EMITTER 5. BASE/ANODE 6. CATHODE | STYLE 30: PIN 1. SOURCE 1 2. DRAIN 2 3. DRAIN 2 4. SOURCE 2 5. GATE 1 6. DRAIN 1 |

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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