

# MOSFET - Power, DUAL COOL<sup>®</sup> N-Channel, PQFN8 150 V, 11.4 mΩ, 80 A NTMFSC012N15MC

## Features

- Advanced Dual-sided Cooled Packaging
- Ultra Low  $R_{DS(on)}$
- MSL1 Robust Packaging Design

## Typical Applications

- Primary DC-DC FET
- Synchronous Rectifier
- DC-DC Conversion

## MAXIMUM RATINGS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	150	V
Gate-to-Source Voltage			$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	$T_C = 25^{\circ}\text{C}$	$I_D$	80	A
		$T_C = 100^{\circ}\text{C}$		50	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^{\circ}\text{C}$	$P_D$	147	W
		$T_C = 100^{\circ}\text{C}$		58	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25^{\circ}\text{C}$	$I_D$	10	A
		$T_A = 100^{\circ}\text{C}$		6	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^{\circ}\text{C}$	$P_D$	2.7	W
		$T_A = 100^{\circ}\text{C}$		1	
Pulsed Drain Current	$T_C = 25^{\circ}\text{C}$ , $t_p = 10 \mu\text{s}$	$I_{DM}$	1067	A	
Operating Junction / Storage Temperature Max			$T_J$ , $T_{stg}$	+150	$^{\circ}\text{C}$
Source Current (Body Diode)			$I_S$	122	A
Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 35 \text{ A}$ )			$E_{AS}$	161	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			$T_L$	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

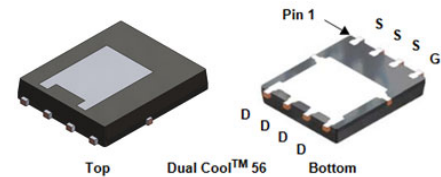
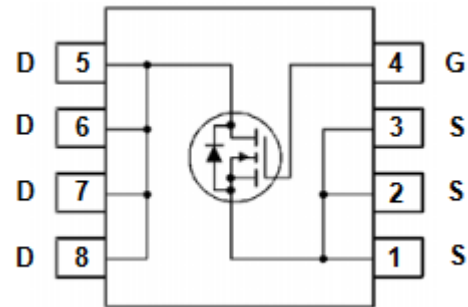
## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	0.85	$^{\circ}\text{C}/\text{W}$
Junction-to-Case Top - Steady State	$R_{\theta JT}$	1.5	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	46	

- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
- Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
- Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

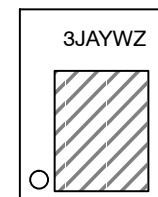
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	11.4 mΩ @ 10 V	44 A
	14.5 mΩ @ 8 V	22 A

## N-CHANNEL MOSFET



DFN8 5x6.15  
CASE 506EG

## MARKING DIAGRAM



- 3J = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
Z = Assembly Lot Code

## ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTMFSC012N15MC	PQFN8 (Pb-Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# NTMFSC012N15MC

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	150			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		6.9		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 150\text{ V}$	$T_J = 25^\circ\text{C}$		1	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 194\text{ }\mu\text{A}$	2.5		4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 194\text{ }\mu\text{A}$ , ref to $25^\circ\text{C}$		8		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 44\text{ A}$		8.9	11.4	m $\Omega$
		$V_{GS} = 8\text{ V}, I_D = 22\text{ A}$		9.5	14.5	
Gate-Resistance	$R_G$	$T_A = 25^\circ\text{C}$		0.7		$\Omega$

### CHARGES & CAPACITANCES

Input Capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 75\text{ V}$		2490		pF
Output Capacitance	$C_{OSS}$			676		
Reverse Transfer Capacitance	$C_{RSS}$			9.0		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 75\text{ V}, I_D = 44\text{ A}$		20.4		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 44\text{ A}$		32.4		
Gate-to-Source Charge	$Q_{GS}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 44\text{ A}$		13.9		
Gate-to-Drain Charge	$Q_{GD}$			5.5		
Plateau Voltage	$V_{GP}$			5.7		V

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 75\text{ V}, I_D = 44\text{ A}, R_G = 2.5\text{ }\Omega$		18.4		ns
Rise Time	$t_r$			3.7		
Turn-Off Delay Time	$t_{d(OFF)}$			21.3		
Fall Time	$t_f$			3		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V}, I_S = 44\text{ A}$	$T_J = 25^\circ\text{C}$		0.88	V
			$T_J = 125^\circ\text{C}$		0.76	
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 44\text{ A}$		42.7		ns
Reverse Recovery Charge	$Q_{RR}$			559		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

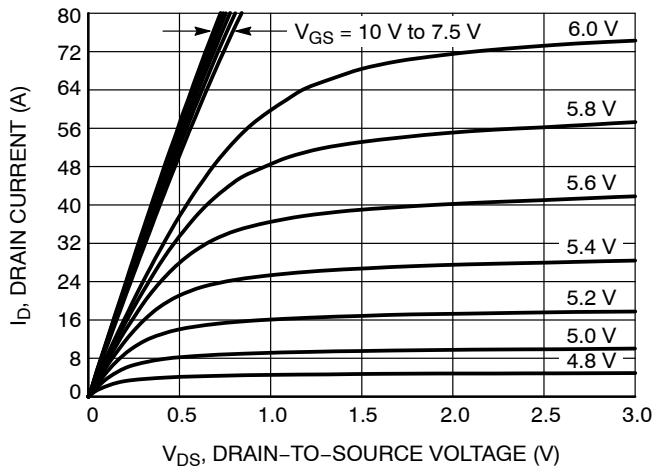


Figure 1. On-Region Characteristics

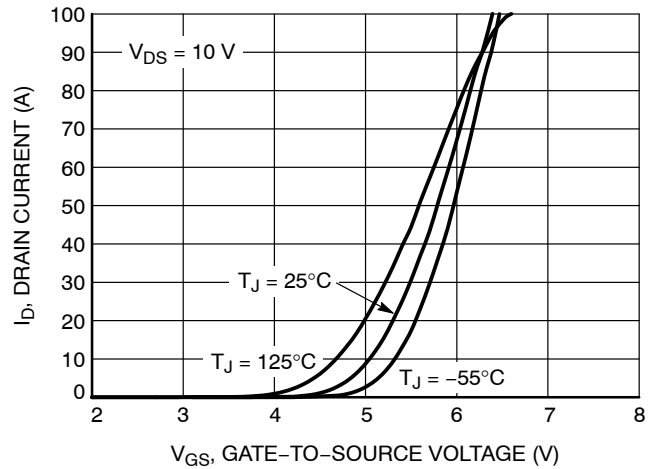


Figure 2. Transfer Characteristics

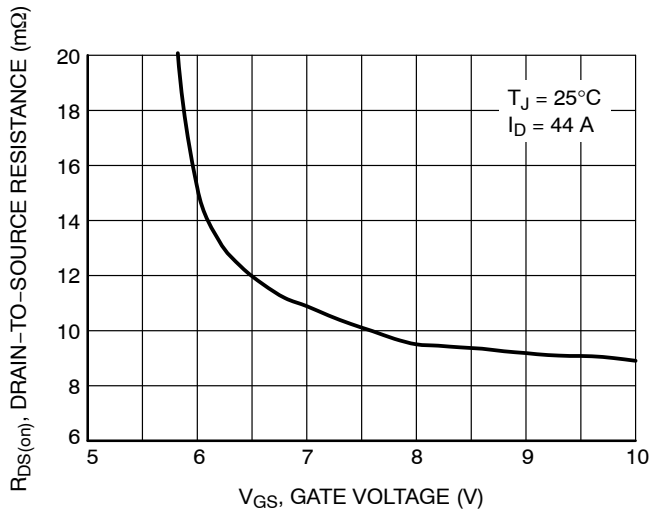


Figure 3. On-Resistance vs. Gate-to-Source Voltage

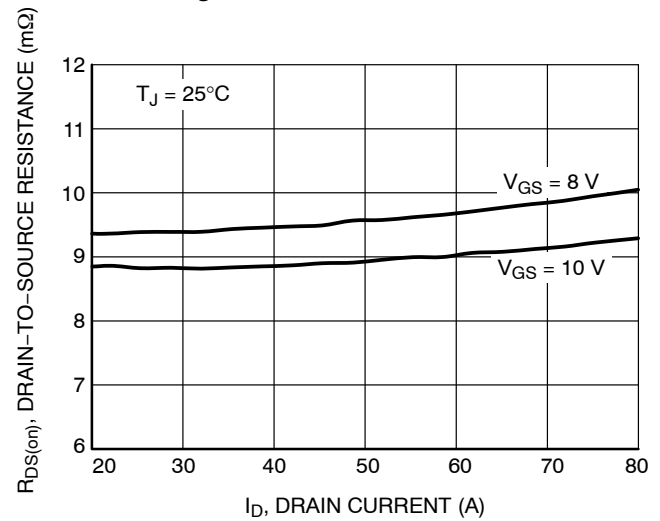


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

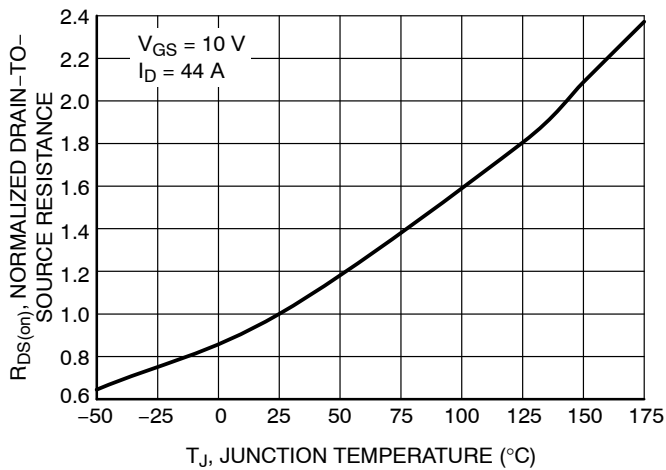


Figure 5. On-Resistance Variation with Temperature

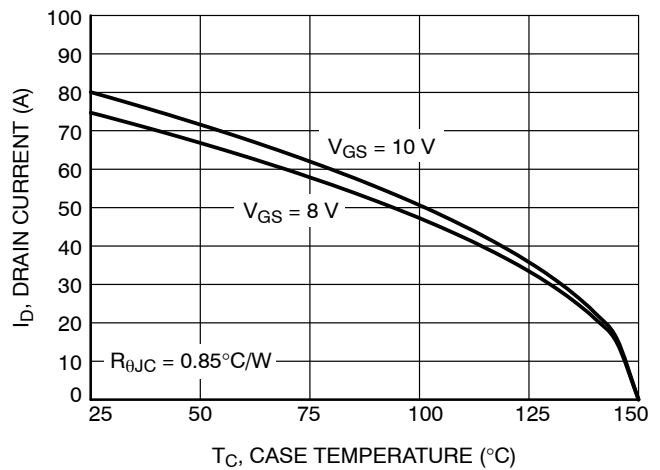


Figure 6. Maximum Continuous Drain Current vs. Case Temperature

# NTMFSC012N15MC

## TYPICAL CHARACTERISTICS

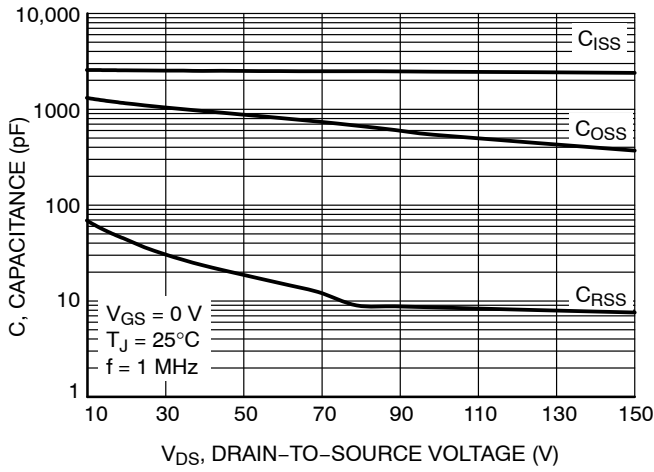


Figure 7. Capacitance Variation

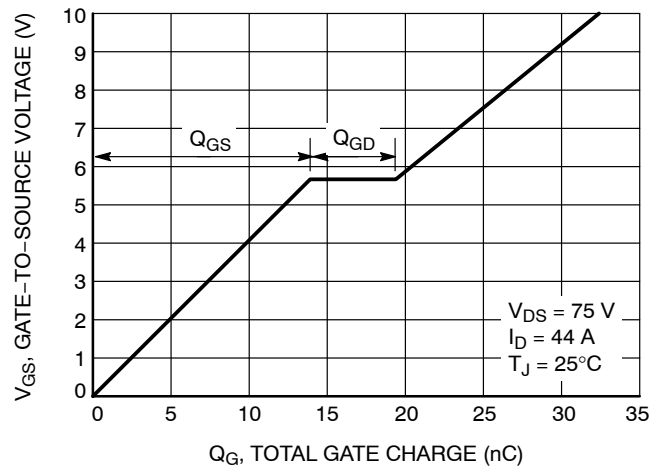


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

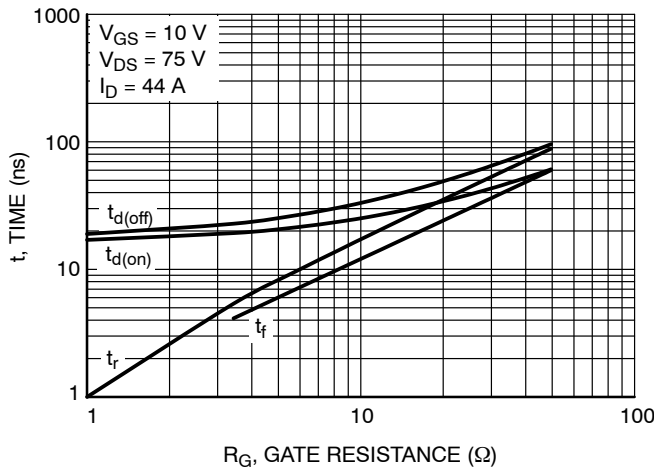


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

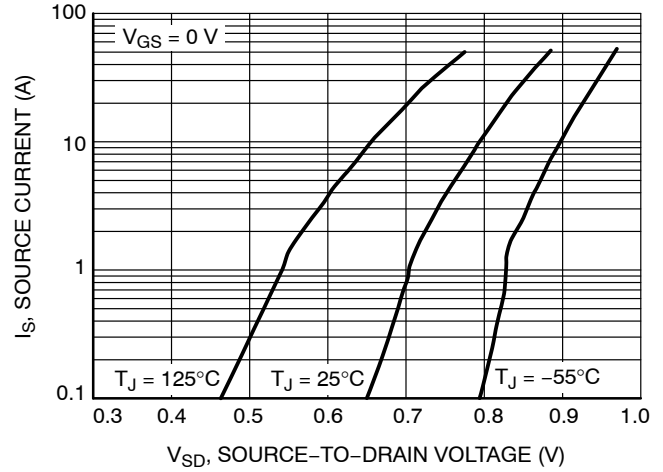


Figure 10. Diode Forward Voltage vs. Current

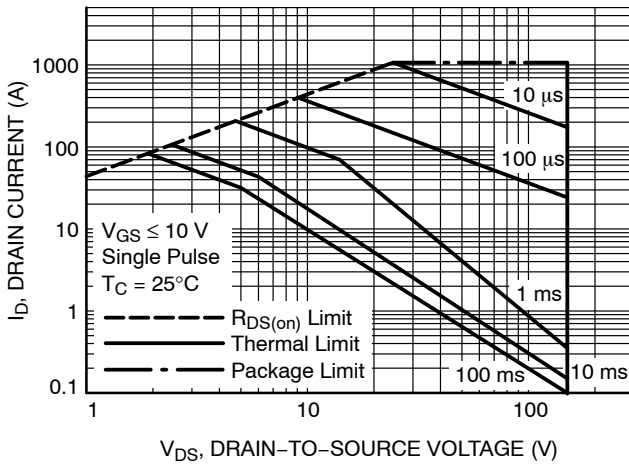


Figure 11. Safe Operating Area

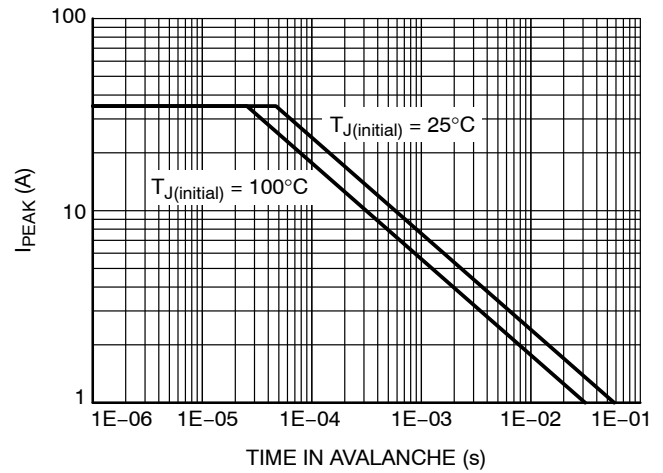


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NTMFSC012N15MC

## TYPICAL CHARACTERISTICS

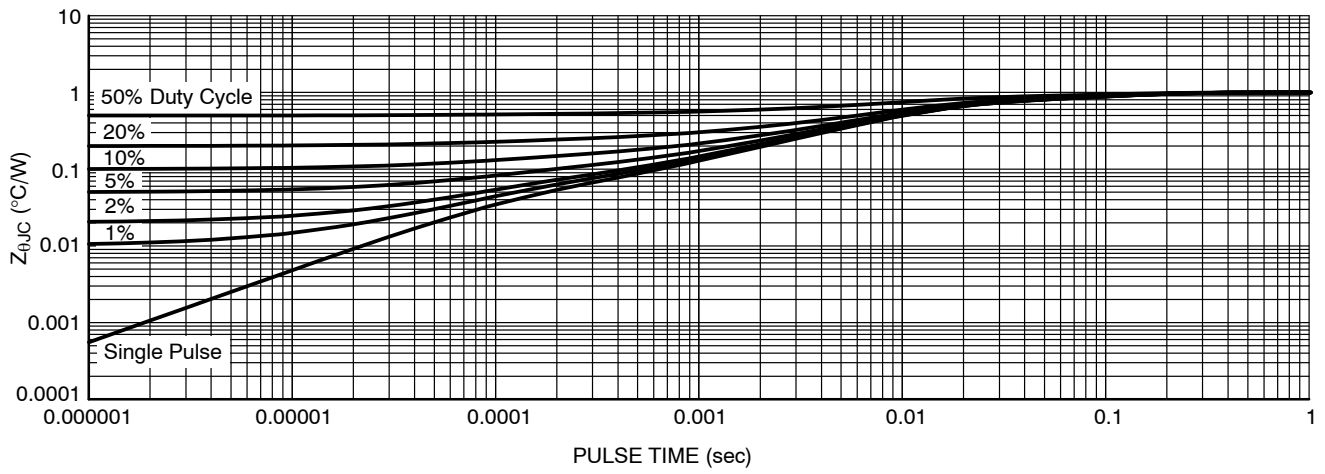
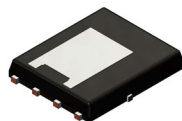


Figure 13. Thermal Characteristics

# MECHANICAL CASE OUTLINE

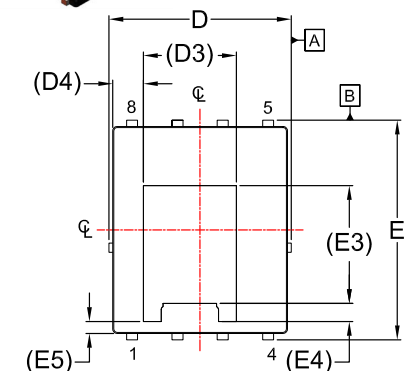
## PACKAGE DIMENSIONS

ON Semiconductor®

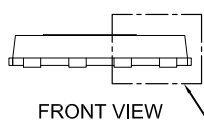


### DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

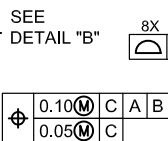
DATE 25 AUG 2020



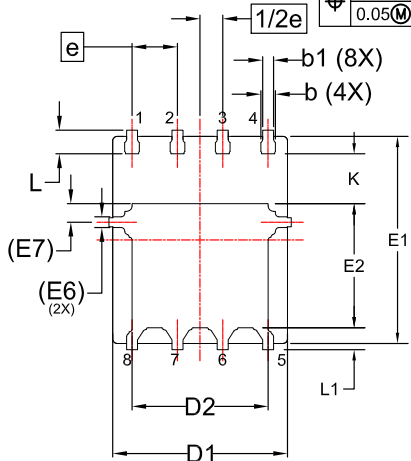
TOP VIEW



FRONT VIEW

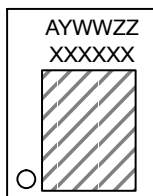


0.10 (M) C A B  
0.05 (M) C



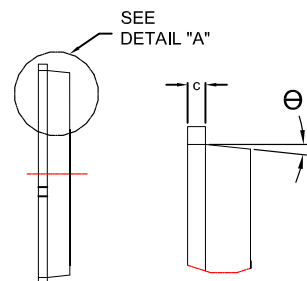
BOTTOM VIEW

### GENERIC MARKING DIAGRAM\*



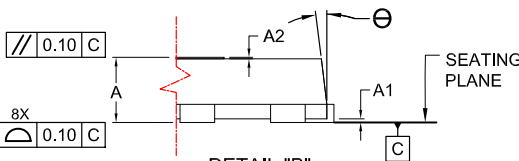
XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



SIDE VIEW

DETAIL "A"  
SCALE: 2:1

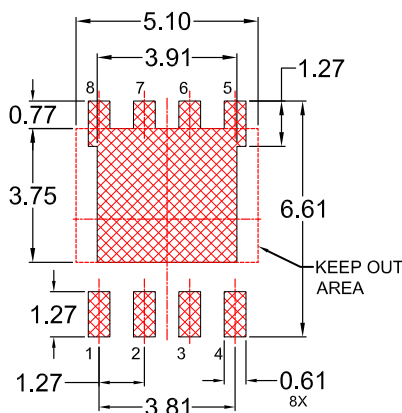


DETAIL "B"  
SCALE: 2:1

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°



LAND PATTERN  
RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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DESCRIPTION: DFN8 5x6.15, 1.27P, DUAL COOL

PAGE 1 OF 1

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