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DATA SHEET
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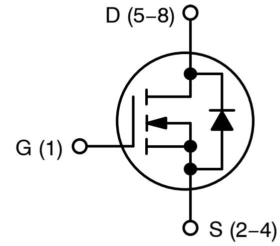
MOSFET - Power, Single N-Channel, DUAL COOL®

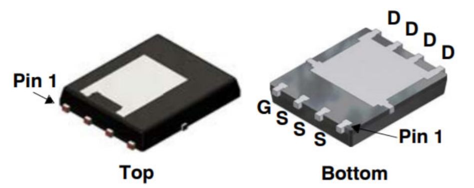
80 V, 10 mΩ, 61 A

NTMFSC011N08M7

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
80 V	10 mΩ @ 10 V	61 A

N−Channel MOSFET





DFN8 5x6
(Dual Cool 56)
CASE 506EG

Features

- DUAL COOL Top Side Cooling PQFN Package
- Max $r_{DS(on)}$ = 10 mΩ at V_{GS} = 10 V, I_D = 10 A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- 100% UIL Tested
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

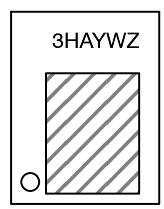
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	80	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	Steady State	T_C = 25°C	I_D	61	A
		T_C = 100°C		38.6	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	78.1	W
		T_C = 100°C		31.2	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T_A = 25°C	I_D	12.5	A
		T_A = 100°C		7.9	
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)		T_A = 25°C	P_D	3.3	W
		T_A = 100°C		1.3	
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	180	A
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	61	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 3.9 A)			E_{AS}	640	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 1 in^2 pad size, 1 oz Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

MARKING DIAGRAM



3H = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
Z = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping
NTMFSC011N08M7	DFN8 (Pb−Free)	3000 / Tape & Reel

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		80			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				49		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 80 V	T_J = 25°C			10	μA
			T_J = 125°C			100	
Zero Gate Voltage Drain Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V				±100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = $V_{DS,}$ I_D = 120 μA		2.5	3.3	4.5	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−9		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 10 A		7.6	10	mΩ
Forward Transconductance	gFS	V_{DS} = 5 V	I_D = 10 A		21.5	40	S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{iss}	V_{GS} = 0 V, f = 1 MHz	V_{DS} = 0 V		2373		pF
	C_{iss}		V_{DS} = 40 V		2080	2700	
Output Capacitance	C_{oss}				286	430	
Reverse Transfer Capacitance	C_{rss}				11	17	
Gate Resistance	R_g	V_{GS} = 0.5 V, f = 1MHz			1	2	Ω
Threshold Gate Charge	$Q_{g(th)}$	V_{GS} = 0 to 2 V	V_{GS} = 10 V, V_{DS} = 40 V; I_D = 10 A		4.3		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 0 to 10 V			29.3	38	
Gate to Source Gate Charge	Q_{gs}	V_{GS} = 0 to 10 V			11.8		
Gate to Drain “Miller” Charge	Q_{gd}				4.3		
Plateau Voltage	V_{GP}				5.5		V
Output Charge	Q_{oss}	V_{DS} = 40 V, V_{GS} = 0 V			26		nC
SWITCHING CHARACTERISTICS (Note 5)							
Turn−On Delay Time	$t_{d(ON)}$	V_{DD} = 40 V, I_D = 10 A, V_{GS} = 10 V, R_{GEN} = 6 Ω			14		ns
Turn−On Rise Time	t_r				6		ns
Turn−Off Delay Time	$t_{d(OFF)}$				27		ns
Turn−Off Fall Time	t_f				6		ns
DRAIN – SOURCE DIODE CHARACTERISTICS							
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 10 A, V_{GS} = 0 V			0.82	1.2	V
Reverse Recovery Time	T_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 10 A			41	50	ns
Charge Time	t_a				24.6		
Discharge Time	t_b				16.1		
Reverse Recovery Charge	Q_{RR}				45	58	nC

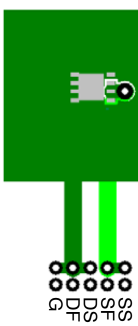
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

THERMAL CHARACTERISTICS

Symbol	Parameter		Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Top Source)	1.6	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Bottom Drain)	3.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1l)	13	

6. $R_{\theta JA}$ is determined with the device mounted on a FR−4 board using a specified pad of 2 oz copper as shown below. $R_{\theta JA}$ is guaranteed by design while $R_{\_CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in2 pad of 2 oz copper.

b) 81°C/W when mounted on a minimum pad of 2 oz copper.

c) Still air, 20.9·10.4·12.7 mm Aluminum Heat Sink, 1 in2 pad of 2 oz copper
d) Still air, 20.9·10.4·12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
e) Still air, 45.2·41.4·11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, 1 in2 pad of 2 oz copper
f) Still air, 45.2·41.4·11.7 mm Aavid Thermalloy Part # 10−L41B−11 Heat Sink, minimum pad of 2 oz copper
g) .200FPM Airflow, No Heat Sink, 1 in2 pad of 2 oz copper
h) .200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
i) .200FPM Airflow, 20.9·10.4·12.7 mm Aluminum Heat Sink, 1 in2 pad of 2 oz copper
j) .200FPM Airflow, 20.9·10.4·12.7 mm Aluminum Heat Sink, minimum pad of 2 oz copper
k) .200FPM Airflow, 45.2·41.4·11.7 mm Aavid Thermalloy Part # 10 − L41B − 11 Heat Sink, 1 in2 pad of 2 oz copper
l) .200FPM Airflow, 45.2·41.4·11.7 mm Aavid Thermalloy Part # 10 − L41B − 11 Heat Sink, minimum pad of 2 oz copper

7. Pulse Test: Pulse Width < 300 _s, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

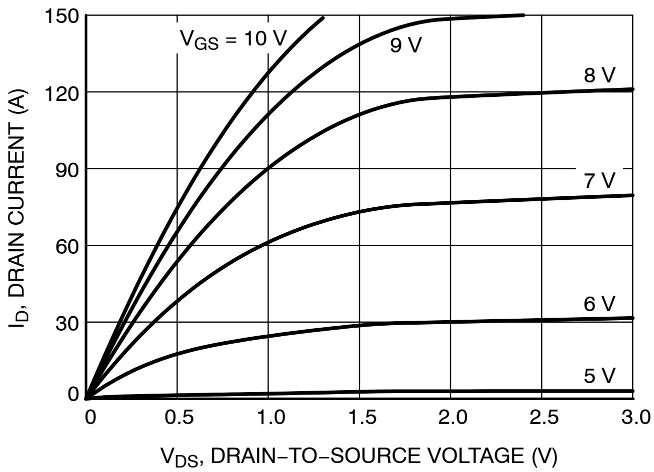


Figure 1. On−Region Characteristics

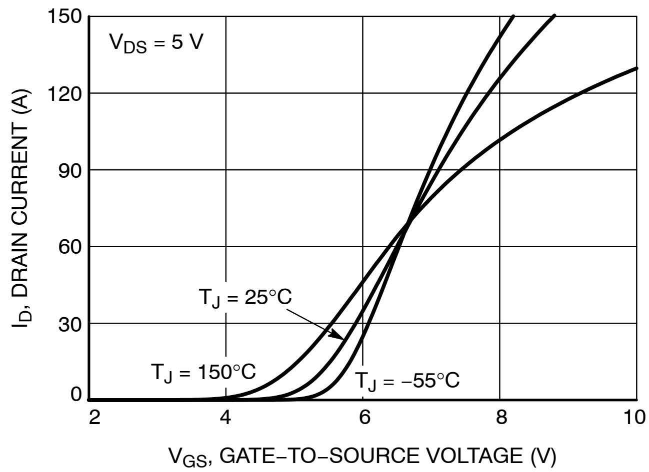


Figure 2. Transfer Characteristics

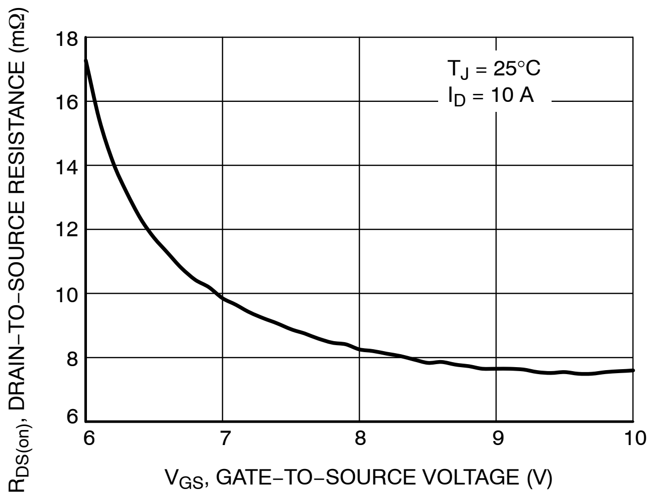


Figure 3. On−Resistance vs. Gate−to−Source Voltage

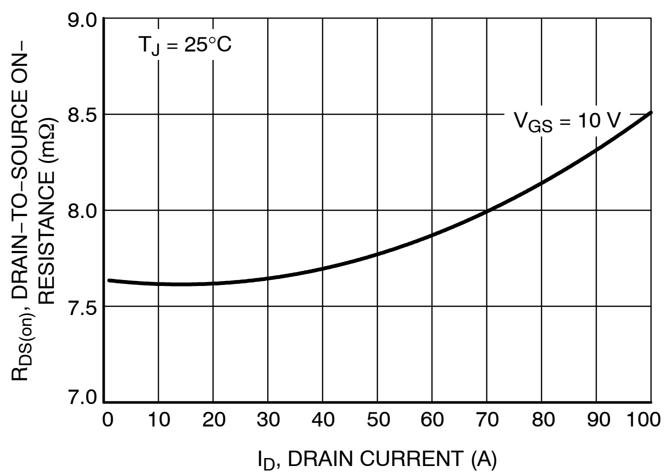


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

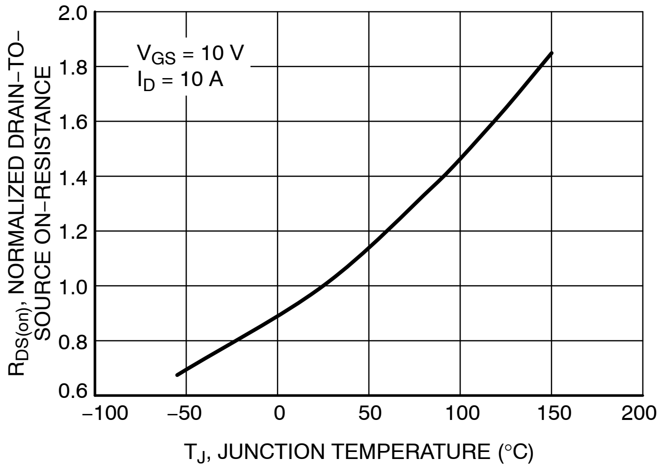


Figure 5. On−Resistance Variation with Temperature

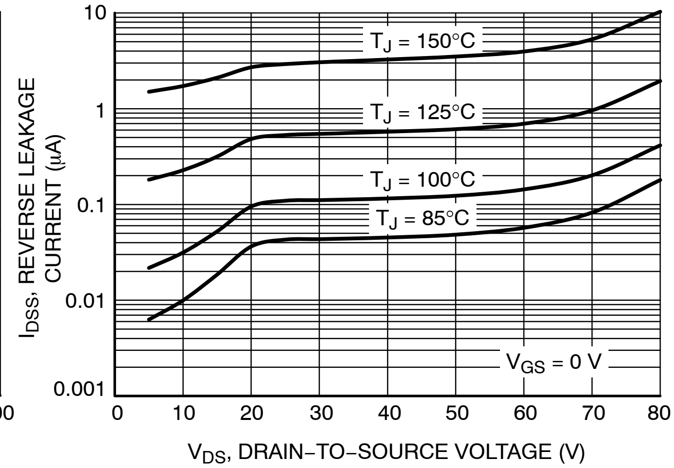


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

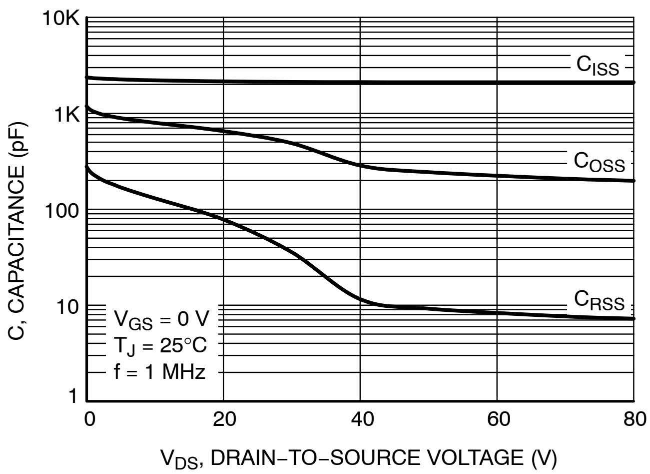


Figure 7. Capacitance Variation

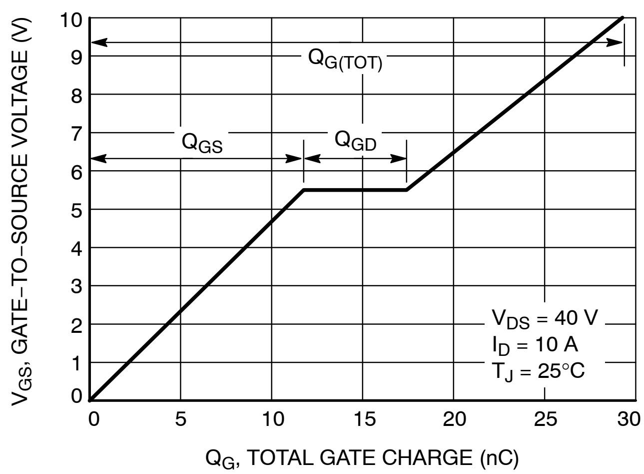


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

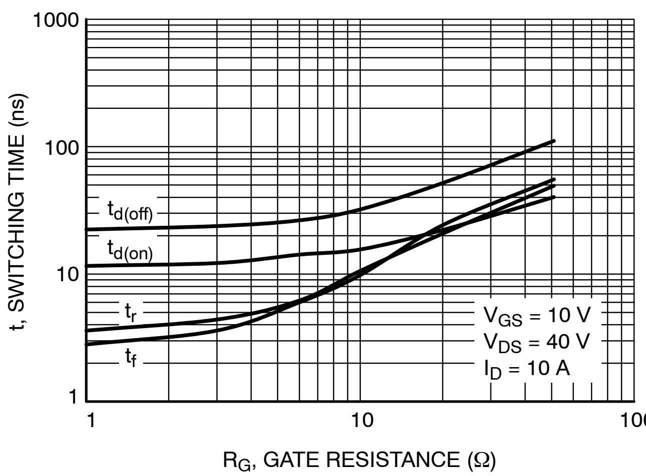


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

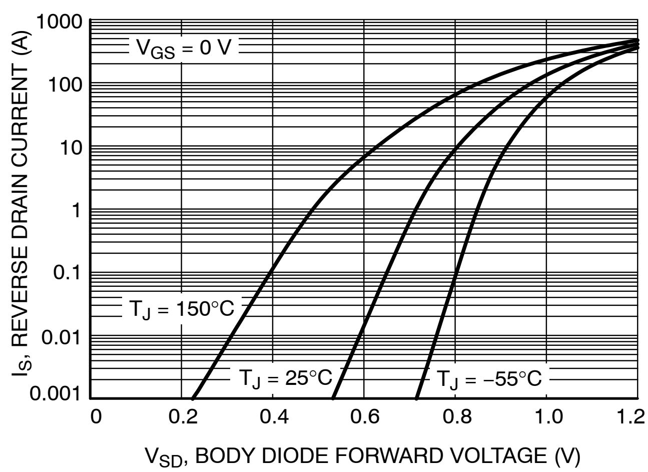


Figure 10. Diode Forward Voltage vs. Current

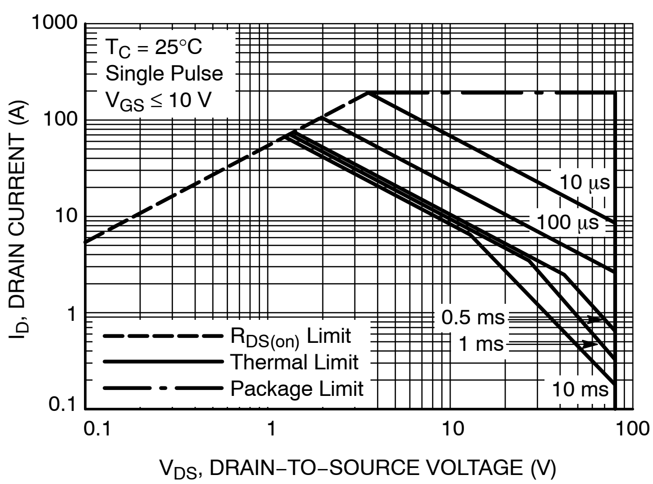


Figure 11. Safe Operating Area

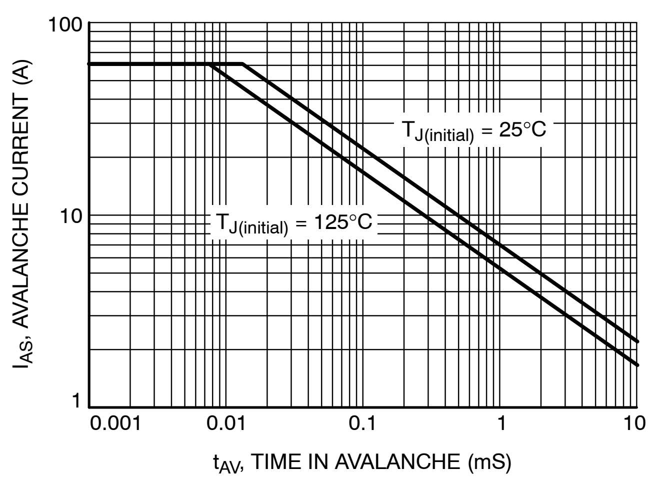


Figure 12. I_{PEAK} vs. Time in Avalanche

TYPICAL CHARACTERISTICS

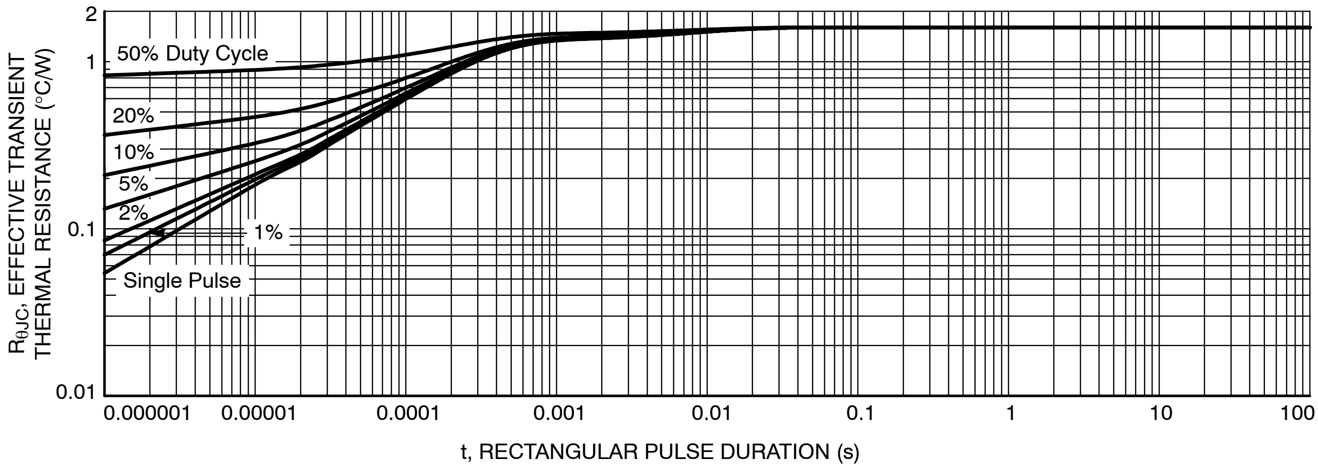
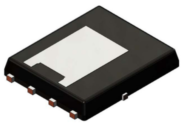
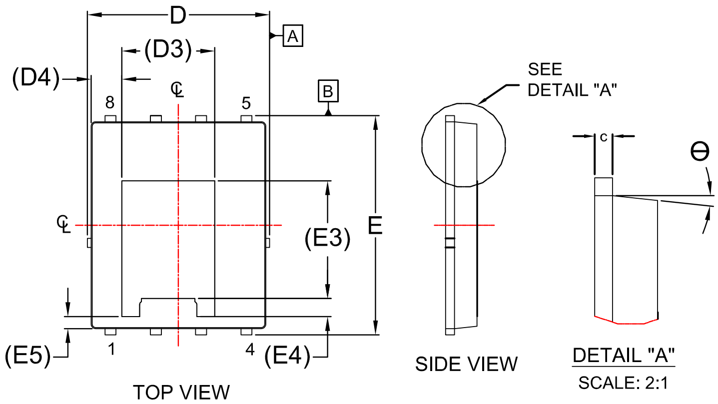


Figure 13. Thermal Response



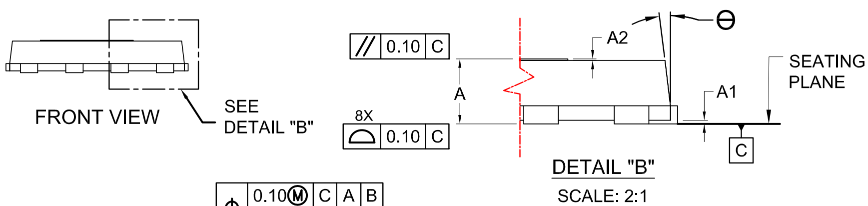
DFN8 5x6.15, 1.27P, DUAL COOL
CASE 506EG
ISSUE D

DATE 25 AUG 2020

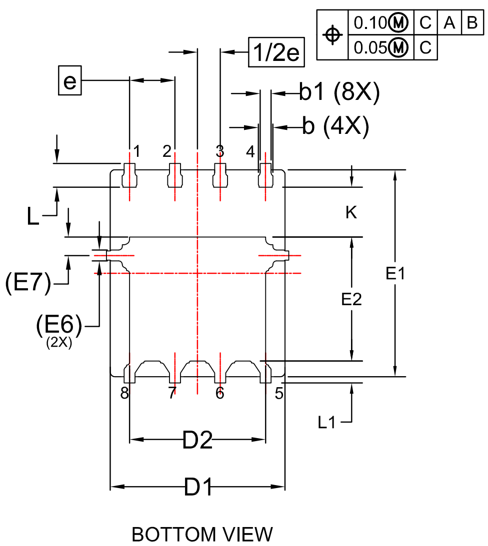


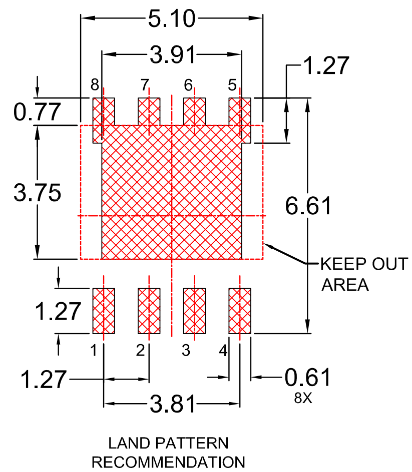
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



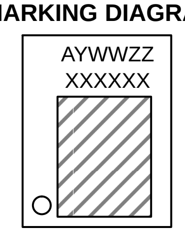
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
Θ	0°	---	12°





*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**DFN8 5x6.15, 1.27P, DUAL COOL**	**PAGE 1 OF 1**

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