

MOSFET – Power, Single, N-Channel

100 V, 3.5 mΩ, 142 A

NTMFS3D2N10MD

Features

- Shielded Gate MOSFET Technology
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Low Q_{RR} , Soft Recovery Body Diode
- Low Q_{OSS} to Improve Light Load Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

Typical Applications

- Primary Switch in Isolated DC-DC Converter
- Synchronous Rectification (SR) in DC-DC and AC-DC
- AC-DC Adapters (USB PD) SR
- Load Switch, Hotswap, and ORing Switch
- BLDC Motor and Solar Inverter

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	100	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	I_D	142	A
Power Dissipation $R_{\theta JC}$ (Note 1)			
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	I_D	19	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			
Pulsed Drain Current	I_{DM}	879	A
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	129	A
Single Pulse Drain-to-Source Avalanche Energy ($I_{AV} = 22\text{ A}$) (Note 6)	E_{AS}	726	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)	T_L	300	$^\circ\text{C}$

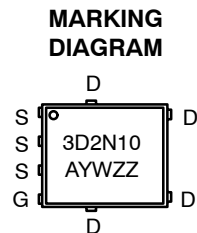
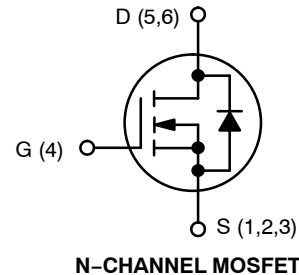
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Note 1)	$R_{\theta JC}$	0.8	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	45.2	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using 1 in² pad size, 1 oz. Cu pad.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	3.5 mΩ @ 10 V	142 A
	5.8 mΩ @ 6 V	



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS3D2N10MDT1G	DFN5 (Pb-Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		30		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 316\text{ }\mu\text{A}$	2		4	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	$I_D = 316\text{ }\mu\text{A}$, ref to 25°C		-8.1		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 50\text{ A}$		2.9	3.5	$\text{m}\Omega$
		$V_{GS} = 6\text{ V}, I_D = 30.5\text{ A}$		4.3	5.8	
Forward Transconductance	g_{FS}	$V_{DS} = 8\text{ V}, I_D = 50\text{ A}$		115		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		0.6	1.25	Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		3900		pF
Output Capacitance	C_{OSS}			1100		
Reverse Transfer Capacitance	C_{RSS}			24		
Output Charge	Q_{OSS}	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}$		81		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 6\text{ V}, V_{DS} = 50\text{ V}, I_D = 50\text{ A}$		29		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 50\text{ A}$		48	71.3	
Gate-to-Source Charge	Q_{GS}			19		
Gate-to-Drain Charge	Q_{GD}			8	11.8	
Plateau Voltage	V_{GP}			5		V

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 50\text{ A}, R_G = 6\text{ }\Omega$		26.1		ns
Rise Time	t_r			7.2		
Turn-Off Delay Time	$t_{d(OFF)}$			39		
Fall Time	t_f			6.3		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 50\text{ A}$	$T_J = 25^\circ\text{C}$		0.83		V
			$T_J = 125^\circ\text{C}$		0.70		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 1000\text{ A}/\mu\text{s}, I_S = 30.5\text{ A}$		31			ns
Reverse Recovery Charge	Q_{RR}			271			nC
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 50\text{ A}$		60			ns
Reverse Recovery Charge	Q_{RR}			74			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

4. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

5. Pulse Test: pulse width < 300 μs , duty cycle < 2%.

6. E_{AS} of 726 mJ is based on started $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AV} = 22\text{ A}$, $V_{DD} = 100\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AV} = 69\text{ A}$.

7. As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

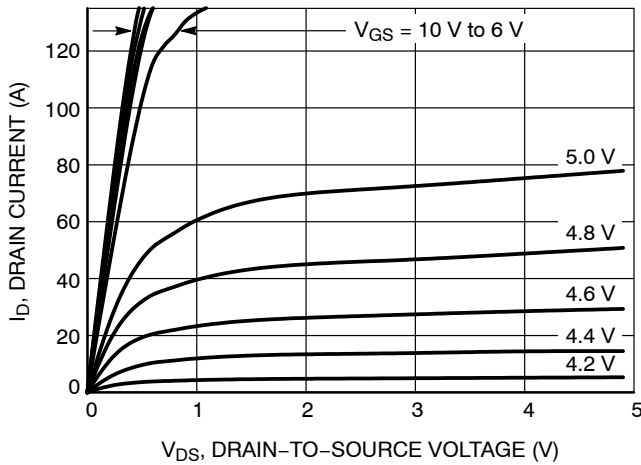


Figure 1. On-Region Characteristics

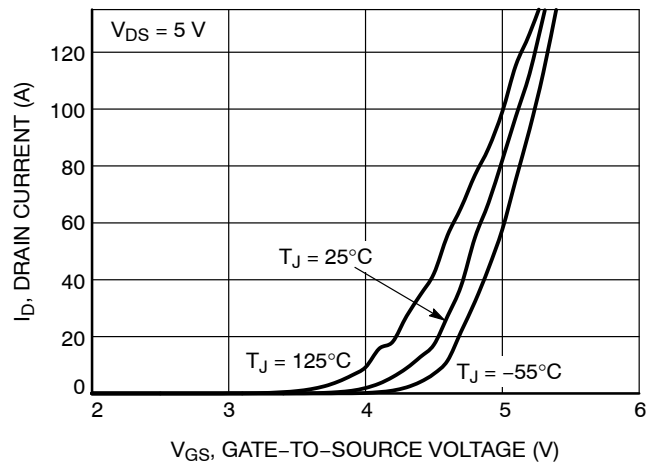


Figure 2. Transfer Characteristics

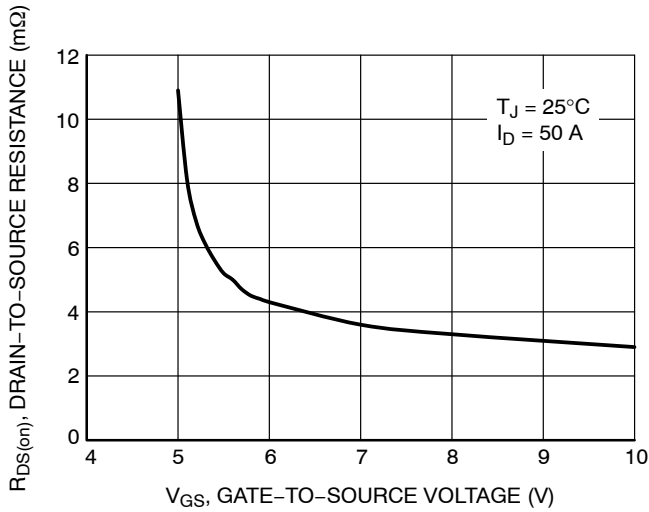


Figure 3. On-Resistance vs. Gate-to-Source Voltage

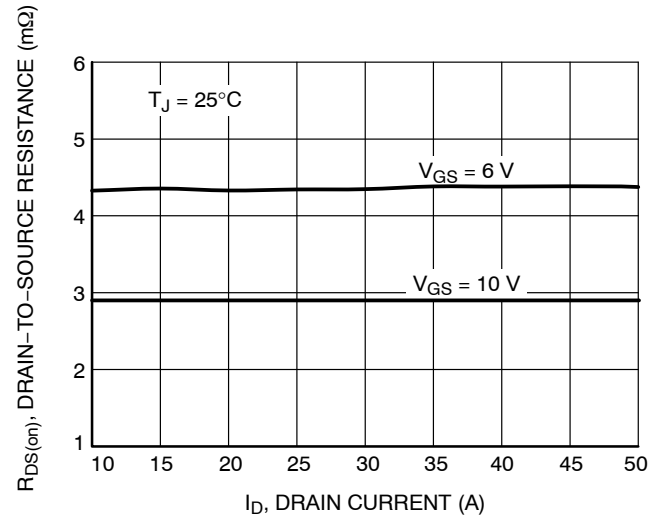


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

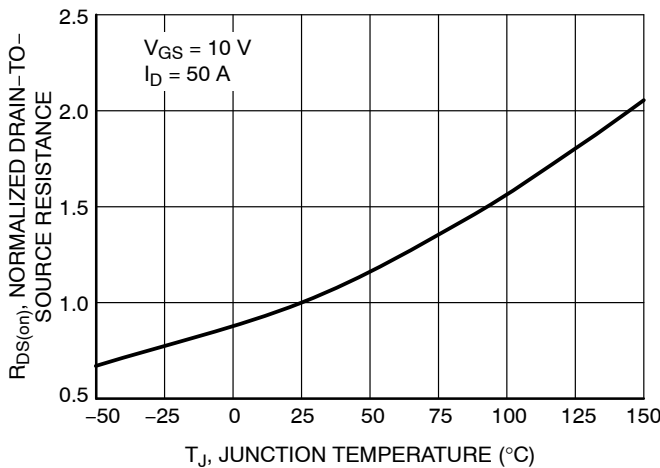


Figure 5. On-Resistance Variation with Temperature

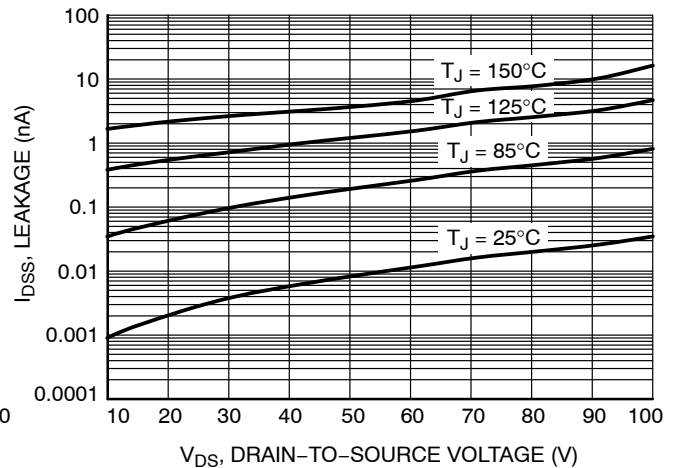


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

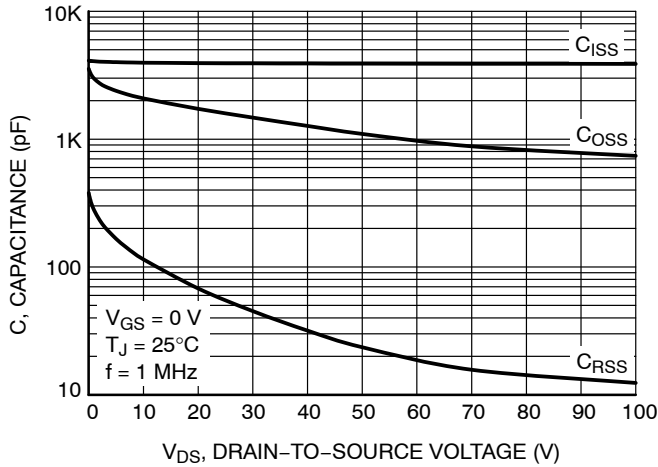


Figure 7. Capacitance Variation

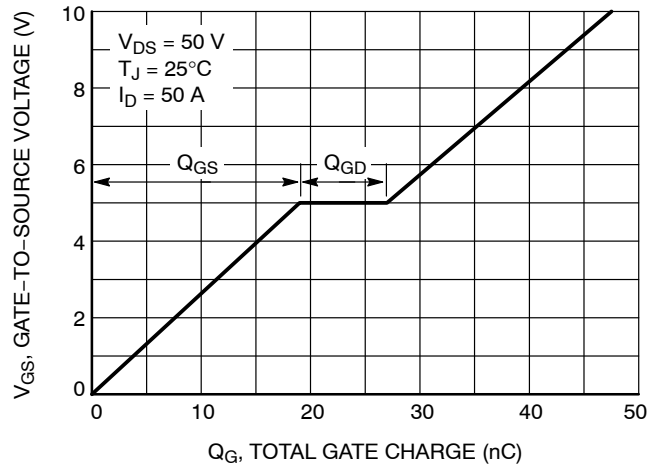


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

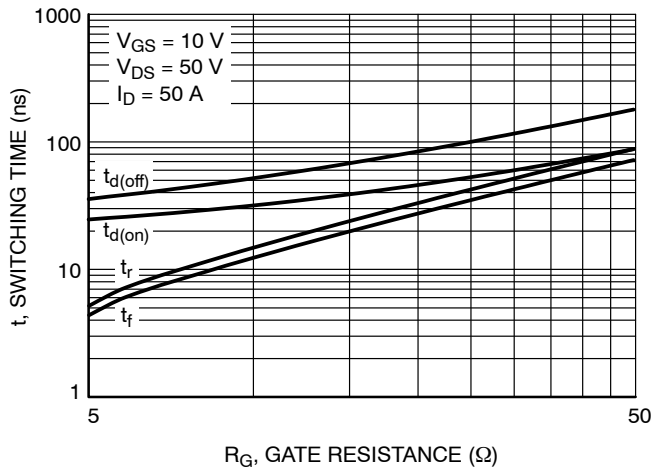


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

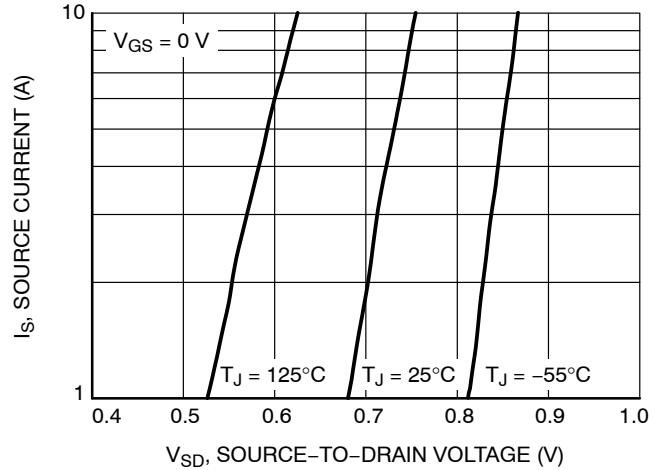


Figure 10. Diode Forward Voltage vs. Current

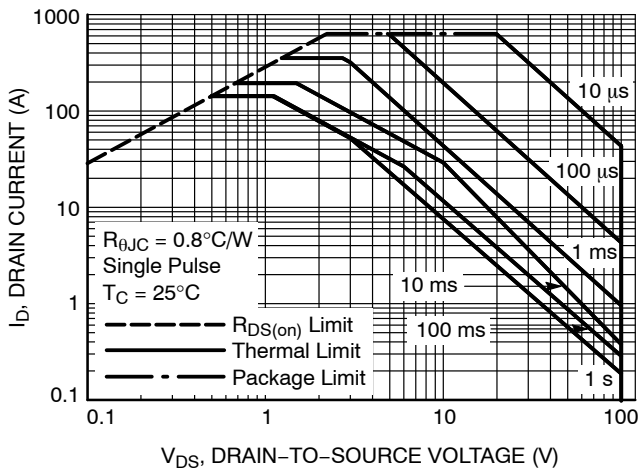


Figure 11. Forward Bias Safe Operating Area

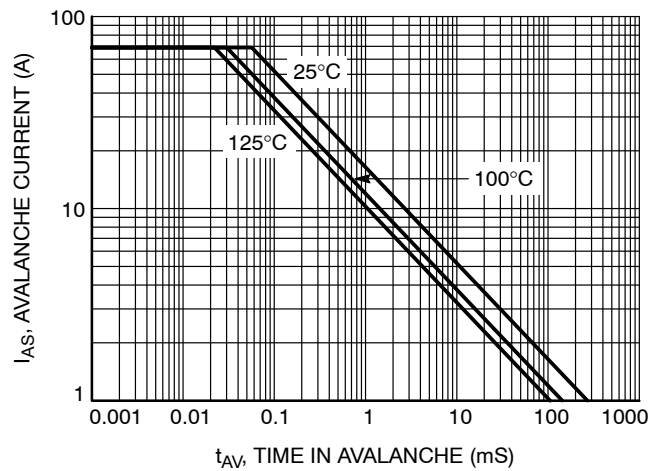


Figure 12. Unclamped Inductive Switching Capability

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TYPICAL CHARACTERISTICS

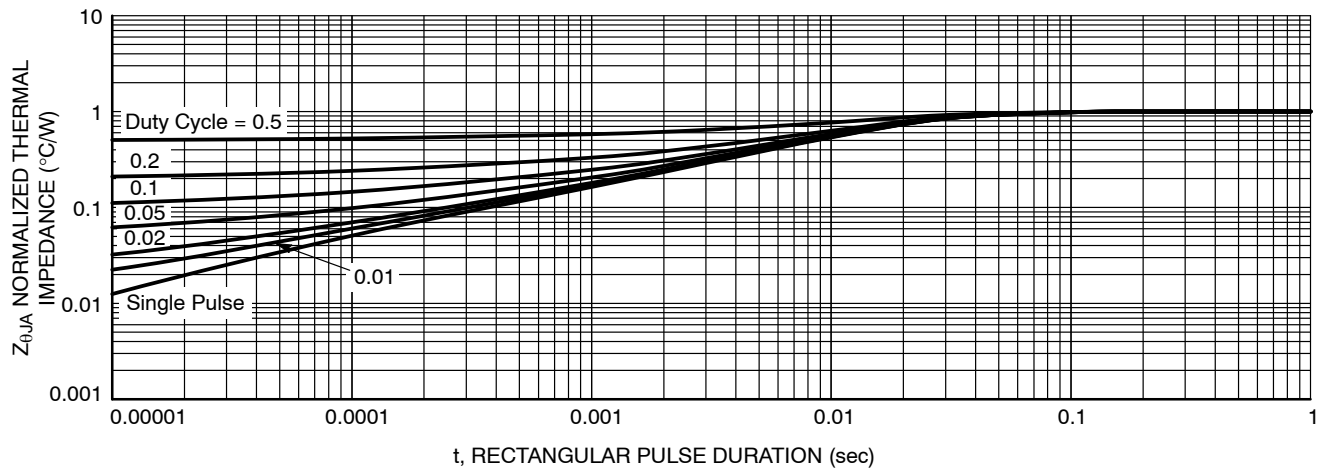
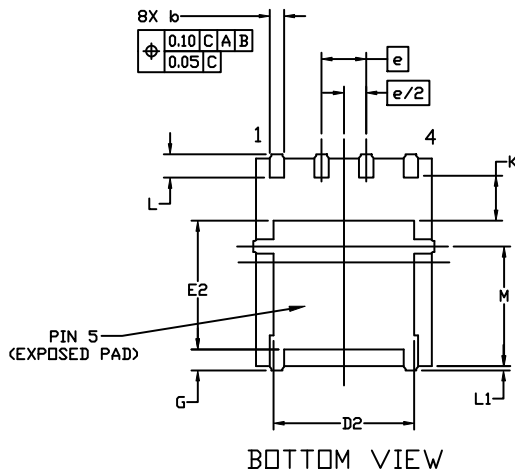
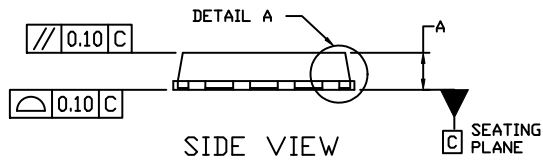
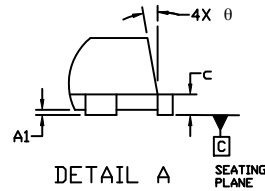
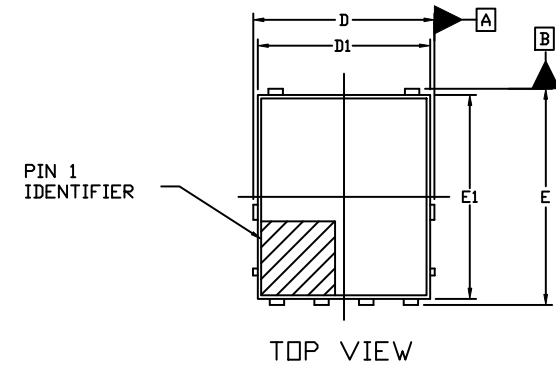


Figure 13. Transient Thermal Impedance

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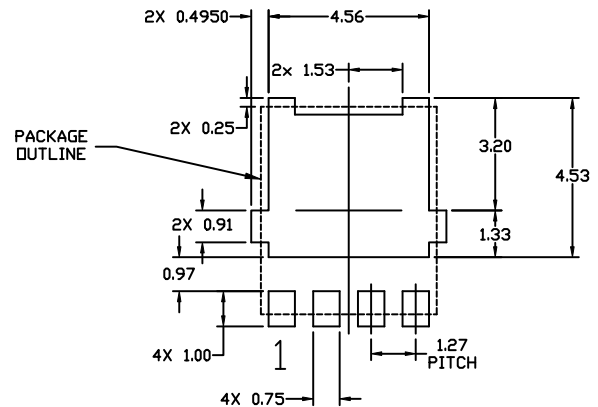
PACKAGE DIMENSIONS

DFN5 5x6, 1.27P (SO-8FL)
CASE 506EZ
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.80	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
k	1.10	1.20	1.40
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0°	---	12°



RECOMMENDED MOUNTING FOOTPRINT

- * For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

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