

NTMFD4C86N

PowerPhase, Dual N-Channel SO8FL

30 V, High Side 20 A / Low Side 32 A

Features

- Co-Packaged Power Stage Solution to Minimize Board Space
- Minimized Parasitic Inductances
- Optimized Devices to Reduce Power Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- DC-DC Converters
- System Voltage Rails
- Point of Load

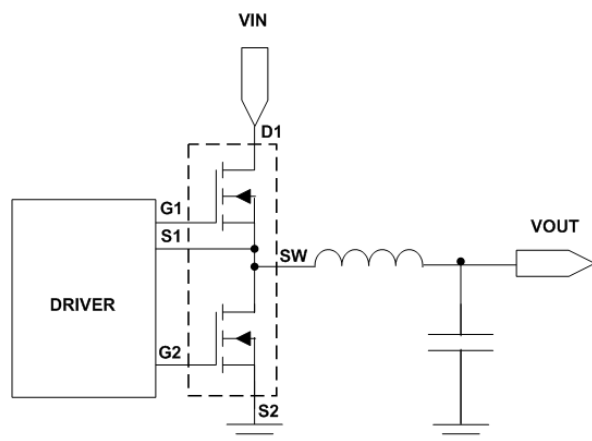


Figure 1. Typical Application Circuit

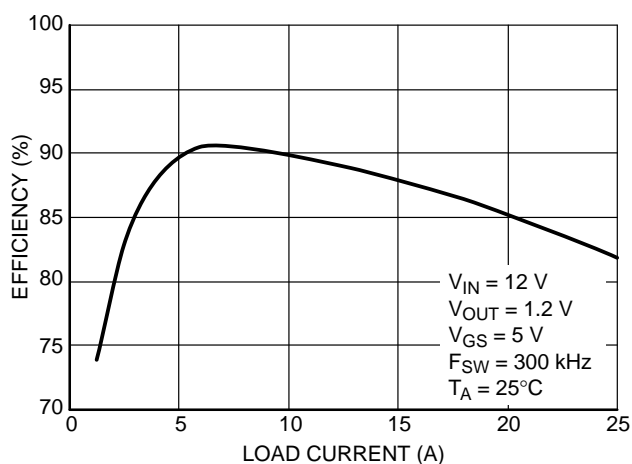


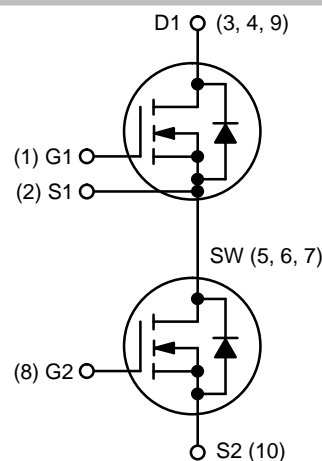
Figure 2. Typical Efficiency Performance
POWERPHASEGEVB Evaluation Board



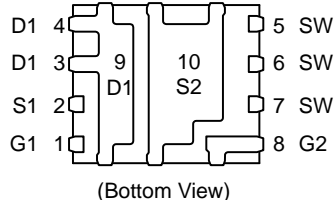
ON Semiconductor®

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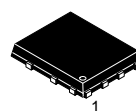
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
Q1 Top FET 30 V	5.4 mΩ @ 10 V	20 A
	8.1 mΩ @ 4.5 V	
Q2 Bottom FET 30 V	2.6 mΩ @ 10 V	32 A
	3.4 mΩ @ 4.5 V	



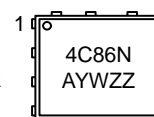
PIN CONNECTIONS



MARKING DIAGRAM



DFN8
CASE 506CR



4C86N = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

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MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter				Symbol	Value	Unit
Drain-to-Source Voltage			Q1	V _{DSS}	30	V
Drain-to-Source Voltage			Q2			
Gate-to-Source Voltage			Q1	V _{GS}	±20	V
Gate-to-Source Voltage			Q2			
Continuous Drain Current R _{θJA} (Note 1)	Steady State	T _A = 25°C	Q1	I _D	14.8	A
		T _A = 85°C			10.7	
		T _A = 25°C	Q2		23.7	
		T _A = 85°C			17.1	
Power Dissipation R _{θJA} (Note 1)		T _A = 25°C	Q1	P _D	1.89	W
			Q2			
Continuous Drain Current R _{θJA} ≤ 10 s (Note 1)		T _A = 25°C	Q1	I _D	20.2	A
			T _A = 85°C			
		T _A = 25°C	Q2		32.3	
			T _A = 85°C			
Power Dissipation R _{θJA} ≤ 10 s (Note 1)		T _A = 25°C	Q1	P _D	3.51	W
			Q2			
Continuous Drain Current R _{θJA} (Note 2)		T _A = 25°C	Q1	I _D	11.3	A
			T _A = 85°C			
		T _A = 25°C	Q2		18.1	
			T _A = 85°C			
Power Dissipation R _{θJA} (Note 2)	T _A = 25 °C	Q1	P _D	1.10	W	
		Q2				
Pulsed Drain Current		T _A = 25°C t _p = 10 μs	Q1	I _{DM}	160	A
			Q2		280	
Operating Junction and Storage Temperature			Q1	T _J , T _{STG}	–55 to +150	°C
			Q2			
Source Current (Body Diode)			Q1	I _S	10	A
			Q2		10	
Drain to Source DV/DT				dV/dt	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy (T _J = 25°C, V _{DD} = 50 V, V _{GS} = 10 V, L = 0.1 mH, R _G = 25 Ω)		I _L = 20 A _{pk}	Q1	EAS	20	mJ
		I _L = 40 A _{pk}	Q2	EAS	80	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)				T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

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THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Top) – Steady State (Note 3)	$R_{\theta JC}$	3.3	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	66.0	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	113.7	
Junction-to-Ambient – ($t \leq 10$ s) (Note 3)	$R_{\theta JA}$	35.6	

3. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Break-down Voltage	Q1	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		30		V
	Q2				30		
Drain-to-Source Break-down Voltage Temperature Coefficient	Q1	$V_{(BR)DSS} / T_J$				17	mV / °C
	Q2					16.5	
Zero Gate Voltage Drain Current	Q1	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
				$T_J = 125^\circ\text{C}$		10	
	Q2	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	
				$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	Q1	I_{GSS}	$V_{GS} = 0\text{ V}, V_{DS} = +20\text{ V}$			100	nA
	Q2					100	

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	Q1	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250 \mu A$		1.3		2.2	V
	Q2				1.3		2.2	
Negative Threshold Temperature Coefficient	Q1	$V_{GS(TH)} / T_J$				4.5		mV / °C
	Q2					4.6		
Drain-to-Source On Resistance	Q1	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}$	$I_D = 30 \text{ A}$		4.3	5.4	mΩ
			$V_{GS} = 4.5 \text{ V}$	$I_D = 18 \text{ A}$		6.5	8.1	
	Q2		$V_{GS} = 10 \text{ V}$	$I_D = 30 \text{ A}$		1.7	2.6	
			$V_{GS} = 4.5 \text{ V}$	$I_D = 12.5 \text{ A}$		2.4	3.4	

CAPACITANCES

Input Capacitance	Q1	C _{ISS}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 15 V		1153		pF
	Q2				3050		
Output Capacitance	Q1	C _{OSS}			532		
	Q2				1650		
Reverse Capacitance	Q1	C _{RSS}			107		
	Q2				77		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
CHARGES, CAPACITANCES & GATE RESISTANCE							
Total Gate Charge	Q1	Q _{G(TOT)}	V _{GS} = 4.5 V, V _{DS} = 15 V; I _D = 30 A		10.9		nC
	Q2				21.6		
Threshold Gate Charge	Q1	Q _{G(TH)}			1.2		
	Q2				1.4		
Gate-to-Source Charge	Q1	Q _{GS}			3.4		
	Q2				8.6		
Gate-to-Drain Charge	Q1	Q _{GD}			5.4		
	Q2				5.5		
Total Gate Charge	Q1	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 15 V; I _D = 30 A		22.2		nC
	Q2				47.5		
Gate Resistance	Q1	R _G	T _A = 25°C		1.0		Ω
	Q2				1.0		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		8.9		ns
	Q2				8.3		
Rise Time	Q1	t_r			21.2		
	Q2				15.1		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			15.3		
	Q2				19.3		
Fall Time	Q1	t_f			4.4		
	Q2				4.2		

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	Q1	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.7		ns
	Q2				6.3		
Rise Time	Q1	t_r			19.5		
	Q2				13.8		
Turn-Off Delay Time	Q1	$t_{d(OFF)}$			20.1		
	Q2				22.8		
Fall Time	Q1	t_f			2.8		
	Q2				3.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Voltage	Q1	VSD	VGS = 0 V, IS = 10 A	TJ = 25°C		0.80		V
				TJ = 125°C		0.60		
	Q2		VGS = 0 V, IS = 10 A	TJ = 25°C		0.78		
				TJ = 125°C		0.62		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	FET	Symbol	Test Condition	Min	Typ	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS							
Reverse Recovery Time	Q1	t _{RR}	V _{GS} = 0 V, d _I S/d _t = 100 A/μs, I _S = 30 A		29.1		ns
	Q2				33.7		
Charge Time	Q1	t _a			14.5		
	Q2				17.4		
Discharge Time	Q1	t _b			14.6		
	Q2				16.3		
Reverse Recovery Charge	Q1	Q _{RR}			21		nC
	Q2				27.5		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

6. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS – Q1

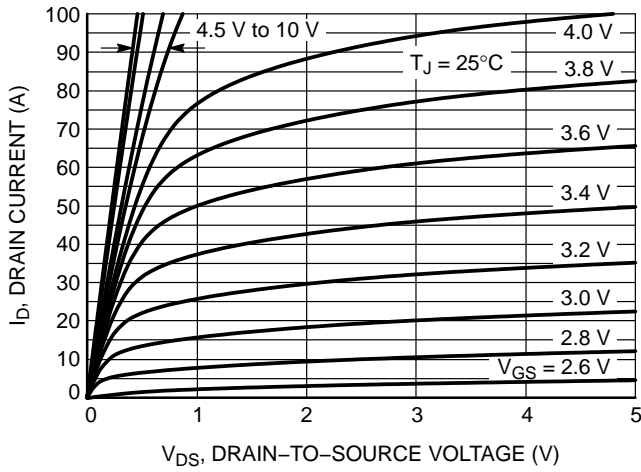


Figure 3. On-Region Characteristics

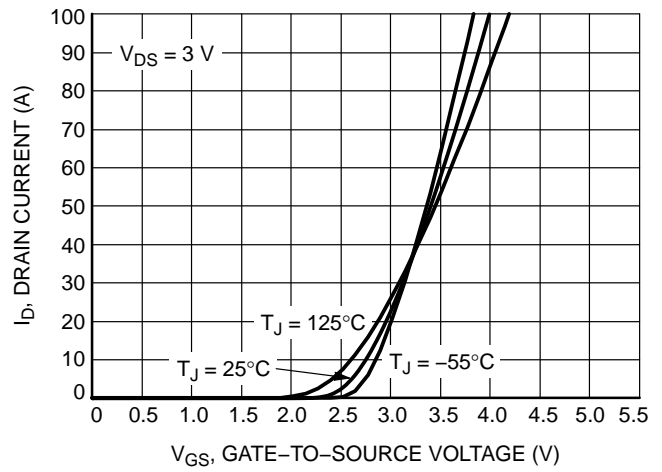


Figure 4. Transfer Characteristics

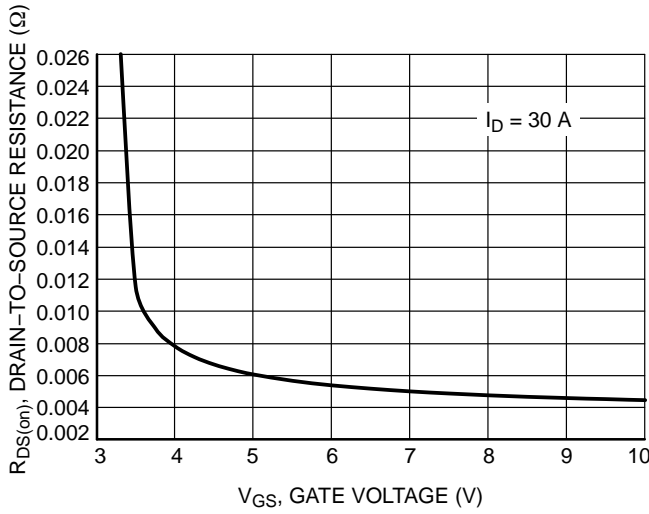


Figure 5. On-Resistance vs. Gate-to-Source Voltage

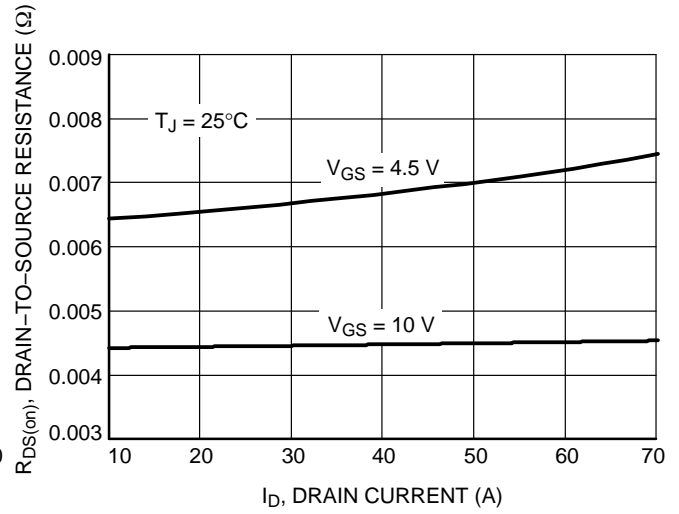


Figure 6. On-Resistance vs. Drain Current and Gate Voltage

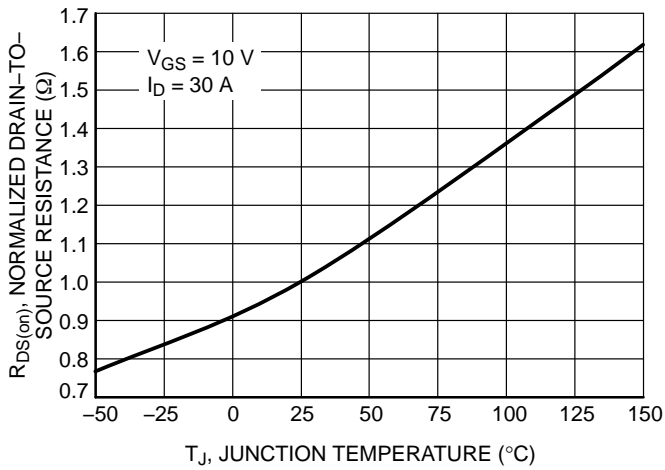


Figure 7. On-Resistance Variation with Temperature

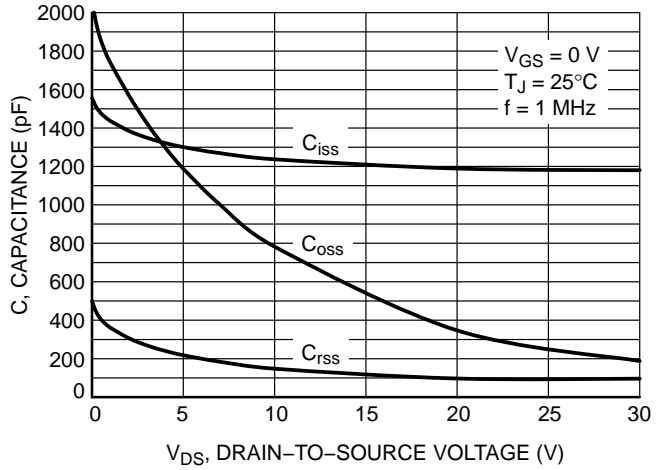


Figure 8. Capacitance Variation

TYPICAL CHARACTERISTICS – Q1

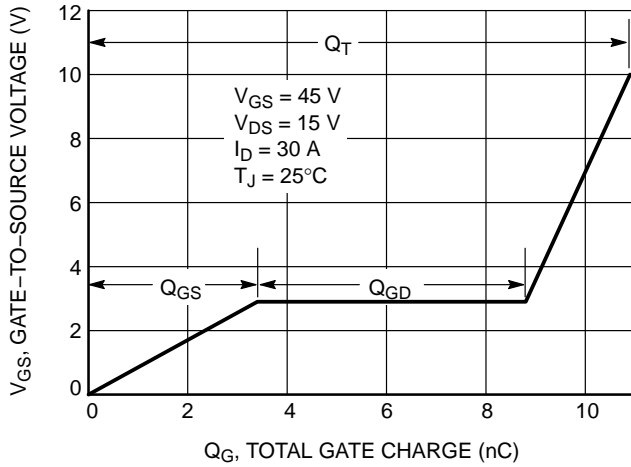


Figure 9. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

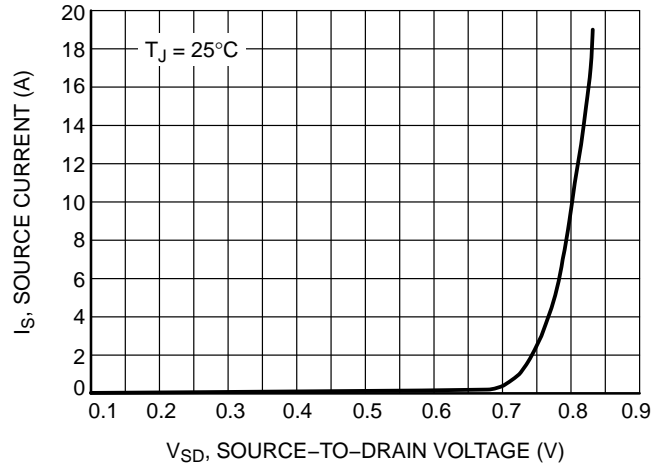


Figure 10. Diode Forward Voltage vs. Current

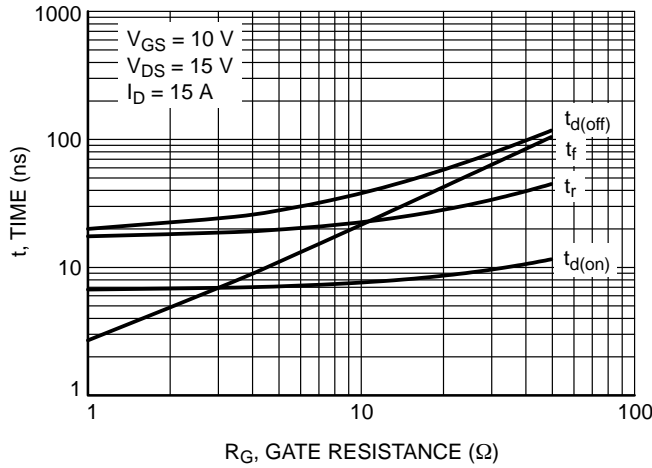


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

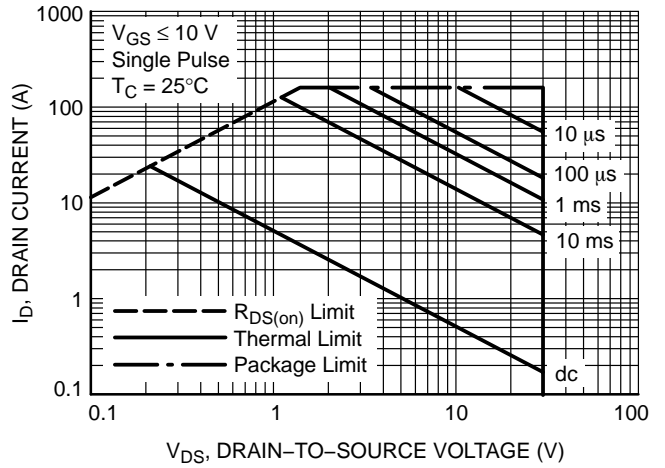


Figure 12. Maximum Rated Forward Biased Safe Operating Area

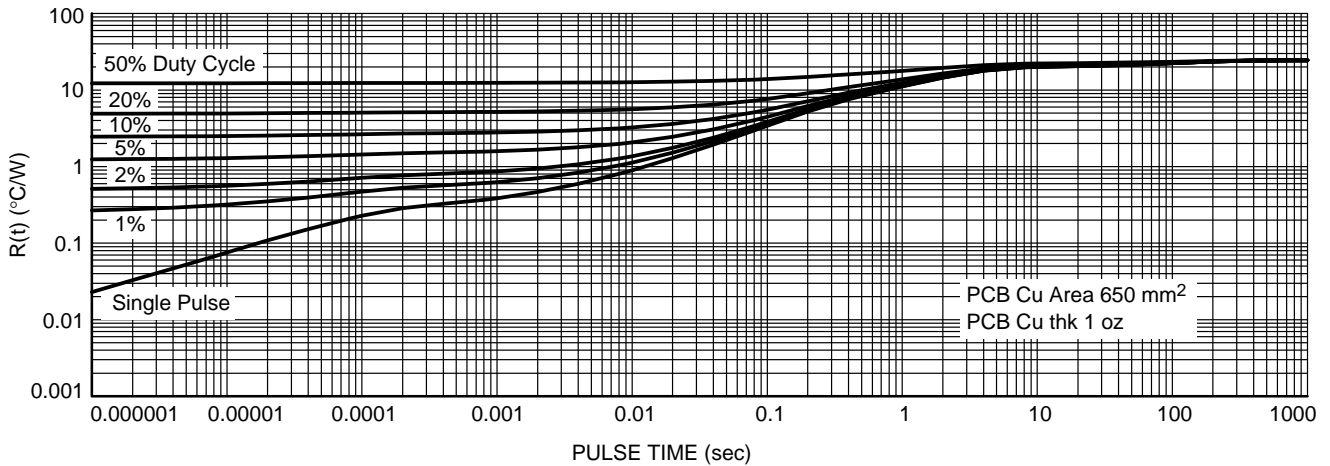


Figure 13. Thermal Characteristics

TYPICAL CHARACTERISTICS – Q2

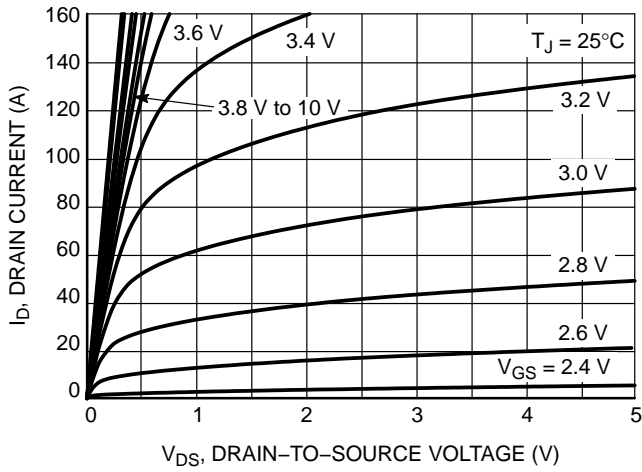


Figure 14. On-Region Characteristics

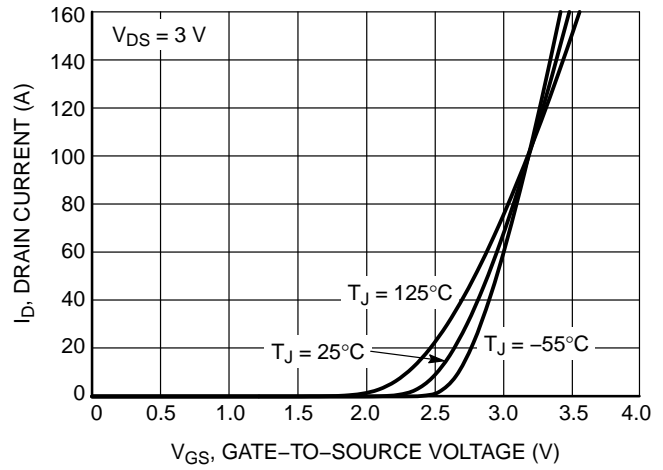


Figure 15. Transfer Characteristics

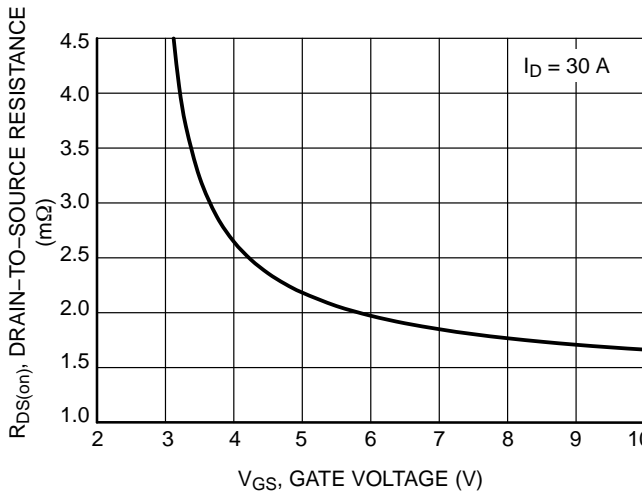


Figure 16. On-Resistance vs. Gate-to-Source Voltage

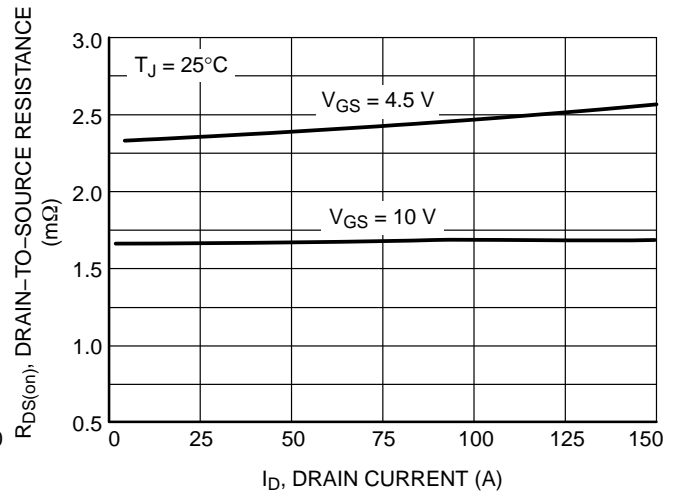


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

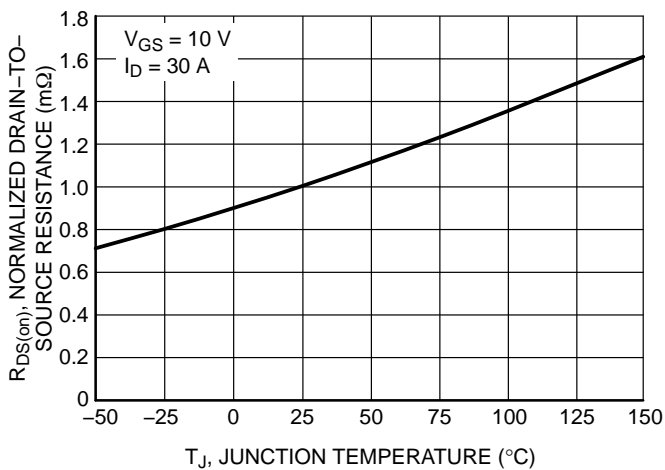


Figure 18. On-Resistance Variation with Temperature

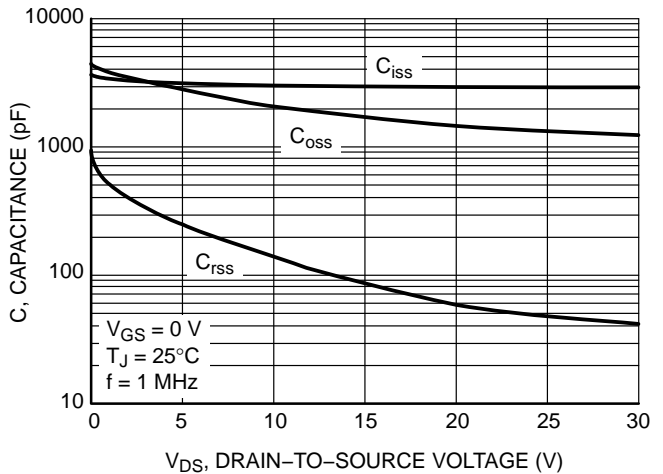


Figure 19. Capacitance Variation

TYPICAL CHARACTERISTICS – Q2

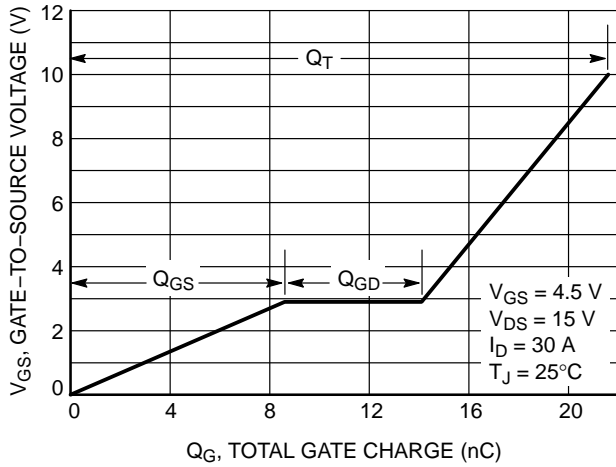


Figure 20. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

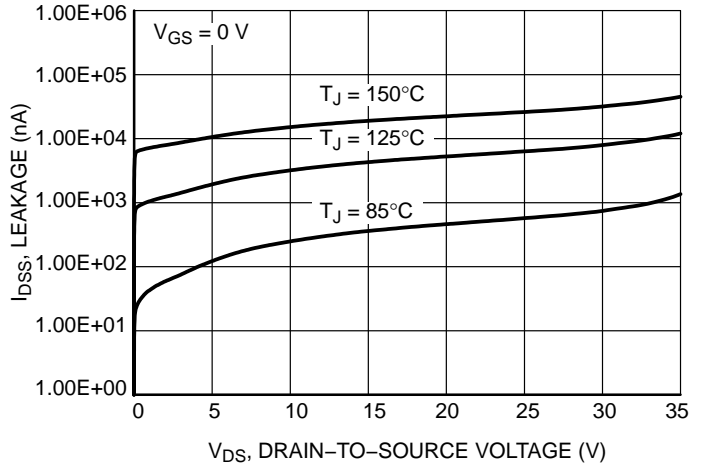


Figure 21. Drain-to-Source Leakage Current vs. Voltage

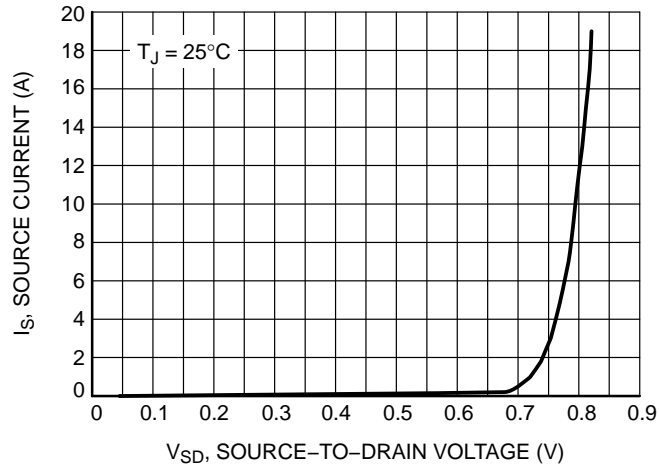


Figure 22. Diode Forward Voltage vs. Current

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TYPICAL CHARACTERISTICS – Q2

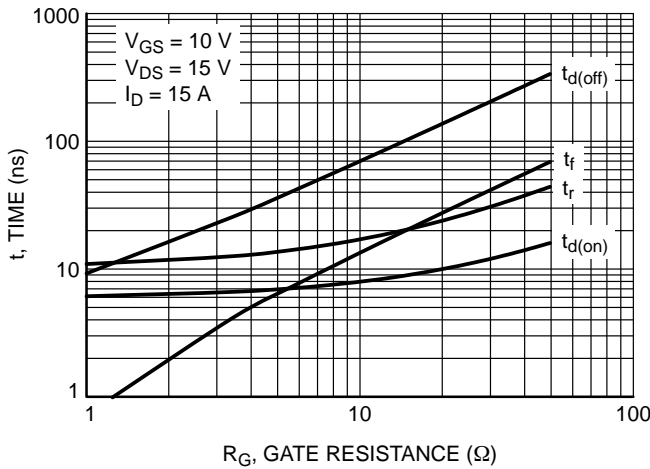


Figure 23. Resistive Switching Time Variation vs. Gate Resistance

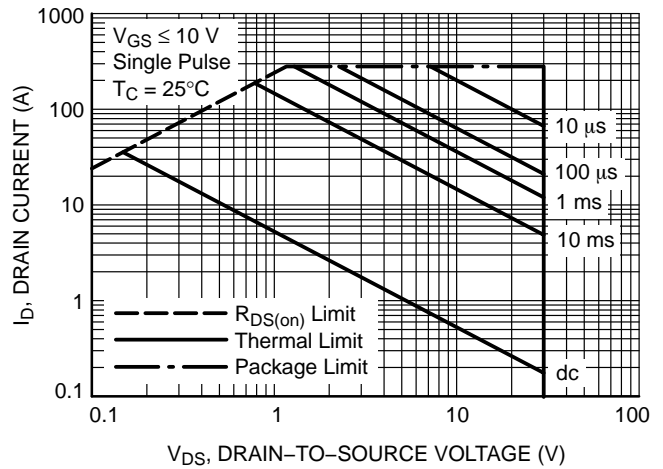


Figure 24. Maximum Rated Forward Biased Safe Operating Area

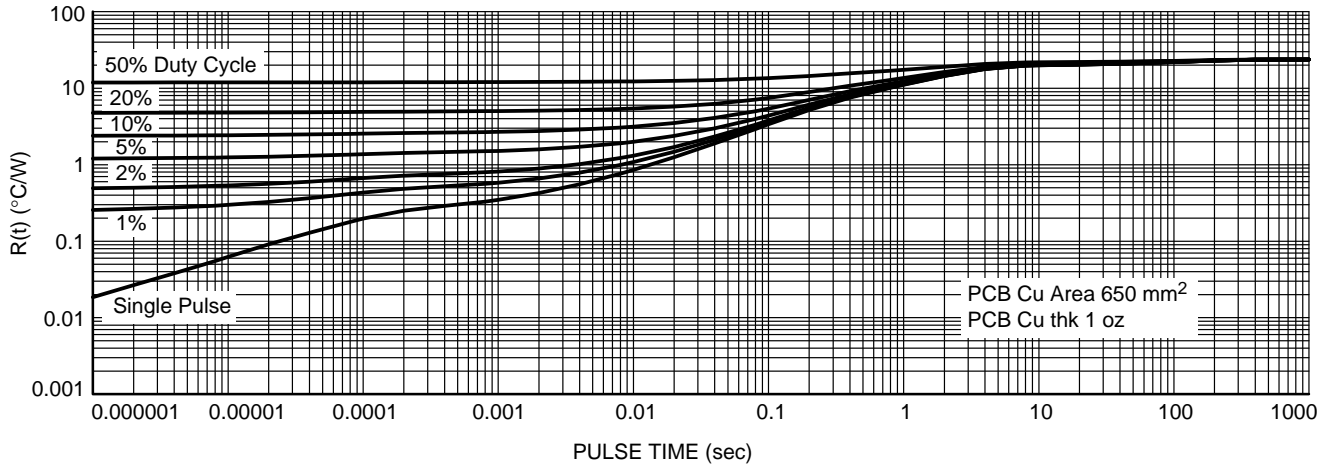


Figure 25. Thermal Characteristics

ORDERING INFORMATION

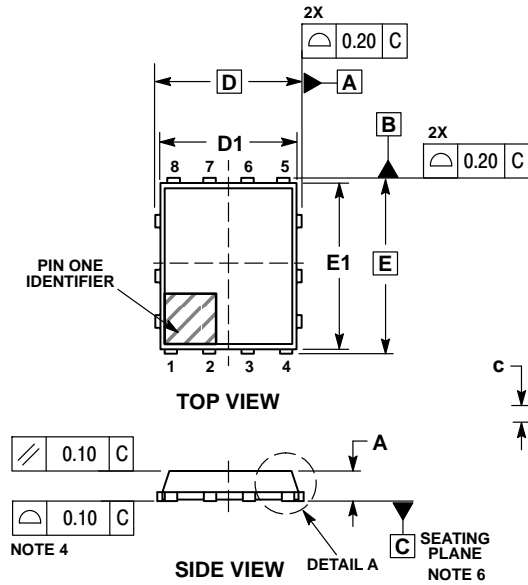
Device	Package	Shipping [†]
NTMFD4C86NT1G	DFN8 (Pb-Free)	1500 / Tape & Reel
NTMFD4C86NT3G	DFN8 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

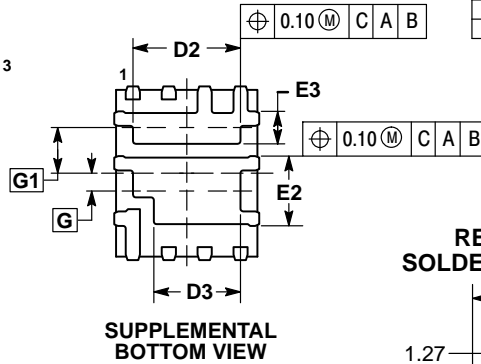
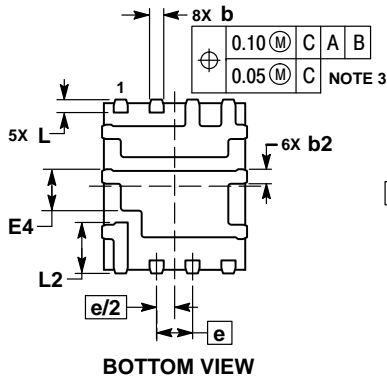
DFN8 5x6, 1.27P PowerPhase FET CASE 506CR ISSUE C



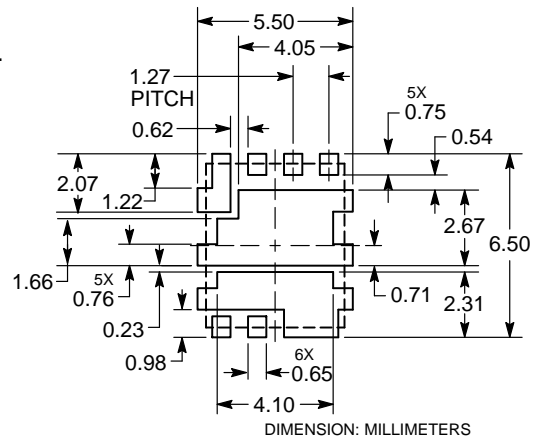
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b AND b1 APPLY TO PLATED TERMINAL AND ARE MEASURED BETWEEN 0.15 AND 0.25 MM FROM THE TIPS.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.


DIM	MILLIMETERS	
	MIN	MAX
A	0.90	1.10
A1	0.00	0.05
b	0.40	0.60
b2	0.40	0.60
c	0.20	0.30
D	5.15 BSC	
D1	4.90	5.10
D2	3.70	3.90
D3	2.96	3.16
E	6.15 BSC	
E1	5.80	6.00
E2	2.37	2.57
E3	1.05	1.25
E4	1.36	1.56
e	1.27 BSC	
G	0.625 BSC	
G1	1.615 BSC	
h	12 °	
L	0.34	0.59
L2	1.68	1.93



RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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