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MOSFET - Power, Dual N- & P-Channel, SO8FL

**100 V, 13.4 mΩ, 60 A,
-100 V, 36 mΩ, -36 A**

NTMFC013NP10M5L

Features

- Small Footprint (5 x 6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- Motor Drive, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$, Unless otherwise specified)

Parameter			Symbol	Q1	Q2	Unit
Drain-to-Source Breakdown Voltage			$V_{(BR)DSS}$	100	-100	V
Gate-to-Source Voltage			V_{GS}	± 20	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Note 2)	Steady State	$T_C = 25^{\circ}\text{C}$	I_D	60	-36	A
Power Dissipation $R_{\theta JC}$ (Note 2)			P_D	102	102	W
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	9	-5	A
Power Dissipation $R_{\theta JA}$ (Notes 1, 2)			P_D	2.7	2.7	W
Pulsed Drain Current	$T_A = 25^{\circ}\text{C}$, $t_p = 10\text{ }\mu\text{s}$		I_{DM}	208	-184	A
Operating Junction and Storage Temperature Range			T_J , T_{stg}	-55 to +150		$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	85	85	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L = 17.9/18.4\text{ A}$, $L = 1\text{ mH}$)			E_{AS}	161	169	mJ
Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			T_L	260	260	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 1 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

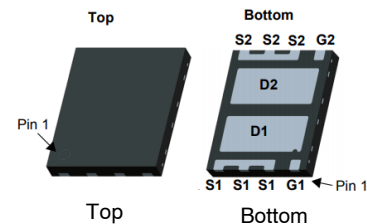
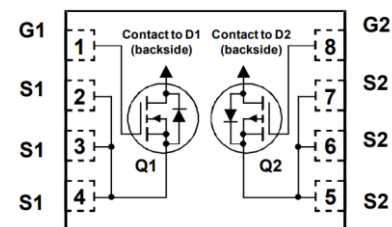


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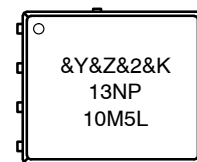
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
100 V	13.4 mΩ @ 10 V	60 A
-100 V	36 mΩ @ 10 V	-36 A

Dual-Channel MOSFET



**WDFN8
CASE 511DC**

MARKING DIAGRAM



&Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&2 = Numeric Date Code
&K = Lot Code
13NP10M5L = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

NTMFC013NP10M5L

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 3)	1.46	1.46	°C/W
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 3)	55	55	

3. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

ELECTRICAL CHARACTERISTICS (Q1, N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = 250\text{ }\mu\text{A}$, ref to 25°C		60		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 158\text{ }\mu\text{A}$	1.0	1.7	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = 158\text{ }\mu\text{A}$, ref to 25°C		8.85		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 8.5\text{ A}$		9.16	13.4	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 6.8\text{ A}$		15.2	35.0	
Forward Transconductance	g_{FS}	$V_{DS} = 5\text{ V}, I_D = 8.5\text{ A}$		15.5		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		1.57		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$		1345		pF
Output Capacitance	C_{OSS}			307		
Reverse Transfer Capacitance	C_{RSS}			17.5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}, I_D = 8.5\text{ A}$		12		nC
Threshold Gate Charge	$Q_{G(TH)}$			2.4		
Gate-to-Source Charge	Q_{GS}			4.7		
Gate-to-Drain Charge	Q_{GD}			5		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DD} = 50\text{ V}, I_D = 8.5\text{ A}$		23		V
Plateau Voltage	V_{GP}			3.3		

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 50\text{ V}, I_D = 8.5\text{ A}, R_G = 6\text{ }\Omega$		12		ns
Rise Time	t_r			8		
Turn-Off Delay Time	$t_{d(OFF)}$			30		
Fall Time	t_f			10		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 50\text{ V}, I_D = 8.5\text{ A}, R_G = 6\text{ }\Omega$		20.1		ns
Rise Time	t_r			40.9		
Turn-Off Delay Time	$t_{d(OFF)}$			22.7		
Fall Time	t_f			16		

NTMFC013NP10M5L

ELECTRICAL CHARACTERISTICS (Q1, N-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}$, $I_S = 8.5\text{ A}$	$T_J = 25^\circ\text{C}$	0.77	1.2	V
			$T_J = 125^\circ\text{C}$	0.63		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}$, $dI_S/dt = 100\text{ A}/\mu\text{s}$, $I_S = 4.2\text{ A}$		39		ns
Charge Time	t_a			22		
Discharge Time	t_b			17		
Reverse Recovery Charge	Q_{RR}			38		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

ELECTRICAL CHARACTERISTICS (Q2, P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}$, $I_D = -250\text{ }\mu\text{A}$	-100			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS} / T_J$	$I_D = -250\text{ }\mu\text{A}$, ref to 25°C		60		mV/ $^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}$, $V_{DS} = -80\text{ V}$	$T_J = 25^\circ\text{C}$		-1	μA
			$T_J = 125^\circ\text{C}$		-100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -158\text{ }\mu\text{A}$	-2.0	-3.31	-4.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)} / T_J$	$I_D = -158\text{ }\mu\text{A}$, ref to 25°C		6.9		mV/ $^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = -8.5\text{ A}$		28.5	36	m Ω
		$V_{GS} = -6\text{ V}$, $I_D = -5.7\text{ A}$		38.3	50.1	
Forward Transconductance	g_{FS}	$V_{DS} = -5\text{ V}$, $I_D = -8.5\text{ A}$		17.7		S
Gate-Resistance	R_G	$T_A = 25^\circ\text{C}$		2.41		Ω

CHARGES & CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$, $V_{DS} = -50\text{ V}$		2443		pF
Output Capacitance	C_{OSS}			330		
Reverse Transfer Capacitance	C_{RSS}			15		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -8.5\text{ A}$		30		nC
Threshold Gate Charge	$Q_{G(TH)}$			6.9		
Gate-to-Source Charge	Q_{GS}			10.4		
Gate-to-Drain Charge	Q_{GD}			5.1		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -6\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -8.5\text{ A}$		18.4		
Plateau Voltage	V_{GP}			5		V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}$, $V_{DS} = -50\text{ V}$, $I_D = -8.5\text{ A}$, $R_G = 6\text{ }\Omega$		12.4		ns
Rise Time	t_r			16.1		
Turn-Off Delay Time	$t_{d(OFF)}$			20		
Fall Time	t_f			24		

NTMFC013NP10M5L

ELECTRICAL CHARACTERISTICS (Q2, P-CHANNEL) ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -6\text{ V}, V_{DS} = -50\text{ V}, I_D = -8.5\text{ A},$ $R_G = 6\ \Omega$		27		ns
Rise Time	t_r			25		
Turn-Off Delay Time	$t_{d(OFF)}$			22		
Fall Time	t_f			8.5		

OFF CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -8.5 A	T _J = 25°C		-0.84	-1.2	V
			T _J = 125°C		0.7		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = -4.2 A			39		ns
Charge Time	t _a				23		
Discharge Time	t _b				16.6		
Reverse Recovery Charge	Q _{RR}				38		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS – N-CHANNEL

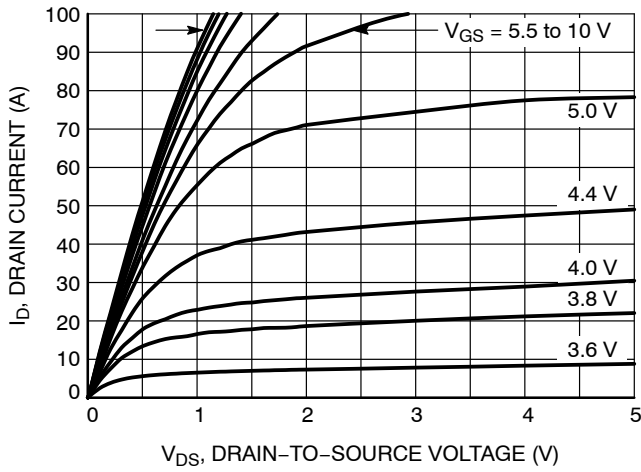


Figure 1. On-Region Characteristics

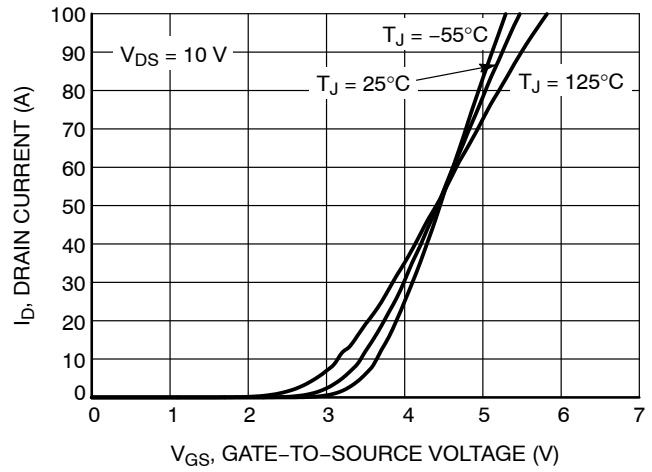


Figure 2. Transfer Characteristics

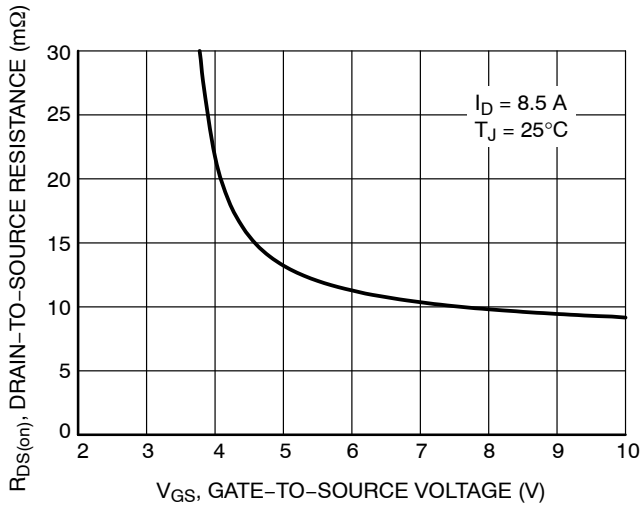


Figure 3. On-Resistance vs. Gate-to-Source Voltage

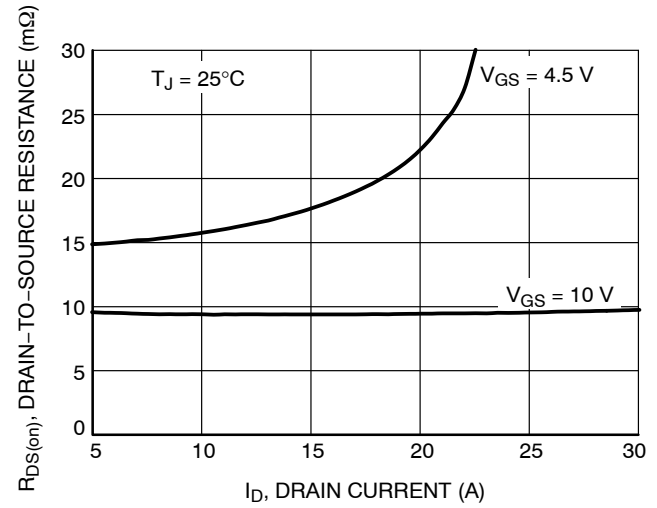


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

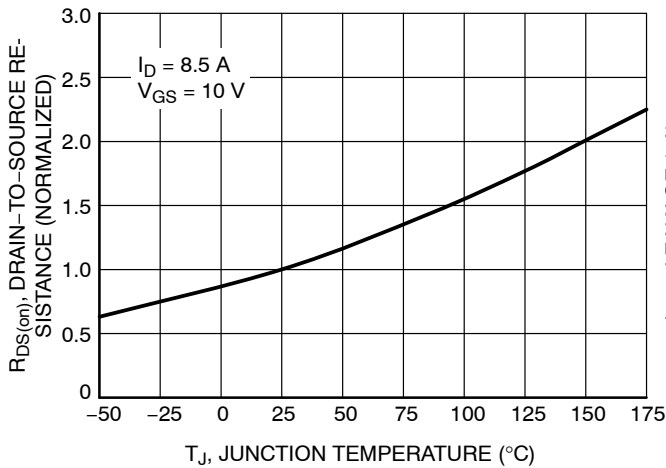


Figure 5. On-Resistance Variation with Temperature

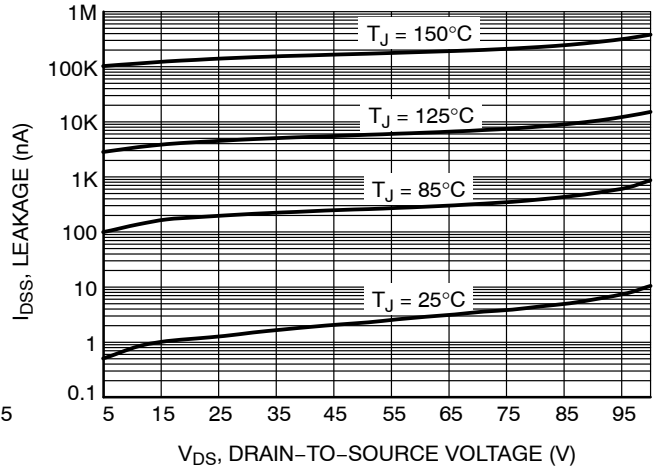


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – N-CHANNEL

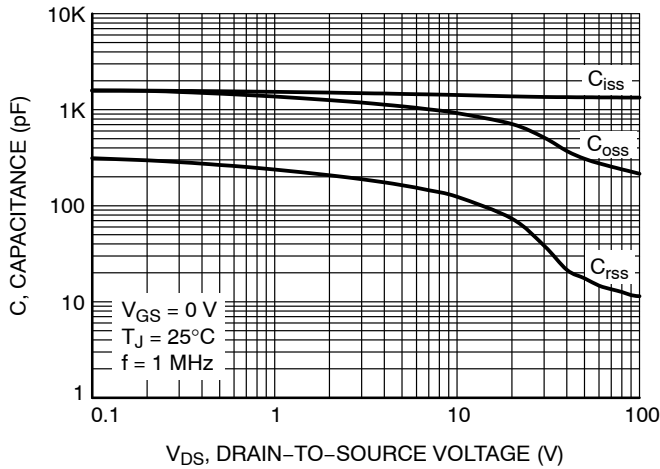


Figure 7. Capacitance Variation

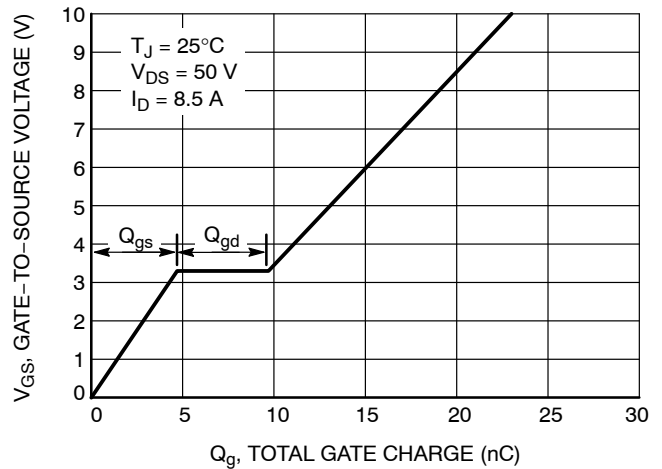


Figure 8. Gate-to-Source vs. Total Charge

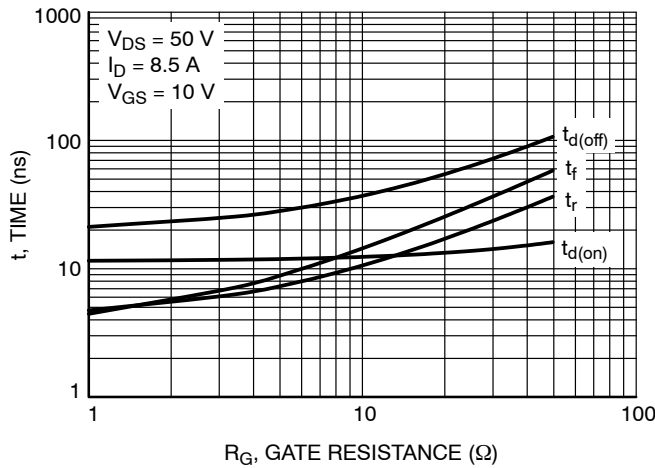


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

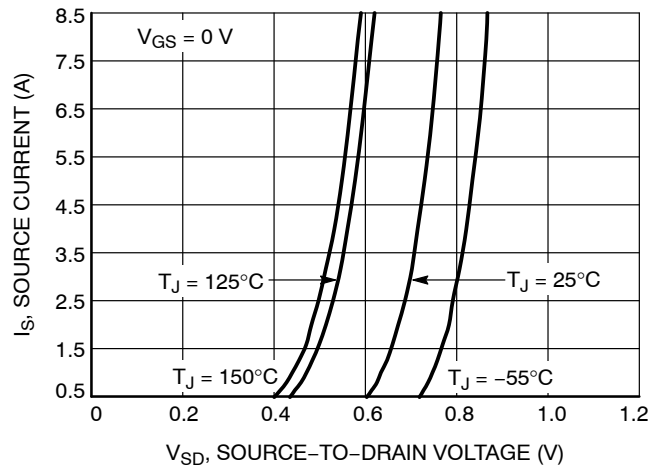


Figure 10. Diode Forward Voltage vs. Current

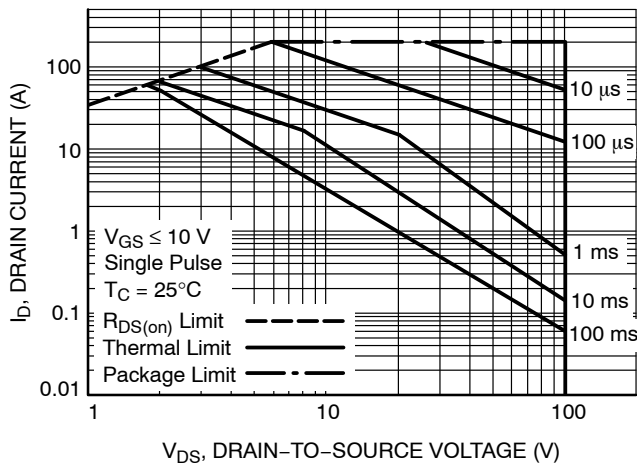


Figure 11. Maximum Rated Forward Biased Safe Operating Area

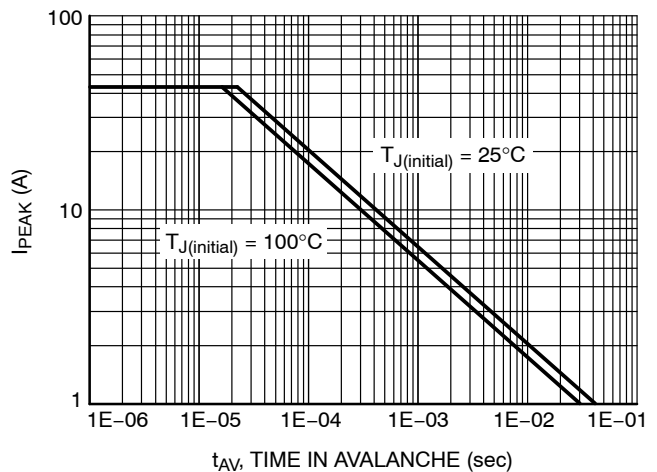


Figure 12. Maximum Drain Current vs. Time in Avalanche

NTMFC013NP10M5L

TYPICAL CHARACTERISTICS – N-CHANNEL

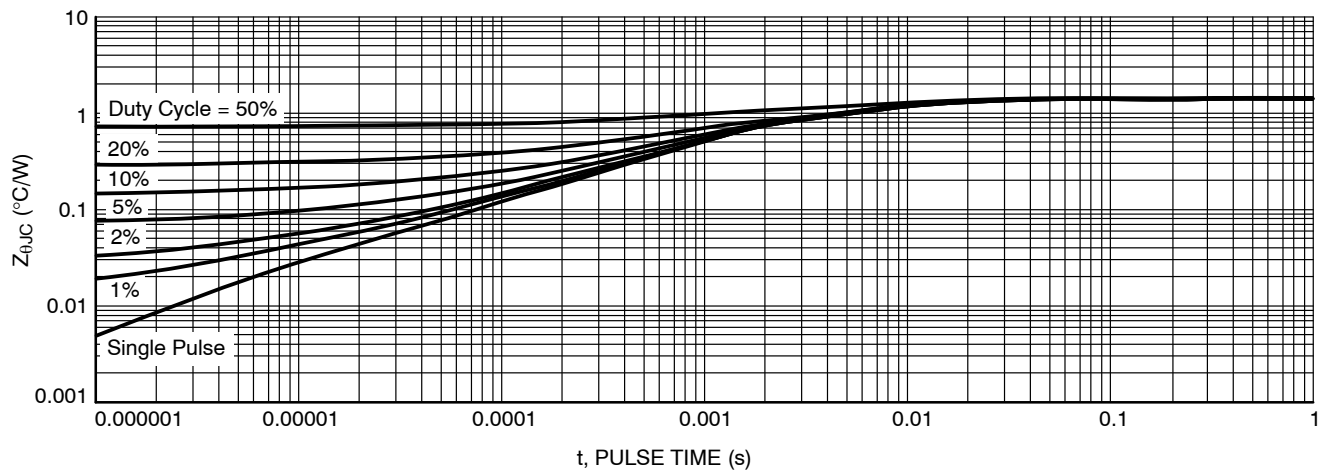


Figure 13. Thermal Response

TYPICAL CHARACTERISTICS – P-CHANNEL

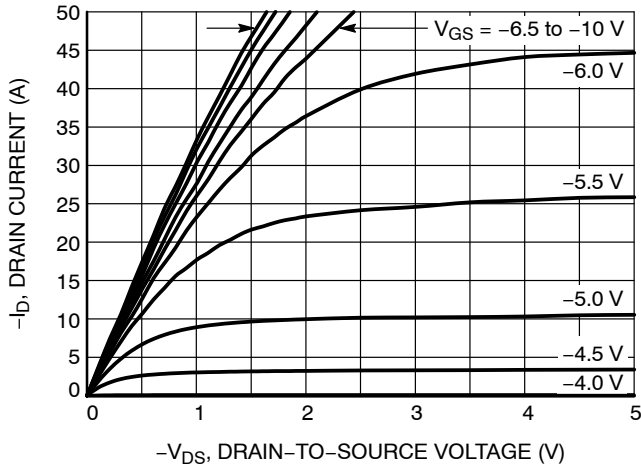


Figure 14. On-Region Characteristics

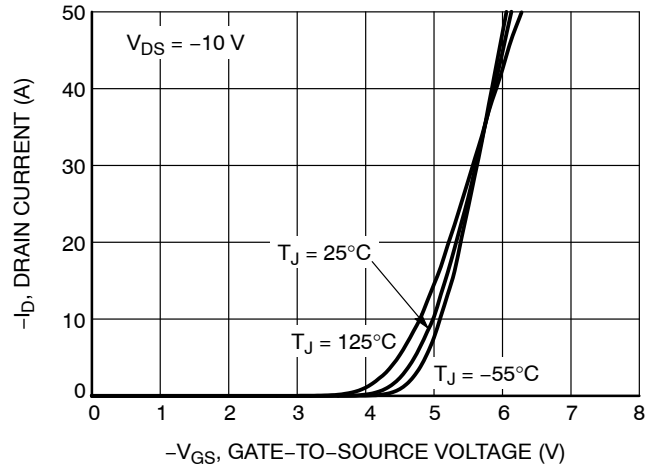


Figure 15. Transfer Characteristics

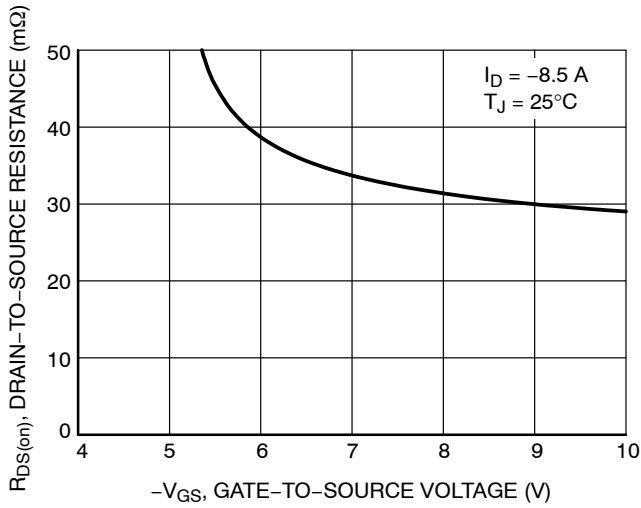


Figure 16. On-Resistance vs. Gate-to-Source Voltage

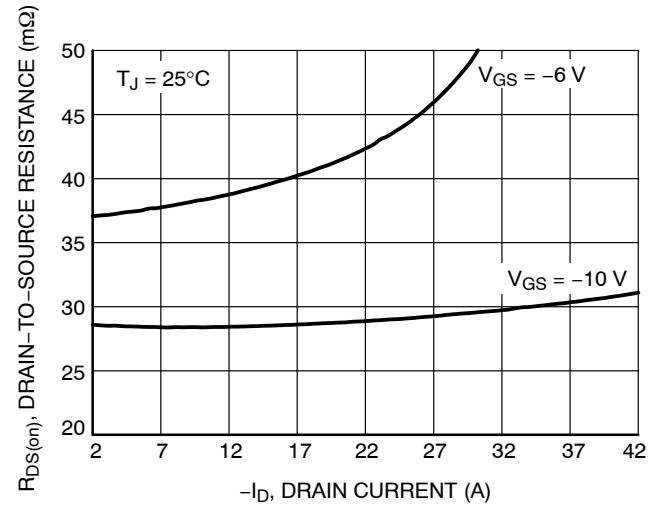


Figure 17. On-Resistance vs. Drain Current and Gate Voltage

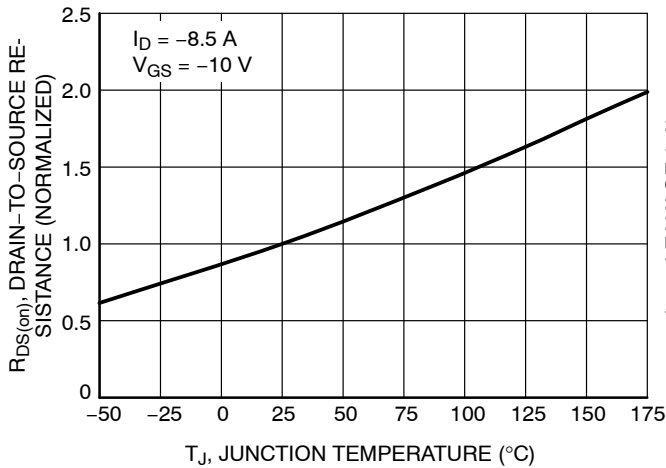


Figure 18. On-Resistance Variation with Temperature

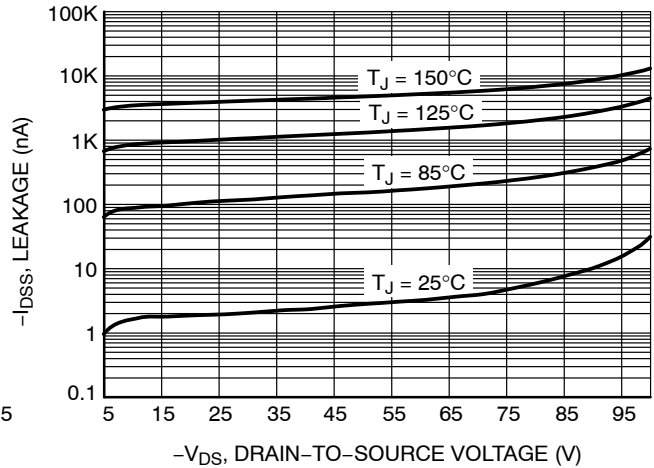


Figure 19. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS – P-CHANNEL

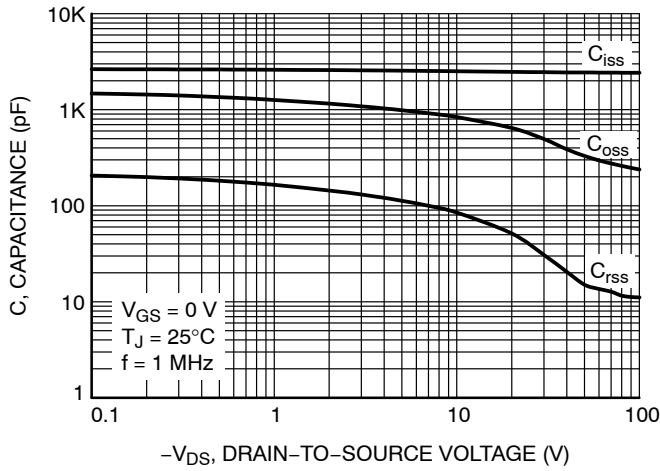


Figure 20. Capacitance Variation

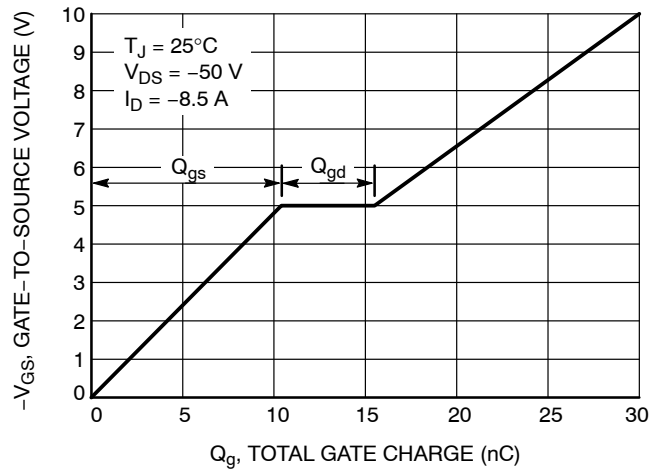


Figure 21. Gate-to-Source vs. Total Charge

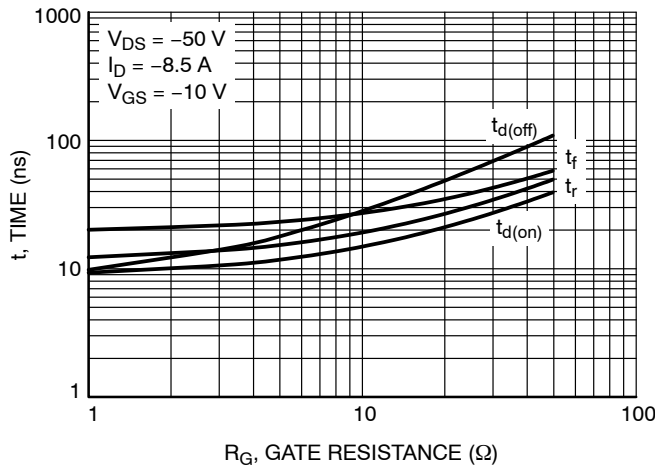


Figure 22. Resistive Switching Time Variation vs. Gate Resistance

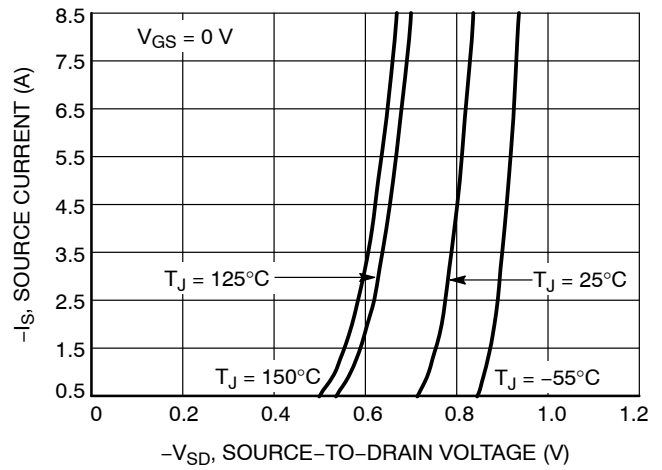


Figure 23. Diode Forward Voltage vs. Current

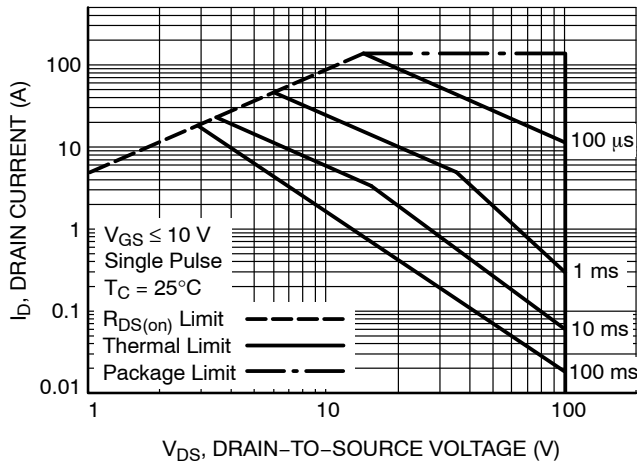


Figure 24. Maximum Rated Forward Biased Safe Operating Area

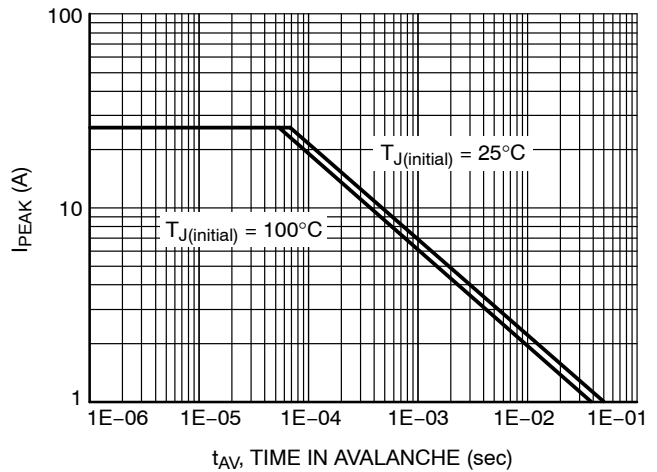


Figure 25. Maximum Drain Current vs. Time in Avalanche

NTMFC013NP10M5L

TYPICAL CHARACTERISTICS – P-CHANNEL

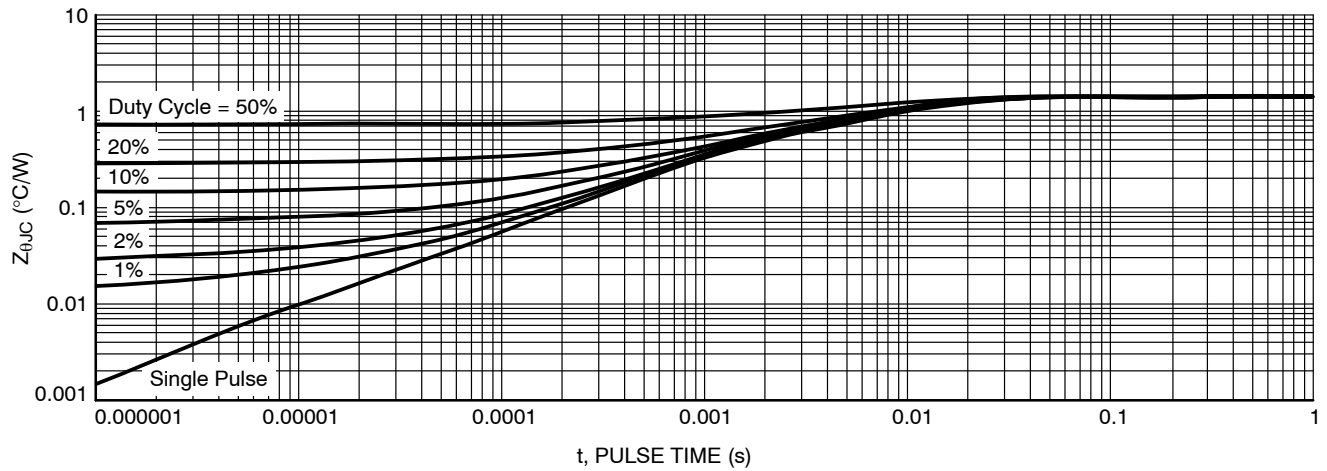


Figure 26. Thermal Response

ORDERING INFORMATION

Device	Device Marking	Package	Shipping (Qty / Packing) [†]
NTMFC013NP10M5L	13NP10M5L	SO8FL (Pb-Free/Halogen Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

[illegible]

The diagram illustrates the Recommended Land Pattern, showing a cross-section of a stepped embankment. The pattern consists of a central rectangular area with a cross-hatched texture, flanked by stepped sections on both sides. The dimensions and labels are as follows:


- Top Section:**
 - Overall width: 4.41 (2X)
 - Width of the central rectangular area: 4.10 (2X)
 - Width of the stepped section on the right: 0.67 (6X)
 - Height of the stepped section on the right: 8
 - Height of the stepped section on the left: 7
 - Height of the central rectangular area: 6
 - Height of the stepped section on the left: 5
- Middle Section:**
 - Height of the central rectangular area: 1.75 (2X)
 - Height of the stepped section on the right: 0.50
 - Height of the stepped section on the left: 1.15 (2X)
 - Height of the central rectangular area: 2.26
- Bottom Section:**
 - Height of the central rectangular area: 0.50 (2X)
 - Height of the stepped section on the right: 0.65 (8X)
 - Height of the stepped section on the left: 0.60 (8X)
 - Height of the central rectangular area: 1.27
 - Height of the stepped section on the right: 0.635
 - Height of the stepped section on the left: 8X
- Overall Dimensions:**
 - Overall height: 6.30

The diagram is labeled "RECOMMENDED LAND PATTERN" at the bottom.

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

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