

# NTHS4101P

## MOSFET – Power, P-Channel, ChipFET -20 V, 6.7 A

### Features

- Offers an Ultra Low  $R_{DS(on)}$  Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP-6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low  $R_{DS(on)}$  at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb-Free Package is Available

### Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	-20	$V_{dc}$
Gate-to-Source Voltage – Continuous	$V_{GS}$	$\pm 8.0$	$V_{dc}$
Drain Current – Continuous – 5 seconds	$I_D$ $I_D$	-4.8 -6.7	A
Total Power Dissipation Continuous @ $T_A = 25^\circ\text{C}$ (5 sec) @ $T_A = 25^\circ\text{C}$ Continuous @ $85^\circ\text{C}$ (5 sec) @ $85^\circ\text{C}$	$P_D$	1.3 2.5 0.7 1.3	W
Pulsed Drain Current – $t_p = 10 \mu\text{s}$	$I_{DM}$	-190	A
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Continuous Source Current	$I_S$	-4.8	A
Thermal Resistance (Note 1) Junction-to-Ambient, 5 sec Junction-to-Ambient, Continuous	$R_{\theta JA}$ $R_{\theta JA}$	50 95	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	$T_L$	260	$^\circ\text{C}$

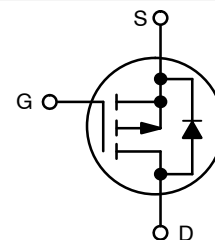
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



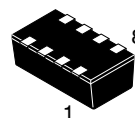
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$V_{(BR)DS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
-20 V	21 m $\Omega$ @ -4.5 V	-6.7 A
	30 m $\Omega$ @ -2.5 V	
	42 m $\Omega$ @ -1.8 V	

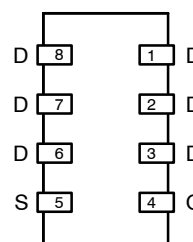


P-Channel MOSFET

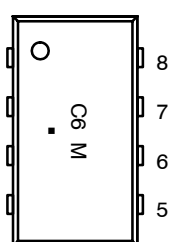


ChipFET  
CASE 1206A  
STYLE 1

### PIN CONNECTIONS



### MARKING DIAGRAM



C6 = Specific Device Code  
M = Month Code  
■ = Pb-Free Package

### ORDERING INFORMATION

Device	Package	Shipping†
NTHS4101PT1	ChipFET	3000 Tape / Reel
NTHS4101PT1G	ChipFET (Pb-free)	3000 Tape / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## **NTHS4101P**

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

# NTHS4101P

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	V <sub>(Br)DSS</sub>	V <sub>GS</sub> = 0 V <sub>dc</sub> , I <sub>D</sub> = -250 μA <sub>dc</sub>	-20			V <sub>dc</sub>
Gate-Body Leakage Current Zero	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V <sub>dc</sub> , V <sub>GS</sub> = ± 8.0 V <sub>dc</sub>			± 100	nA <sub>dc</sub>
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -16 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> V <sub>DS</sub> = -16 V <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub> , T <sub>J</sub> = 85°C			-1.0 -5.0	μA <sub>dc</sub>

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = -250 μA <sub>dc</sub>	-0.45		-1.5	V <sub>dc</sub>
Static Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V <sub>dc</sub> , I <sub>D</sub> = -4.8 A <sub>dc</sub> V <sub>GS</sub> = -2.5 V <sub>dc</sub> , I <sub>D</sub> = -4.2 A <sub>dc</sub> V <sub>GS</sub> = -1.8 V <sub>dc</sub> , I <sub>D</sub> = -1.0 A <sub>dc</sub>		21 30 42	34 40 52	mΩ
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = -5.0 V <sub>dc</sub> , I <sub>D</sub> = -4.8 A <sub>dc</sub>		15		S
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = -4.8 A <sub>dc</sub> , V <sub>GS</sub> = 0 V <sub>dc</sub>		-0.8	-1.2	V

### DYNAMIC CHARACTERISTICS

Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -16 V <sub>dc</sub> V <sub>GS</sub> = 0 V f = 1.0 MHz		2100		pF
Output Capacitance	C <sub>oss</sub>			290		
Transfer Capacitance	C <sub>rss</sub>			200		

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -16 V <sub>dc</sub> V <sub>GS</sub> = -4.5 V <sub>dc</sub> I <sub>D</sub> = -4.5 A <sub>dc</sub> R <sub>G</sub> = 2.5 Ω		8.0		ns
Rise Time	t <sub>r</sub>			28		
Turn-Off Delay Time	t <sub>d(off)</sub>			75		
Fall Time	t <sub>f</sub>			60		
Gate Charge	Q <sub>g</sub>	V <sub>GS</sub> = -4.5 V <sub>dc</sub> I <sub>D</sub> = -4.5 A <sub>dc</sub> V <sub>DS</sub> = -16 V <sub>dc</sub> (Note 3)		25	35	nC
	Q <sub>gs</sub>			4.0		
	Q <sub>gd</sub>			7.0		

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

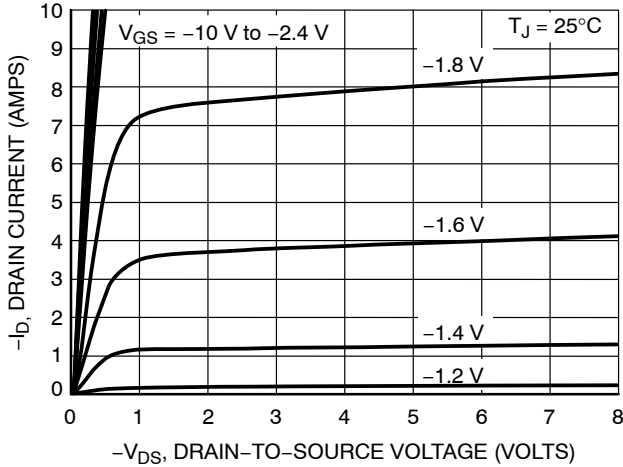


Figure 1. On-Region Characteristics

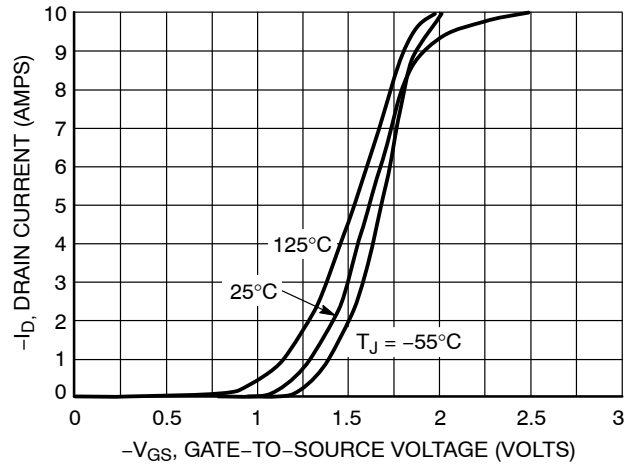


Figure 2. Transfer Characteristics

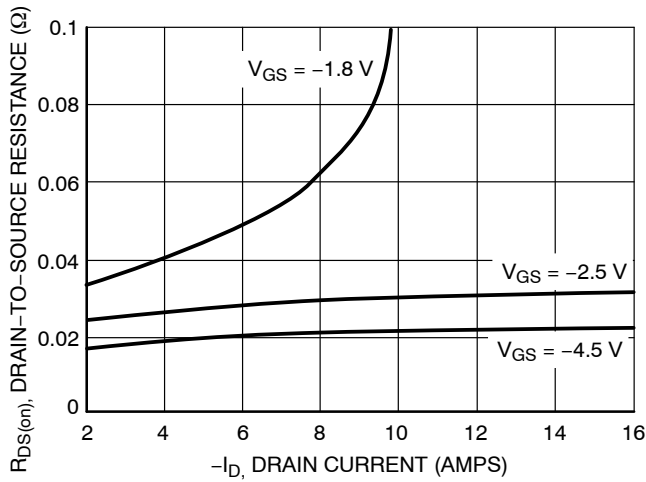


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

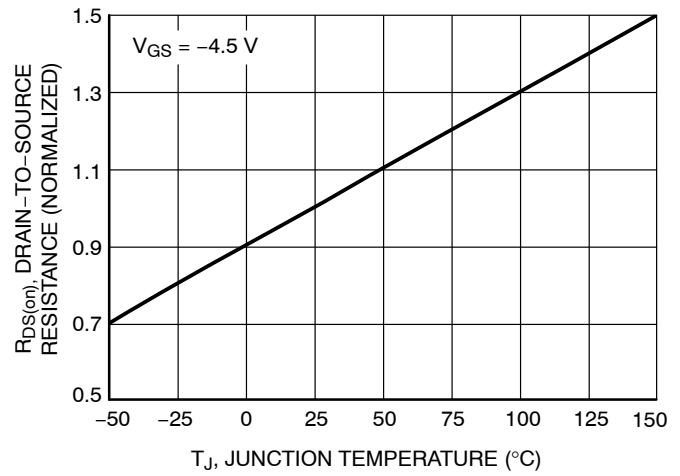


Figure 4. On-Resistance Variation with Temperature

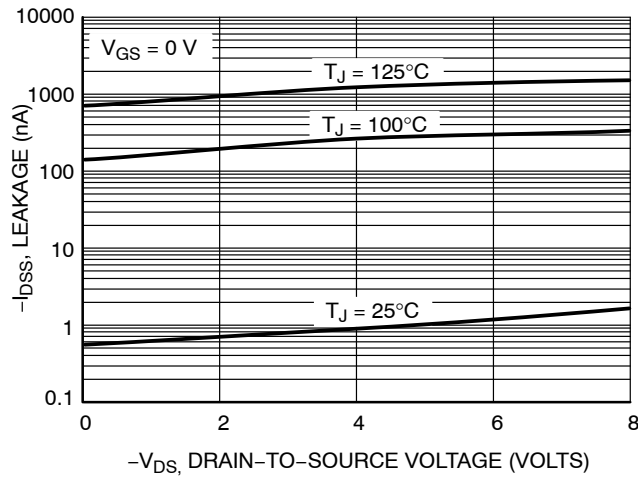
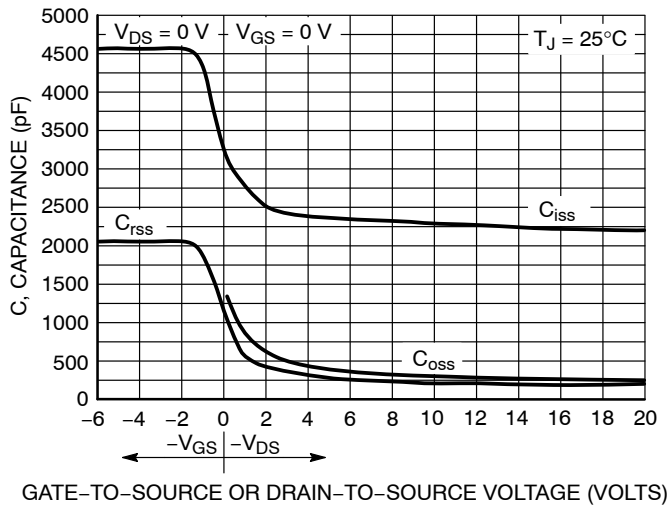
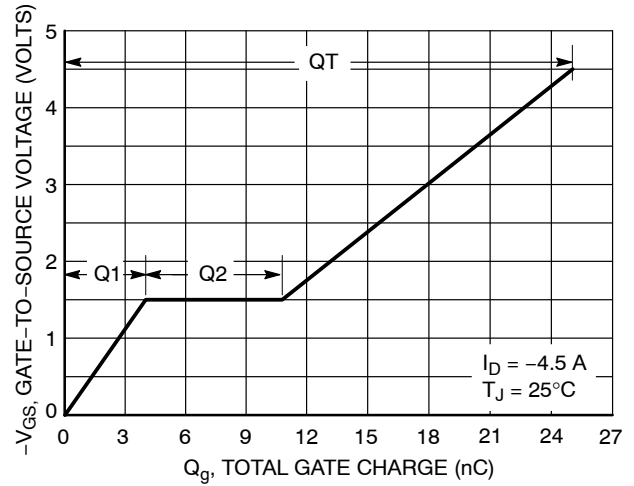


Figure 5. Drain-to-Source Leakage Current vs. Voltage

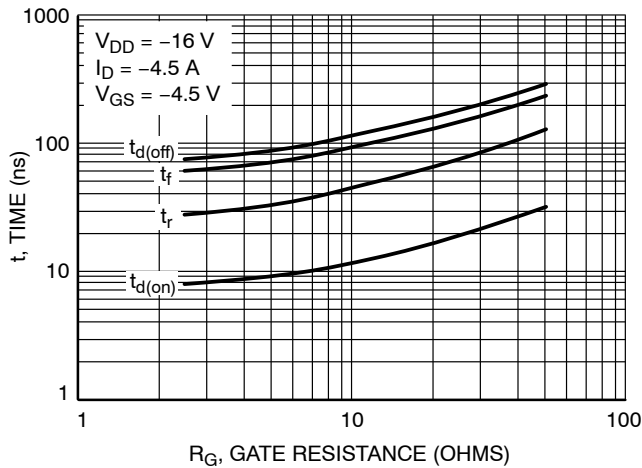
**TYPICAL PERFORMANCE CURVES** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)



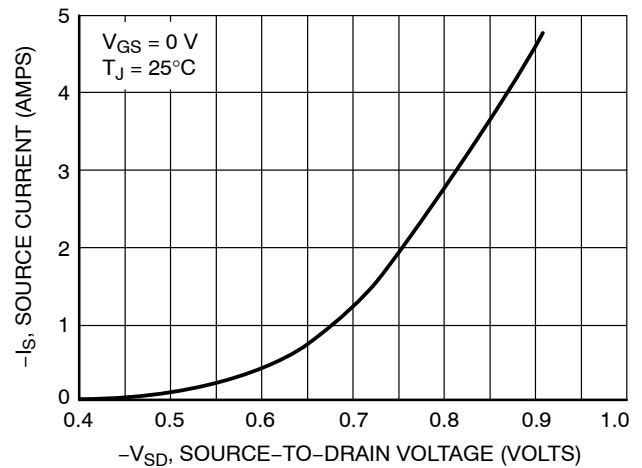
**Figure 6. Capacitance Variation**



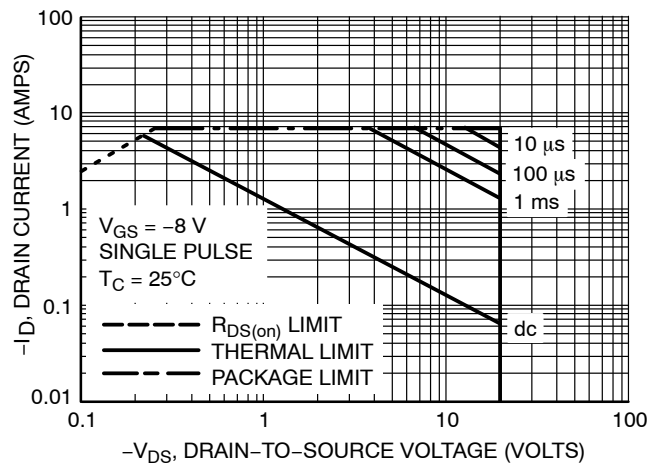
**Figure 7. Gate-to-Source and Drain-to-Source Voltage vs. Total Gate Charge**



**Figure 8. Resistive Switching Time Variation vs. Gate Resistance**



**Figure 9. Diode Forward Voltage vs. Current**



**Figure 10. Maximum Rated Forward Biased Safe Operating Area**

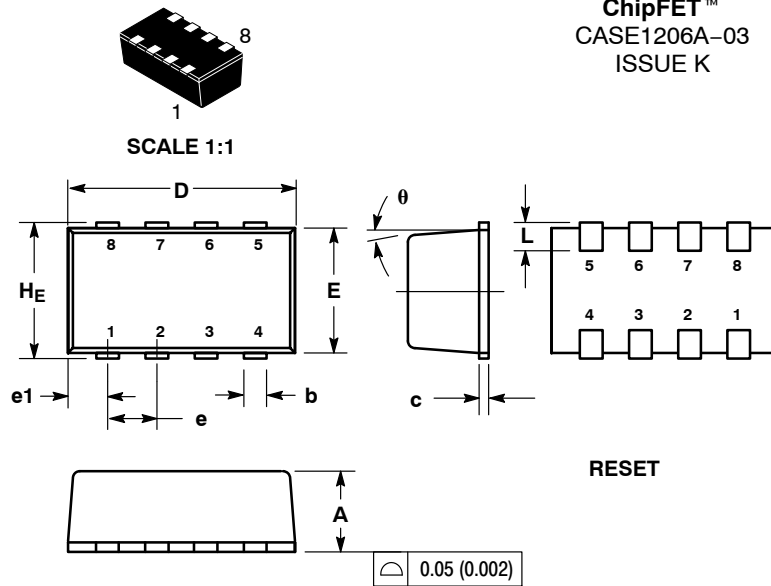
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

ON

ChipFET™  
CASE1206A-03  
ISSUE K

DATE 19 MAY 2009



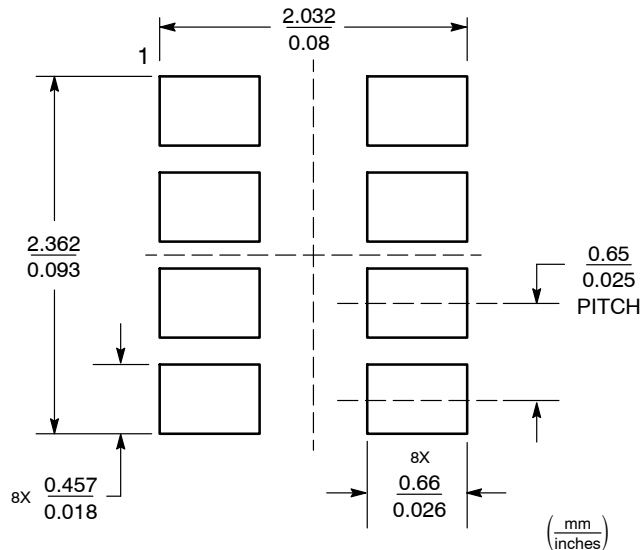
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

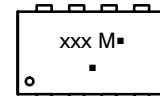
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
He	1.80	1.90	2.00	0.071	0.075	0.079
theta	5° NOM			5° NOM		

STYLE 1: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 2: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 3: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. COLLECTOR 4. BASE 5. EMITTER 6. COLLECTOR 7. COLLECTOR 8. COLLECTOR	STYLE 5: PIN 1. ANODE 2. ANODE 3. DRAIN 4. DRAIN 5. SOURCE 6. GATE 7. CATHODE 8. CATHODE	STYLE 6: PIN 1. ANODE 2. DRAIN 3. DRAIN 4. GATE 5. SOURCE 6. DRAIN 7. DRAIN 8. CATHODE / DRAIN
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## SOLDERING FOOTPRINT



## GENERIC MARKING DIAGRAM\*



xxx = Specific Device Code  
M = Month Code  
▪ = Pb-Free Package  
(Note: Microdot may be in either location)

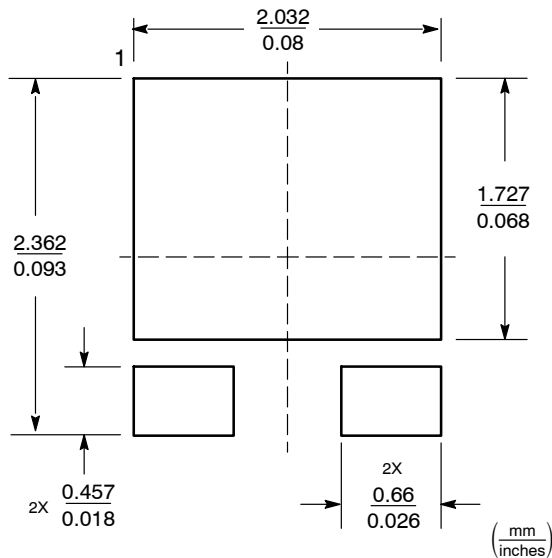
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

## OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

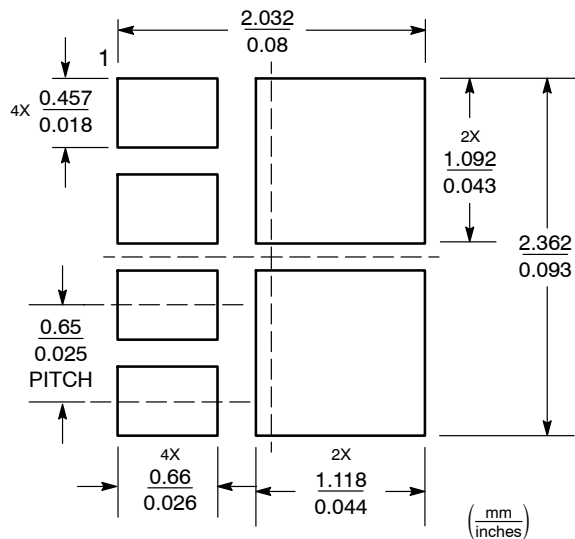
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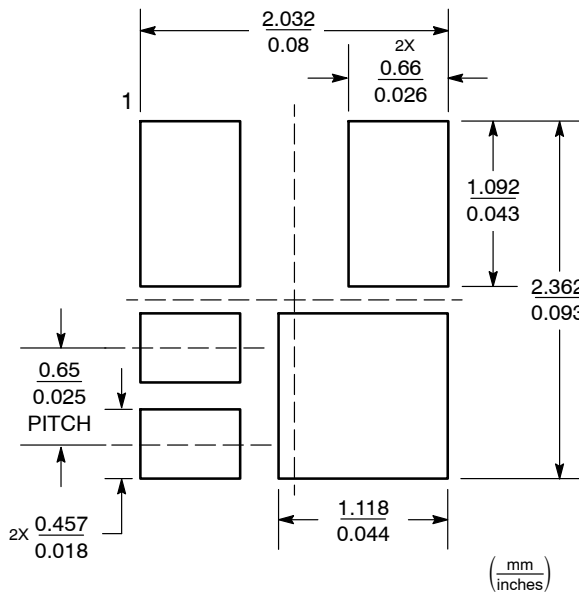
ADDITIONAL SOLDERING FOOTPRINTS\*



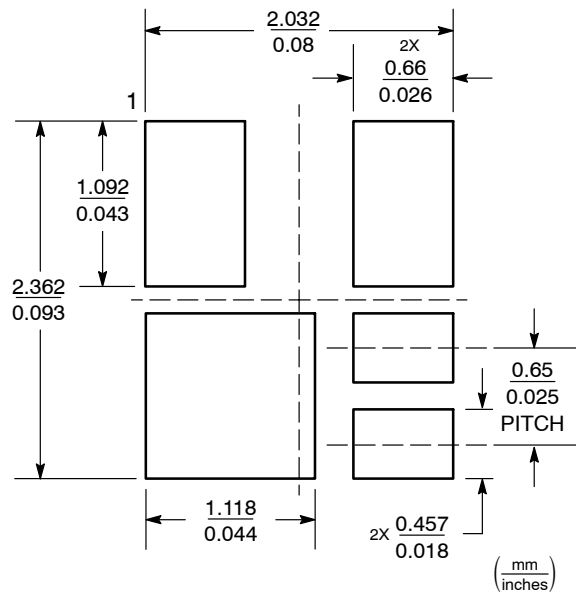
Styles 1 and 4



Style 2




Style 3



Style 5

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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