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Silicon Carbide (SiC) MOSFET - EliteSiC, 23 mohm, 650 V, M3S, TO-247-3L NTHL023N065M3S

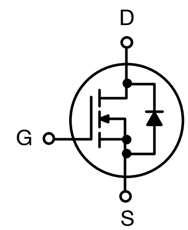
$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX
650 V	23 mΩ @ V_{GS} = 18 V	40 A

Features

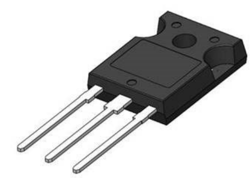
- Typical $R_{DS(on)}$ = 23 mΩ @ V_{GS} = 18 V
- Ultra Low Gate Charge ($Q_{G(tot)}$ = 69 nC)
- High Speed Switching with Low Capacitance (C_{oss} = 153 pF)
- 100% Avalanche Tested
- This Device is Halide Free and RoHS Compliant with Exemption 7a, Pb−Free 2LI (on second level interconnection)

Applications

- SMPS, Solar Inverters, UPS, Energy Storages, EV Charging Infrastructure



N−CHANNEL MOSFET



TO−247−3LD
CASE 340CX

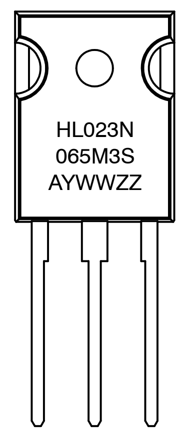
MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain−to−Source Voltage		V_{DSS}	650	V
Gate−to−Source Voltage		V_{GS}	−8/+22	V
Continuous Drain Current (Note 1)	T_C = 25°C	I_D	40	A
Power Dissipation		P_D	263	W
Continuous Drain Current (Note 2)	T_C = 100°C	I_D	40	A
Power Dissipation		P_D	131	W
Pulsed Drain Current (Note 3)	T_C = 25°C t_p = 100 µs	I_{DM}	218	A
Continuous Source−Drain Current (Body Diode)	T_C = 25°C V_{GS} = −3 V	I_S	40	A
	T_C = 100°C V_{GS} = −3 V		25	
Pulsed Source−Drain Current (Body Diode) (Note 3)	T_C = 25°C V_{GS} = −3 V t_p = 100 µs	I_{SM}	162	A
Single Pulse Avalanche Energy (Note 4)	I_{LPK} = 19.6 A, L = 1 mH	E_{AS}	192	mJ
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +175	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 seconds)		T_L	270	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 40 A is limited by package. Power chip max drain current is 70 A if limited by max junction temperature.
2. 40 A is limited by package. Power chip max drain current is 49 A if limited by max junction temperature.
3. Repetitive rating, limited by max junction temperature.
4. E_{AS} of 192 mJ is based on starting T_J = 25°C, L = 1 mH, I_{AS} = 19.6 A, V_{DD} = 100 V, V_{GS} = 18 V

MARKING DIAGRAM



HL023N065M3S = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping
NTHL023N065M3S	TO−247−3L	30 Units / Tube

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THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction−to−Case (Note 5)	$R_{\theta JC}$	0.57	°C/W
Thermal Resistance, Junction−to−Ambient (Note 5)	$R_{\theta JA}$	40	

5. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Operation Values of Gate−to−Source Voltage	V_{GSop}	−5...−3 +18	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650	–	–	V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D = 1 mA, Referenced to 25°C	–	89	–	mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 650 V, T_J = 25°C	–	–	10	μA
		V_{DS} = 650 V, T_J = 175°C (Note 7)	–	–	500	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{GS} = −8/+22 V, V_{DS} = 0 V	–	–	±1.0	μA
ON CHARACTERISTICS						
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 18 V, I_D = 20 A, T_J = 25°C	–	23	33	mΩ
		V_{GS} = 18 V, I_D = 20 A, T_J = 175°C (Note 7)	–	35	–	
		V_{GS} = 15 V, I_D = 20 A, T_J = 25°C	–	29	–	
		V_{GS} = 15 V, I_D = 20 A, T_J = 175°C (Note 7)	–	37	–	
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 10 mA, T_J = 25°C	2	2.8	4	V
Forward Transconductance	g_{FS}	V_{DS} = 10 V, I_D = 20 A (Note 7)	–	14	–	S
CHARGES, CAPACITANCES & GATE RESISTANCE						
Input Capacitance	C_{ISS}	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz (Note 7)	–	1952	–	pF
Output Capacitance	C_{OSS}		–	153	–	
Reverse Transfer Capacitance	C_{RSS}		–	13	–	
Total Gate Charge	$Q_{G(TOT)}$	V_{DD} = 400 V, I_D = 20 A, V_{GS} = −3/18 V (Note 7)	–	69	–	nC
Gate−to−Source Charge	Q_{GS}		–	19	–	
Gate−to−Drain Charge	Q_{GD}		–	18	–	
Gate Resistance	R_G	f = 1 MHz	–	4.0	–	Ω
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, T_J = 25°C (Notes 6 and 7)	–	12	–	ns
Turn−Off Delay Time	$t_{d(OFF)}$		–	38	–	
Rise Time	t_r		–	30	–	
Fall Time	t_f		–	11	–	
Turn−On Switching Loss	E_{ON}		–	174	–	μJ
Turn−Off Switching Loss	E_{OFF}		–	44	–	
Total Switching Loss	E_{TOT}		–	218	–	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = −3/18 V, V_{DD} = 400 V, I_D = 20 A, R_G = 4.7 Ω, T_J = 175°C (Notes 6 and 7)	–	11	–	ns
Turn−Off Delay Time	$t_{d(OFF)}$		–	45	–	
Rise Time	t_r		–	29	–	
Fall Time	t_f		–	14	–	
Turn−On Switching Loss	E_{ON}		–	173	–	μJ
Turn−Off Switching Loss	E_{OFF}		–	64	–	
Total Switching Loss	E_{TOT}		–	237	–	
SOURCE−TO−DRAIN DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	I_{SD} = 20 A, V_{GS} = −3 V, T_J = 25°C	–	3.9	6.0	V
		I_{SD} = 20 A, V_{GS} = −3 V, T_J = 175°C (Note 7)	–	3.6	–	
Reverse Recovery Time	t_{RR}	V_{GS} = −3 V, I_S = 20 A, dI/dt = 1000 A/μs, V_{DS} = 400 V, T_J = 25°C (Note 7)	–	20	–	ns
Charge Time	t_a		–	11	–	
Discharge Time	t_b		–	9	–	
Reverse Recovery Charge	Q_{RR}		–	95	–	nC
Reverse Recovery Energy	E_{REC}		–	6.9	–	μJ
Peak Reverse Recovery Current	I_{RRM}		–	9.8	–	A

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. EON/EOFF result is with body diode.
7. Defined by design, not subject to production test.

TYPICAL CHARACTERISTICS

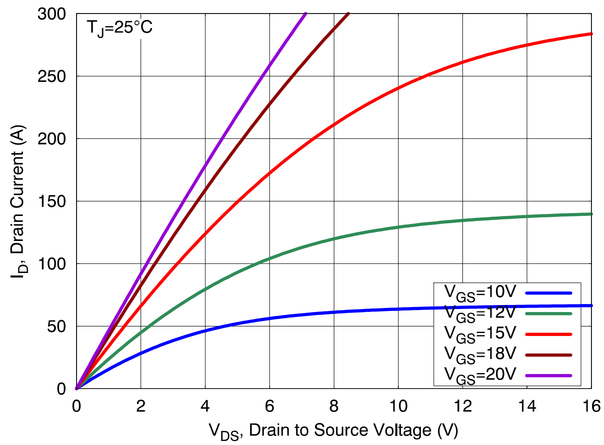


Figure 1. Output Characteristics

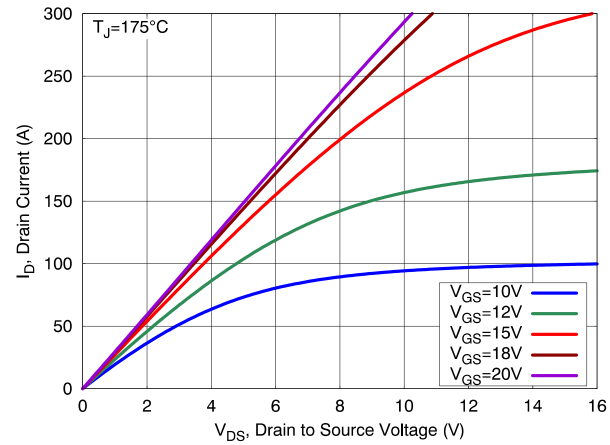


Figure 2. Output Characteristics

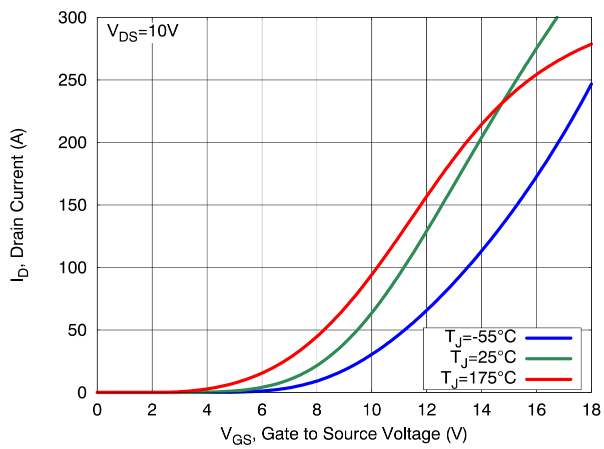


Figure 3. Transfer Characteristics

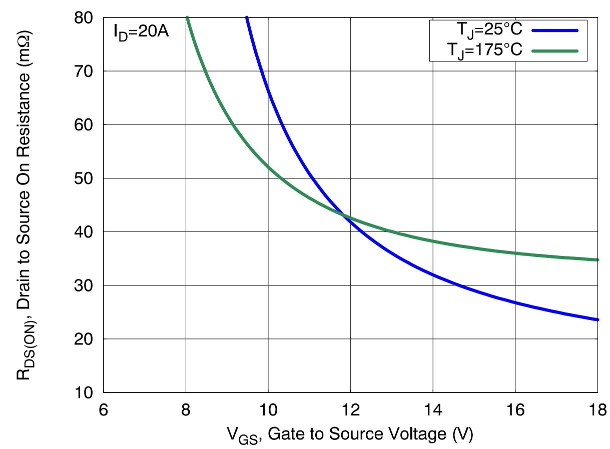


Figure 4. On−Resistance vs Gate Voltage

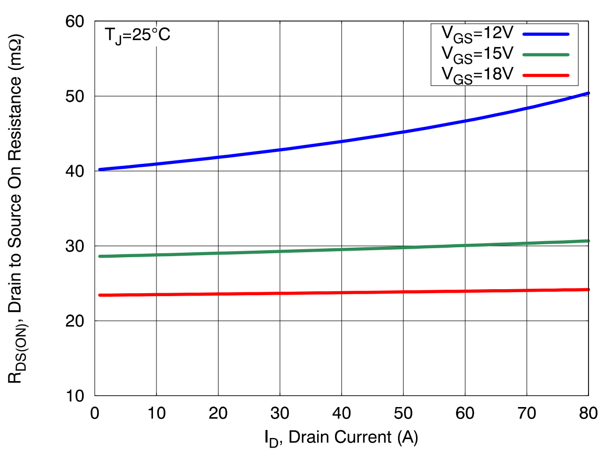


Figure 5. On−Resistance vs Drain Current

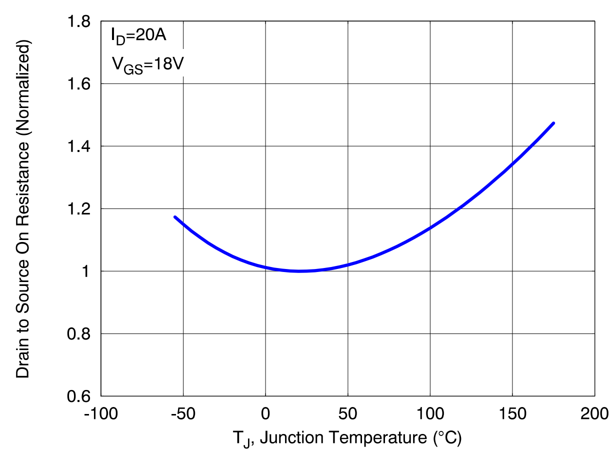


Figure 6. On−Resistance vs Junction Temperature

TYPICAL CHARACTERISTICS

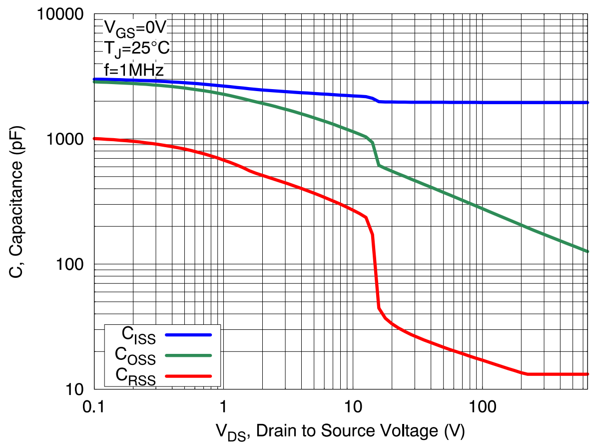


Figure 7. Capacitance Characteristics

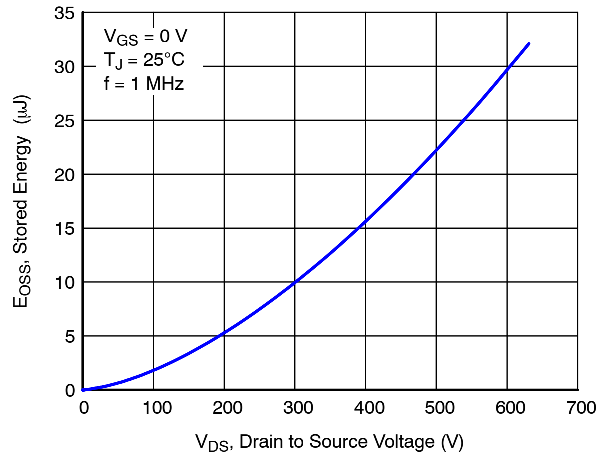


Figure 8. Stored Energy vs Drain to Source Voltage

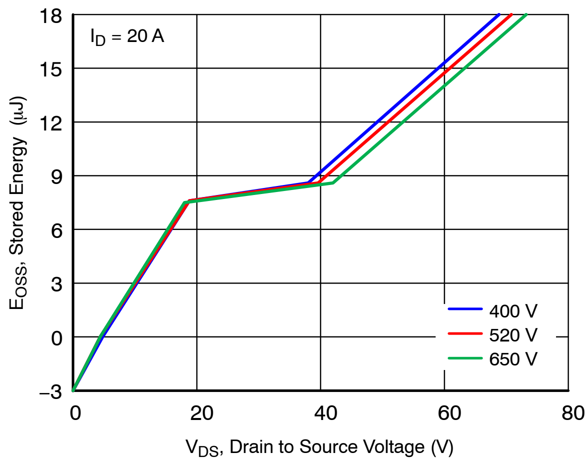


Figure 9. Gate Charge Characteristics

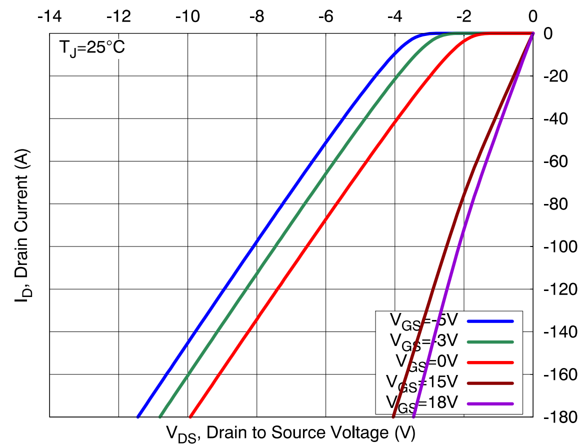


Figure 10. Reverse Conduction Characteristics

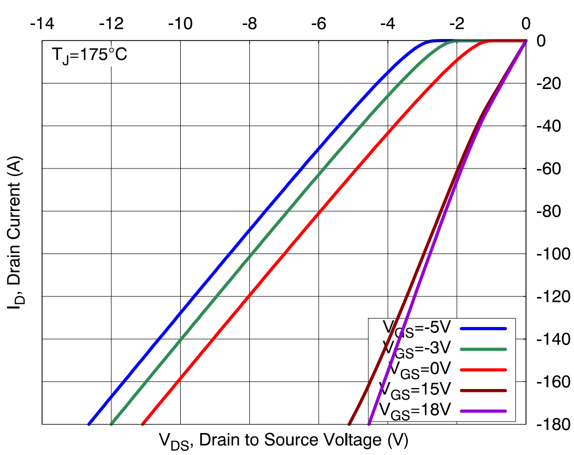


Figure 11. Reverse Conduction Characteristics

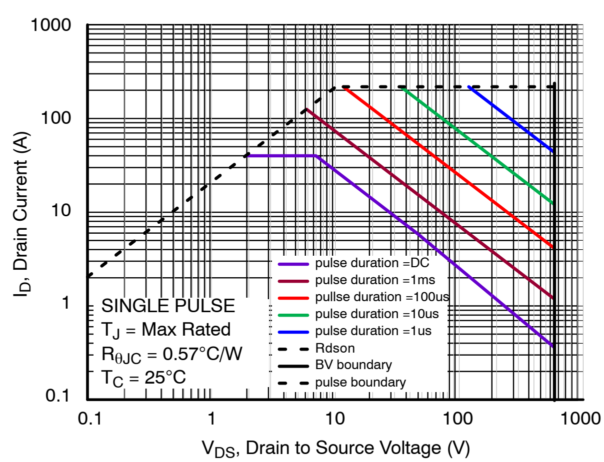


Figure 12. Safe Operating Area

TYPICAL CHARACTERISTICS

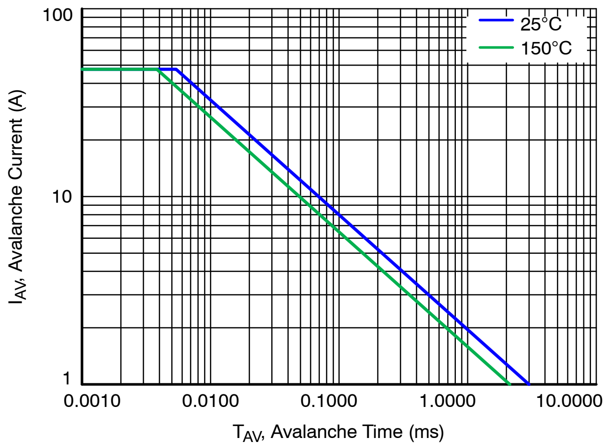


Figure 13. Avalanche Current vs Pulse Time (UIS)

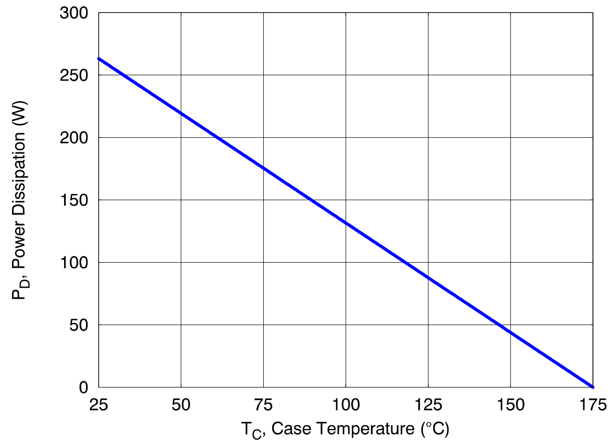


Figure 14. Maximum Power Dissipation vs Case Temperature

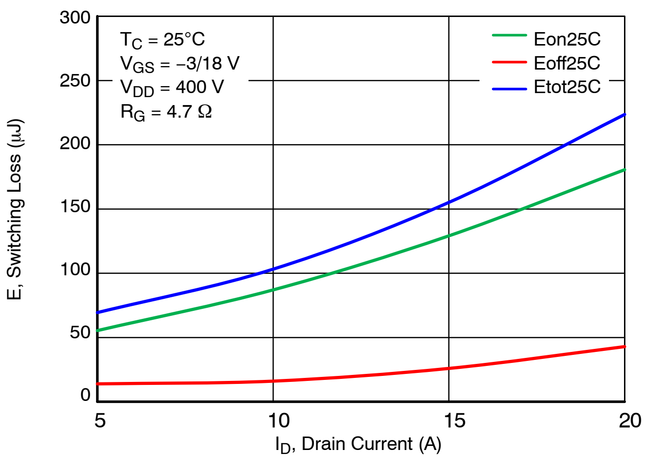


Figure 15. Inductive Switching Loss vs Drain Current

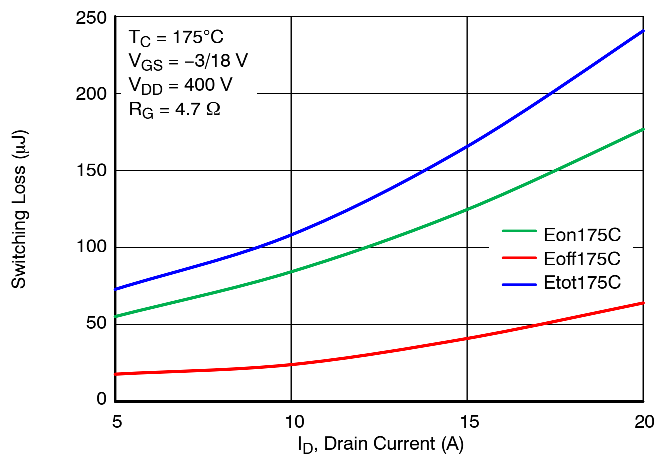


Figure 16. Inductive Switching Loss vs Drain Current

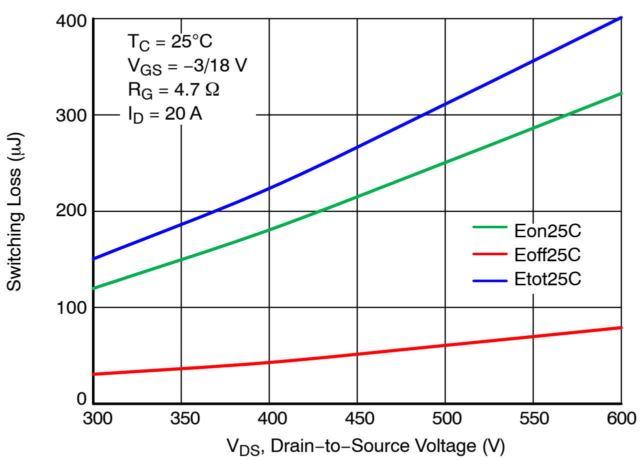


Figure 17. Inductive Switching Loss vs Drain Voltage

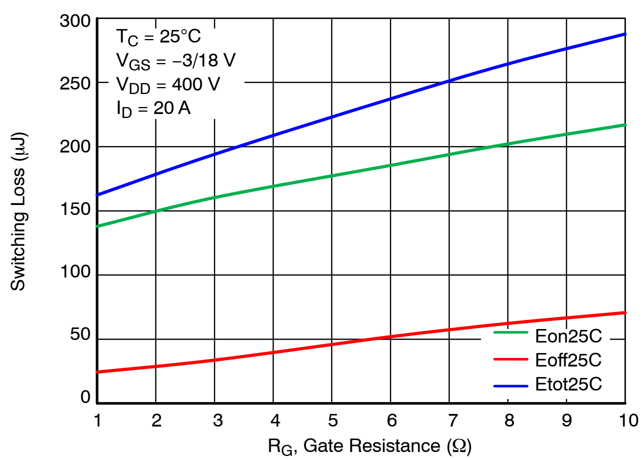


Figure 18. Inductive Switching Loss vs Gate Resistance

TYPICAL CHARACTERISTICS

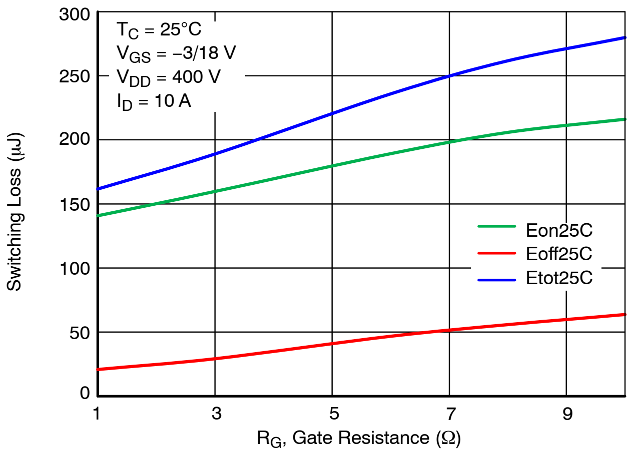


Figure 19. Inductive Switching Loss vs Gate Resistance

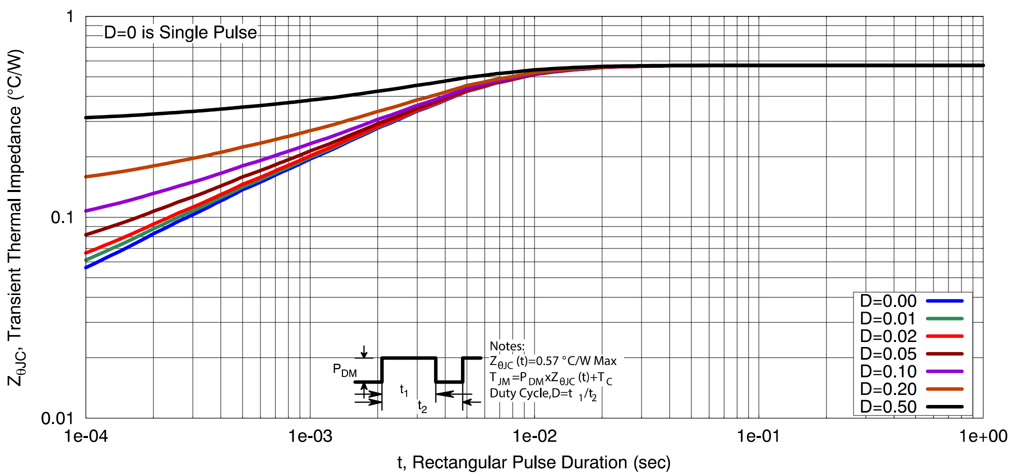
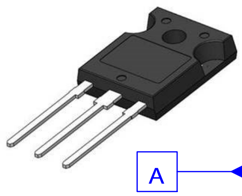
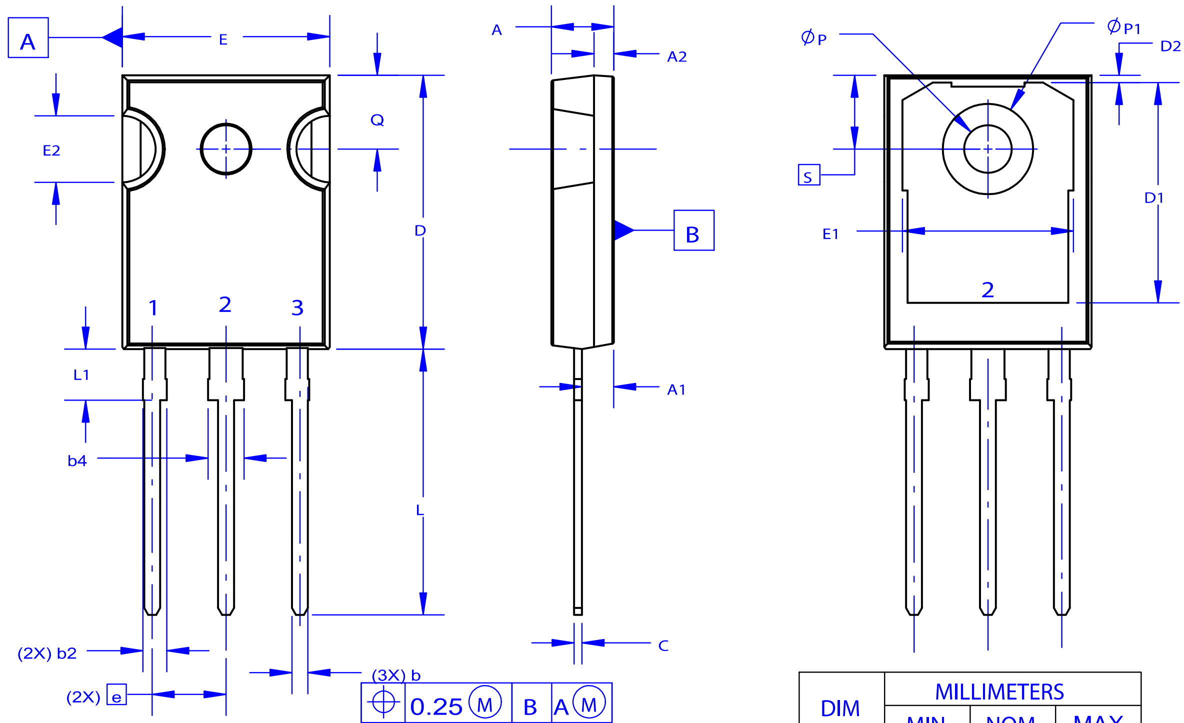


Figure 20. Thermal Response Characteristics



TO−247−3LD
CASE 340CX
ISSUE A

DATE 06 JUL 2020

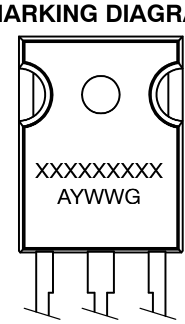


NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
ØP1	6.60	6.80	7.00

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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