

# MOSFET – Power, N-Channel, Logic Level 100 V, 23 A, 56 mΩ

## NTD6415ANL, NVD6415ANL

### Features

- Low  $R_{DS(on)}$
- 100% Avalanche Tested
- NVD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V <sub>DSS</sub>	100	V
Gate-to-Source Voltage – Continuous			V <sub>GS</sub>	± 20	V
Continuous Drain Current	Steady State	T <sub>C</sub> = 25°C	I <sub>D</sub>	23	A
		T <sub>C</sub> = 100°C		16	
Power Dissipation	Steady State	T <sub>C</sub> = 25°C	P <sub>D</sub>	83	W
Pulsed Drain Current	t <sub>p</sub> = 10 μs		I <sub>DM</sub>	80	A
Operating and Storage Temperature Range			T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Source Current (Body Diode)			I <sub>S</sub>	23	A
Single Pulse Drain-to-Source Avalanche Energy (V <sub>DD</sub> = 50 Vdc, V <sub>GS</sub> = 10 Vdc, I <sub>L(pk)</sub> = 23 A, L = 0.3 mH, R <sub>G</sub> = 25 Ω)			E <sub>AS</sub>	79	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds			T <sub>L</sub>	260	°C

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) – Steady State	$R_{\theta JC}$	1.8	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	49	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

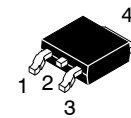
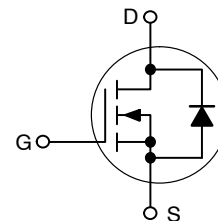
1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).



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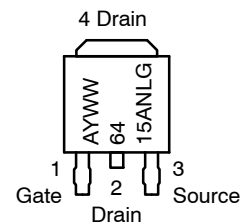
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	56 mΩ @ 4.5 V	23 A
	52 mΩ @ 10 V	



**DPAK**  
**CASE 369AA**  
**STYLE 2**

### MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location\*  
6415ANL = Device Code  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

# NTD6415ANL, NVD6415ANL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA, T <sub>J</sub> = -40°C	100 92			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /T <sub>J</sub>			115		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 100 V	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C		1.0 100	μA
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	1.0		2.0	V
Negative Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>			4.8		mV/°C
Drain-to-Source On-Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 10 A		44	56	mΩ
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 10 A		43	52	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 10 A		24		S

### CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, f = 1.0 MHz, V <sub>DS</sub> = 25 V		1024		pF
Output Capacitance	C <sub>OSS</sub>			156		
Reverse Transfer Capacitance	C <sub>RSS</sub>			70		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 80 V, I <sub>D</sub> = 23 A		20		nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			1.1		
Gate-to-Source Charge	Q <sub>GS</sub>			3.1		
Gate-to-Drain Charge	Q <sub>GD</sub>			14		
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 80 V, I <sub>D</sub> = 23 A		35		nC

### SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>GS</sub> = 4.5 V, V <sub>DD</sub> = 80 V, I <sub>D</sub> = 23 A, R <sub>G</sub> = 6.1 Ω		11		ns
Rise Time	t <sub>r</sub>			91		
Turn-Off Delay Time	t <sub>d(off)</sub>			40		
Fall Time	t <sub>f</sub>			71		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 23 A	T <sub>J</sub> = 25°C T <sub>J</sub> = 125°C	0.87 0.74	1.2	V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 23 A		64		ns
Charge Time	T <sub>a</sub>			40		
Discharge Time	T <sub>b</sub>			24		
Reverse Recovery Charge	Q <sub>RR</sub>			152		nC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

3. Switching characteristics are independent of operating junction temperatures.

## ORDERING INFORMATION

Device	Package	Shipping†
NTD6415ANLT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD6415ANLT4G		
NVD6415ANLT4G-VF01		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

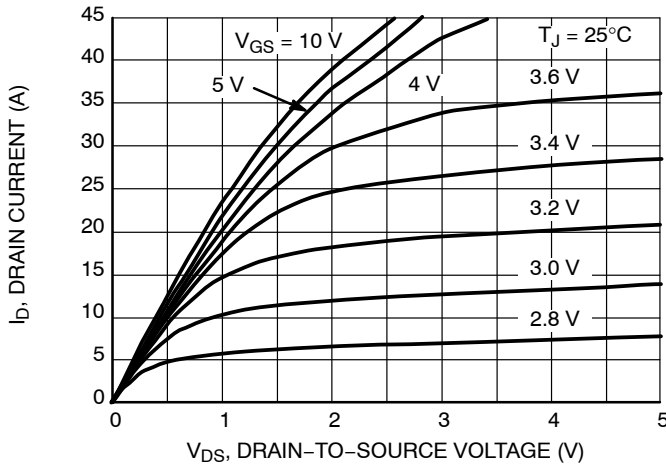


Figure 1. On-Region Characteristics

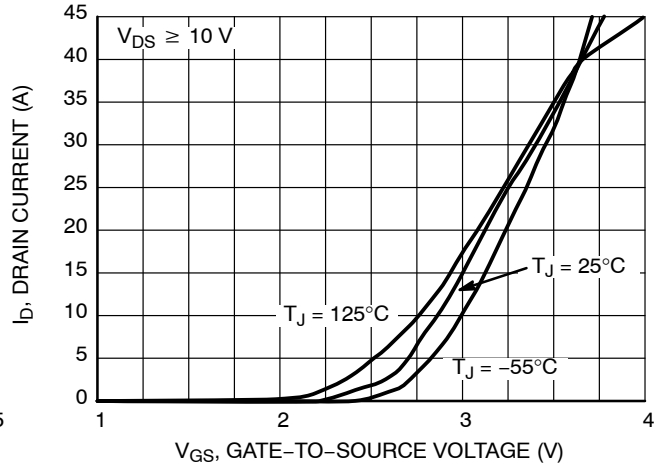


Figure 2. Transfer Characteristics

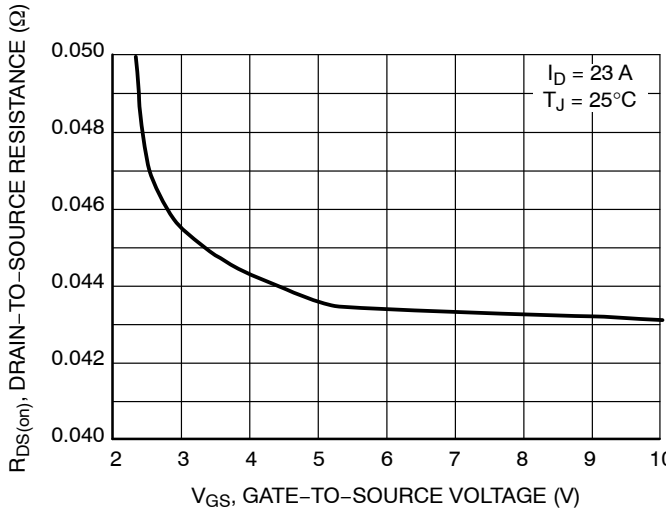


Figure 3. On-Region versus Gate Voltage

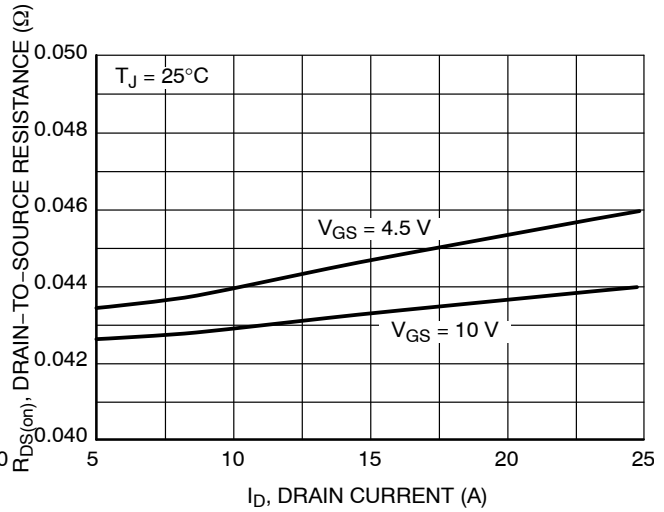


Figure 4. On-Resistance versus Drain Current and Gate Voltage

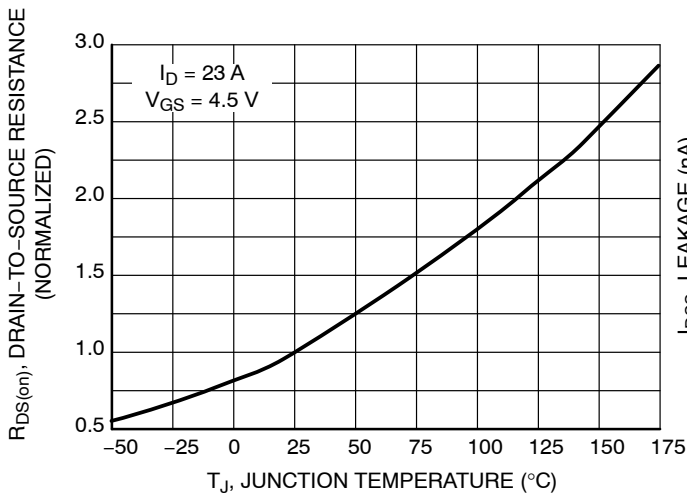


Figure 5. On-Resistance Variation with Temperature

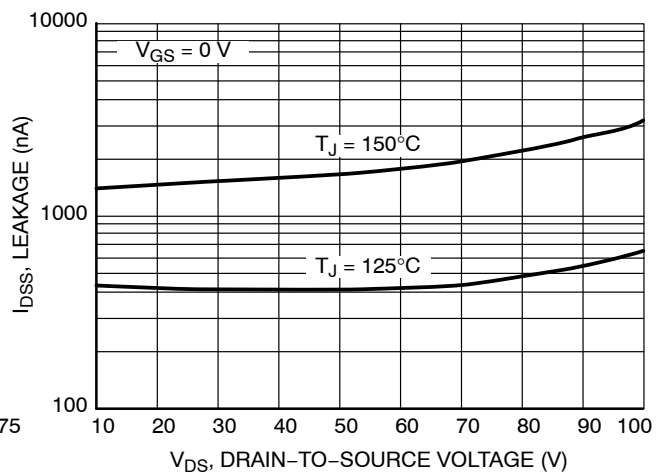


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL CHARACTERISTICS

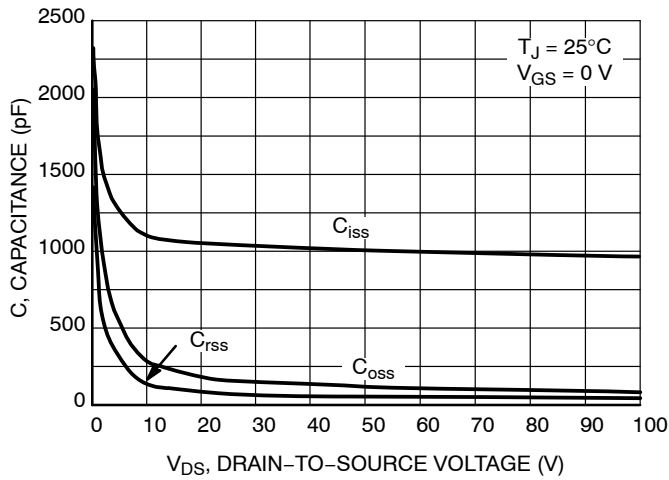


Figure 7. Capacitance Variation

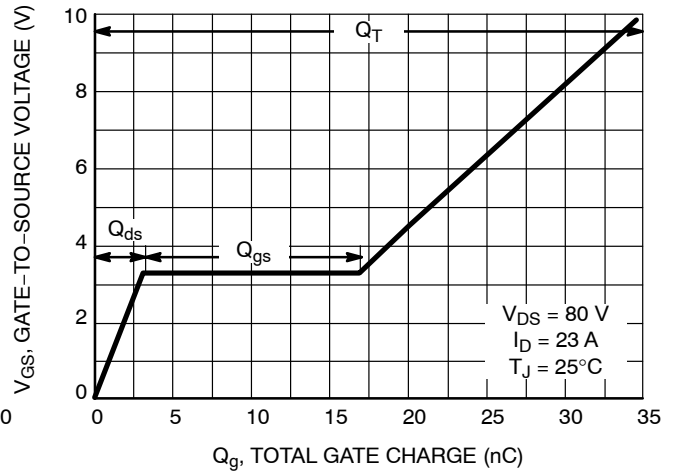


Figure 8. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

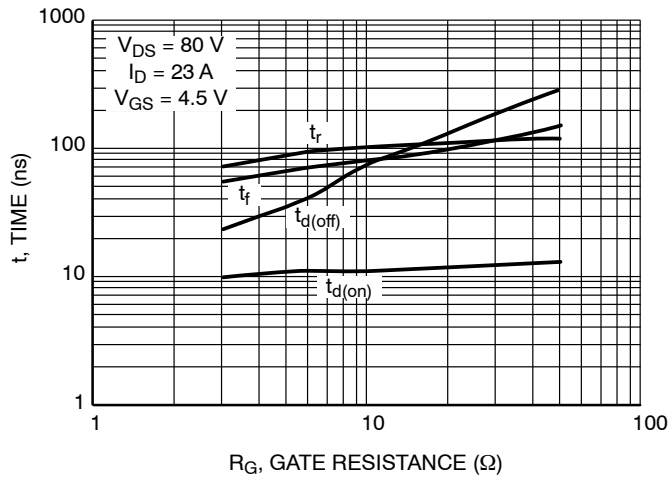


Figure 9. Resistive Switching Time Variation versus Gate Resistance

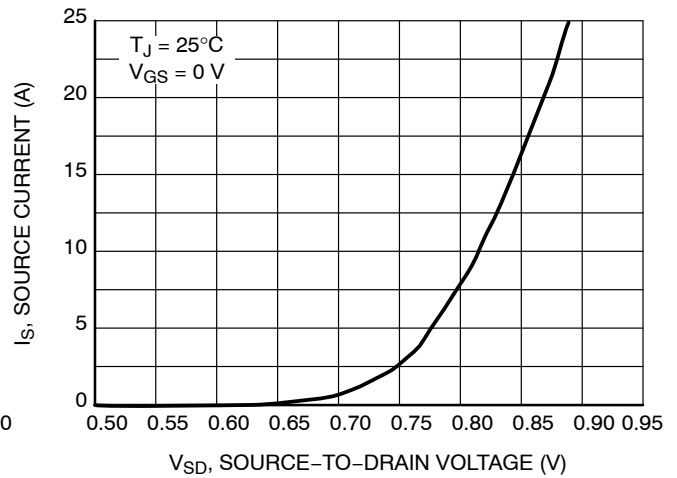


Figure 10. Diode Forward Voltage versus Current

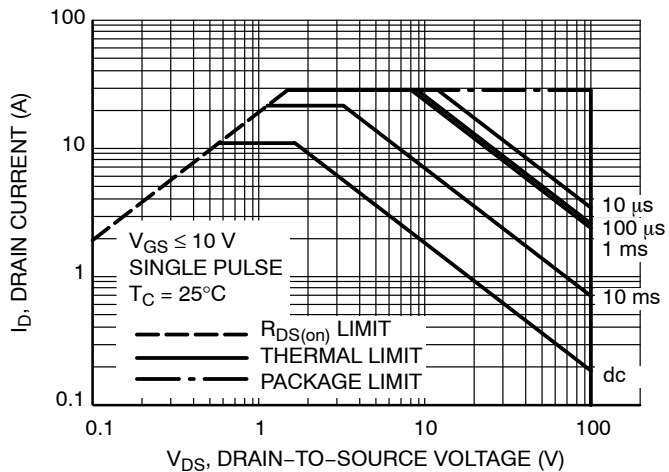


Figure 11. Maximum Rated Forward Biased Safe Operating Area

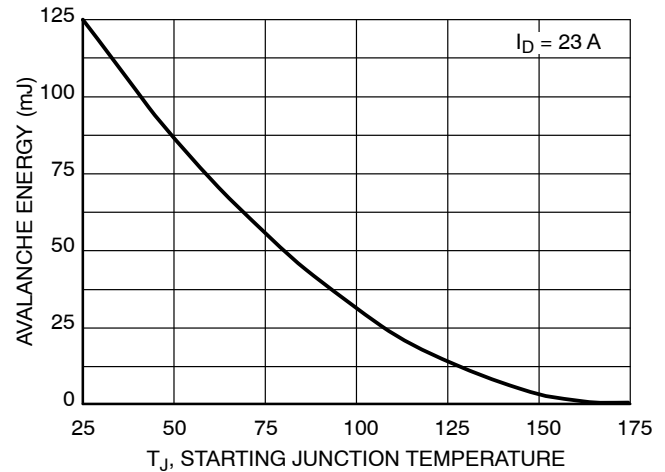


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

# NTD6415ANL, NVD6415ANL

## TYPICAL CHARACTERISTICS

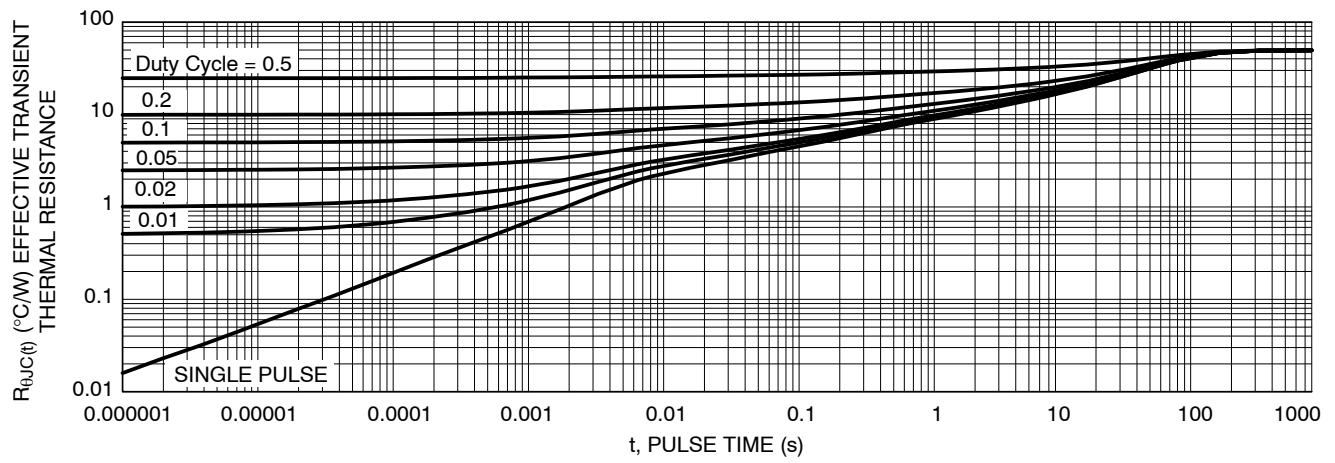


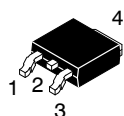
Figure 13. Thermal Response

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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ON



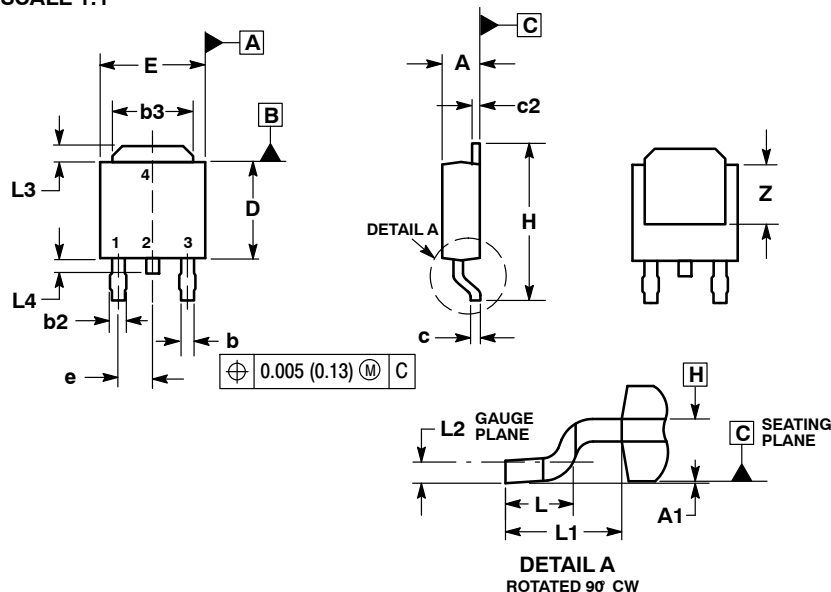
SCALE 1:1

### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010



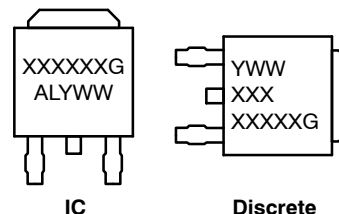
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

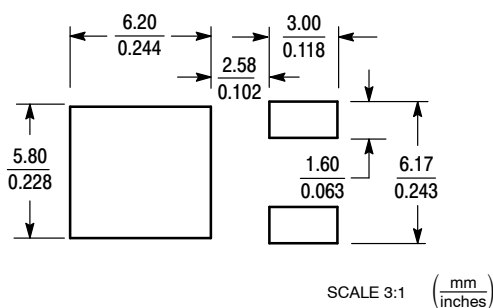
### GENERIC MARKING DIAGRAM\*



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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