NTD5407N, STD5407N, NVD5407N

MOSFET – Power, Single, N-Channel, DPAK
40 V, 38 A

ON Semiconductor®

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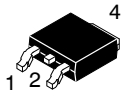
Features
- Low $R_{DS(on)}$
- High Current Capability
- Low Gate Charge
- STD Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable*
- These Devices are Pb−Free and are RoHS Compliant

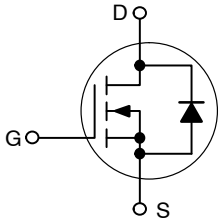
Applications
- Electronic Brake Systems
- Electronic Power Steering
- Bridge Circuits

$V_{(BR)DSS}$	$R_{DS(ON)}$ TYP	I_D MAX (Note 1)
40 V	21 mΩ @ 10 V	38 A



DPAK
CASE 369C
STYLE 2

N−Channel

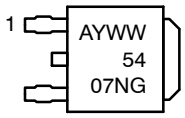


MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current − $R_{\theta JC}$	Steady State	T_C = 25°C	I_D	38	A
		T_C = 100°C		27	
Power Dissipation − $R_{\theta JC}$	Steady State	T_C = 25°C	P_D	75	W
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	7.6	A
		T_A = 100°C		5.3	
Power Dissipation − $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	P_D	2.9	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	75	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 175	°C
Source Current (Body Diode)			I_S	36	A
Single Pulse Drain−to Source Avalanche Energy − (V_{DD} = 50 V, V_{GS} = 10 V, I_{PK} = 17 A, L = 1 mH, R_G = 25 Ω)			EAS	150	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

MARKING DIAGRAM



A = Assembly Location*
Y = Year
WW = Work Week
5407N = Specific Device Code
G = Pb−Free Device

* The Assembly Location code (A) is front side optional. In cases where the Assembly Location is stamped in the package, the front side assembly code may be blank.

ORDERING INFORMATION

Device	Package	Shipping†
NTD5407NT4G	DPAK (Pb−Free)	2500 / Tape & Reel
STD5407NT4G*	DPAK (Pb−Free)	2500 / Tape & Reel
NVD5407NT4G*	DPAK (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS (Note 1)

Parameter	Symbol	Max	Unit
Junction−to−Case (Drain)	$R_{\theta JC}$	2.0	°C/W
Junction−to−Ambient (Note 1)	$R_{\theta JA}$	52	°C/W

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [2 oz] including traces).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				39		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1.0	μA
			T_J = 100°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V				±100	nA
ON CHARACTERISTICS (Note 2)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.5		3.5	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				−6.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 20 A			21	26	mΩ
		V_{GS} = 5.0 V, I_D = 10 A			32	40	
Forward Transconductance	g_{FS}	V_{GS} = 10 V, I_D = 18 A			15		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 32 V			615	1000	pF
Output Capacitance	C_{OSS}				173		
Reverse Transfer Capacitance	C_{RSS}				80		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 38 A			20		nC
Gate−to−Source Charge	Q_{GS}				2.25		
Gate−to−Drain Charge	Q_{GD}				10.5		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 32 V, I_D = 38 A, R_G = 2.5 Ω			6.8		ns
Rise Time	t_r				17		
Turn−Off Delay Time	$t_{d(OFF)}$				66		
Fall Time	t_f				51		
SWITCHING CHARACTERISTICS, V_{GS} = 5 V (Note 3)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 5 V, V_{DD} = 20 V, I_D = 20 A, R_G = 2.5 Ω			10		ns
Rise Time	t_r				175		
Turn−Off Delay Time	$t_{d(OFF)}$				13		
Fall Time	t_f				23		
DRAIN−SOURCE DIODE CHARACTERISTICS (Note 2)							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5.0 A	T_J = 25°C		0.9	1.1	V
			T_J = 125°C		0.75		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 15 A			38		ns
Charge Time	t_a				20.5		
Discharge Time	t_b				17		
Reverse Recovery Charge	Q_{RR}				40		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

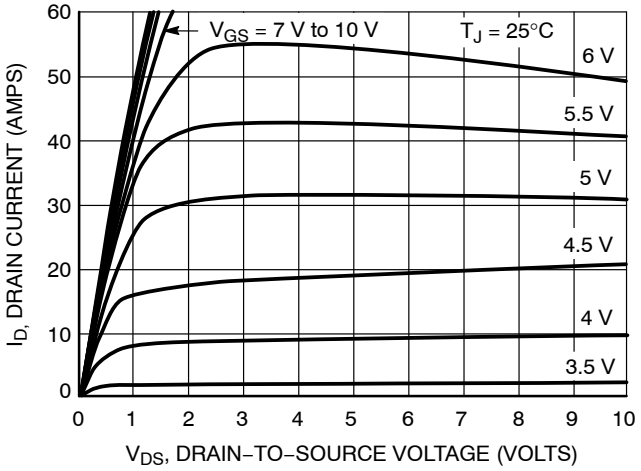


Figure 1. On−Region Characteristics

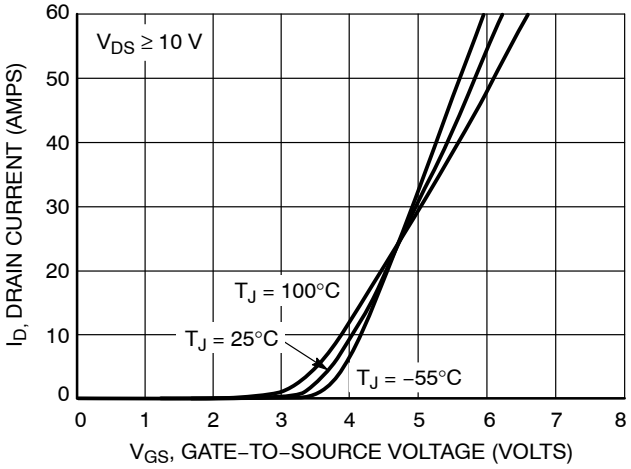


Figure 2. Transfer Characteristics

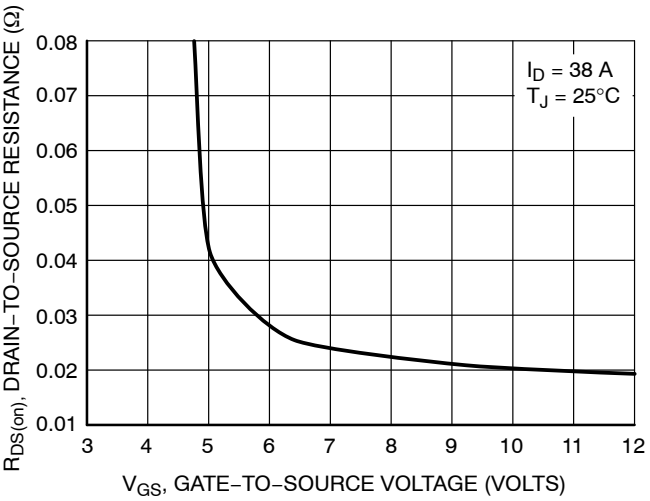


Figure 3. On−Resistance vs. Gate−to−Source Voltage

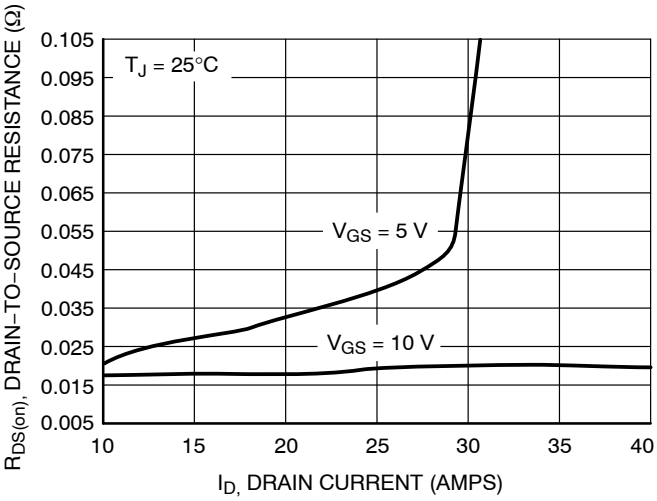


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

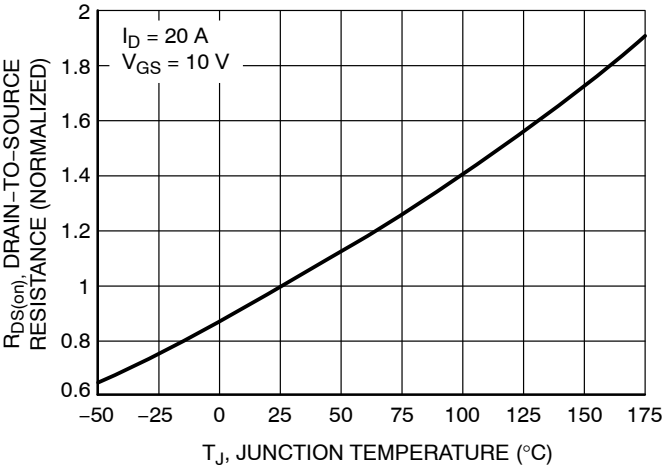


Figure 5. On−Resistance Variation with Temperature

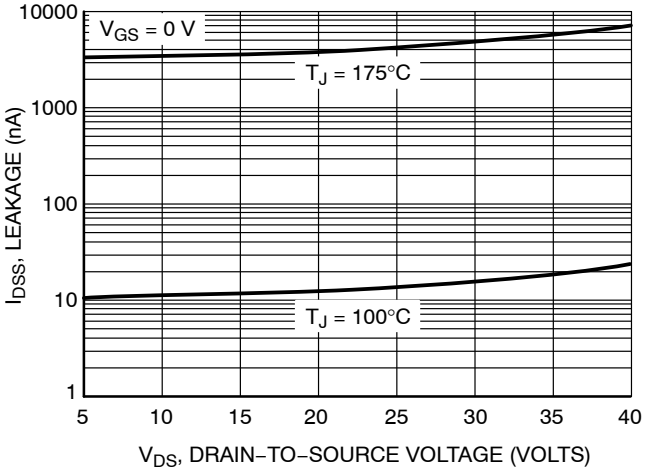


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

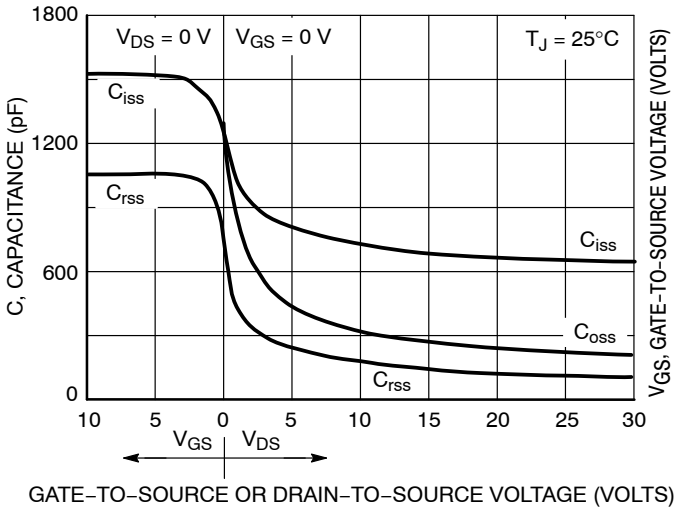


Figure 7. Capacitance Variation

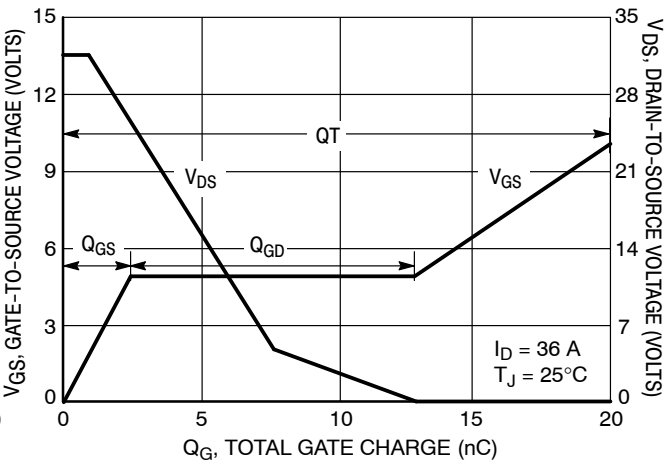


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

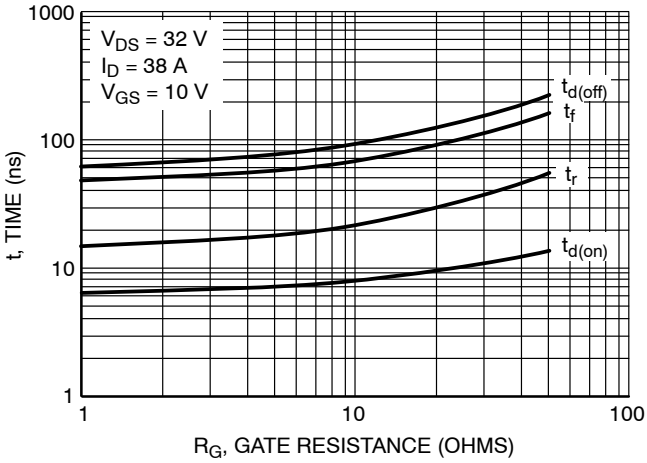


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

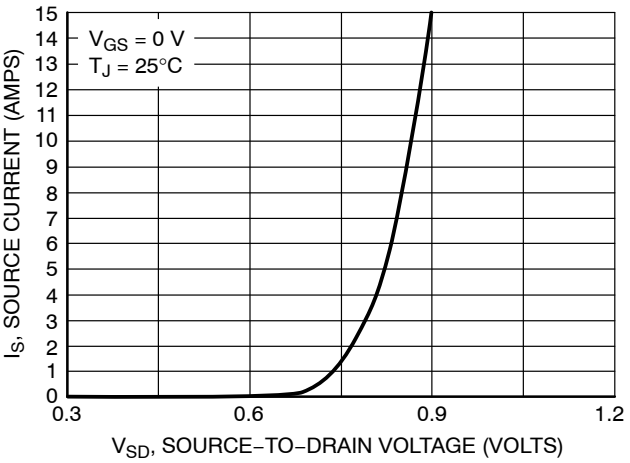


Figure 10. Diode Forward Voltage vs. Current

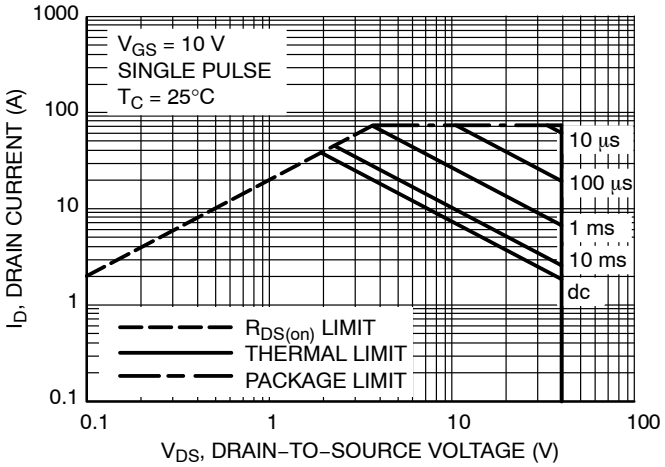


Figure 11. Maximum Rated Forward Biased Safe Operating Area

TYPICAL PERFORMANCE CURVES

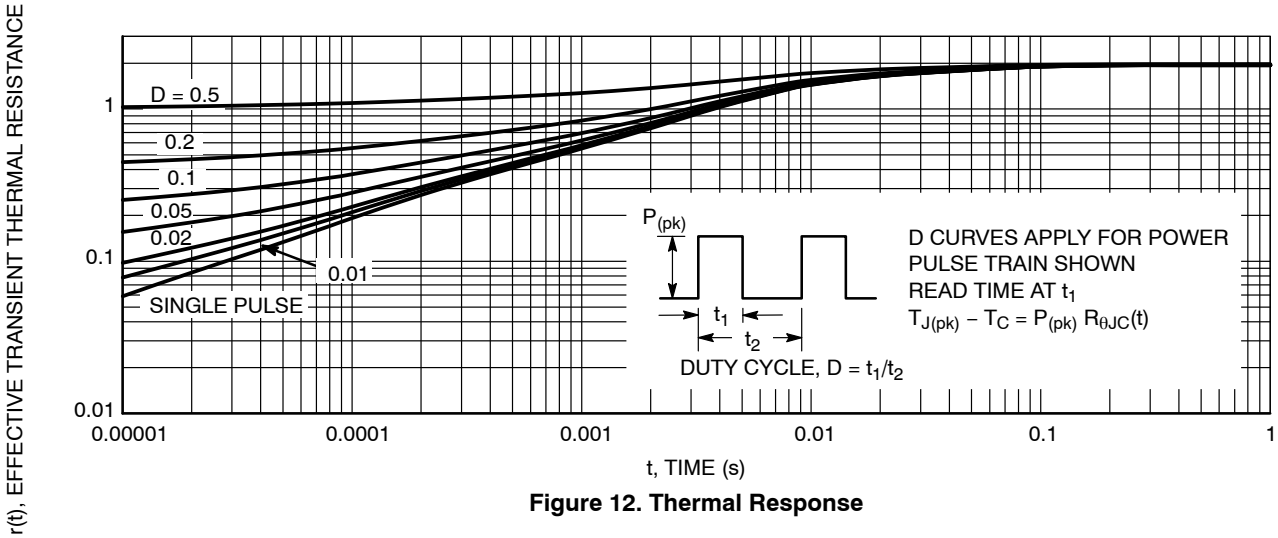


Figure 12. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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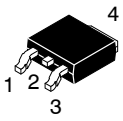
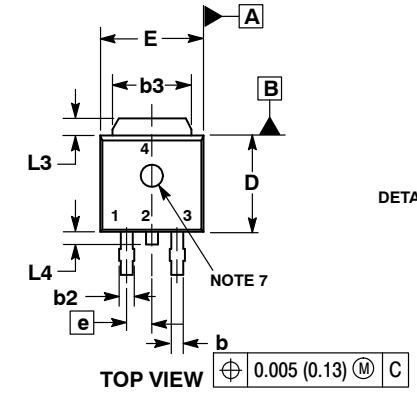
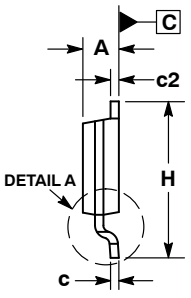


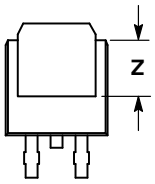
SCALE 1:1

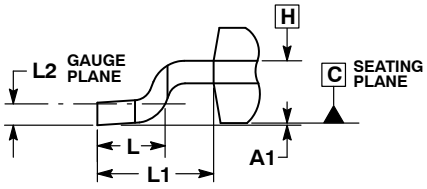
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE F

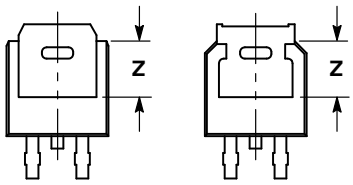
DATE 21 JUL 2015











NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF		2.90 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

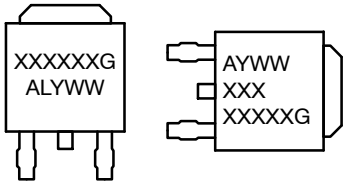
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

GENERIC MARKING DIAGRAM*

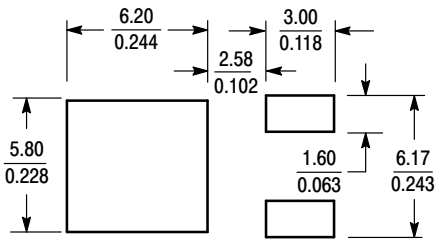


IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.

SOLDERING FOOTPRINT*



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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