NSS60601MZ4

Low $V_{CE(sat)}$ Transistor, NPN, 60 V, 6.0 A

ON Semiconductor's e^2PowerEdge family of low $V_{CE(sat)}$ transistors are surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical applications are DC−DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e^2PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

Features

- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant*
- Complementary to NSS60600MZ4

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	60	Vdc
Collector-Base Voltage	V_{CBO}	100	Vdc
Emitter-Base Voltage	V_{EBO}	6.0	Vdc
Collector Current − Continuous	I_C	6.0	A
Collector Current − Peak	I_{CM}	12.0	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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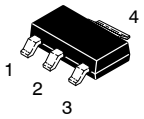
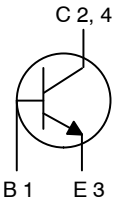
60 VOLTS, 6.0 AMPS
2.0 WATTS
NPN LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 50 mΩ

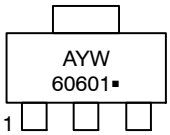


SOT−223
CASE 318E
STYLE 1



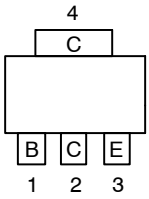
Schematic

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
60601 = Specific Device Code
▪ = Pb−Free Package

PIN ASSIGNMENT



Top View Pinout

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 1)	 800 6.5	 mW mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 1)	155	°C/W
Total Device Dissipation T_A = 25°C Derate above 25°C	P_D (Note 2)	 2 15.6	 W mW/°C
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$ (Note 2)	 64	°C/W
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{Dsingle}$ (Note 3)	 710	mW
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

1. FR−4 @ 7.6 mm^2, 1 oz. copper traces.
2. FR−4 @ 645 mm^2, 1 oz. copper traces.
3. Thermal response.

ORDERING INFORMATION

Device	Package	Shipping†
NSS60601MZ4T1G	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NSV60601MZ4T1G*	SOT−223 (Pb−Free)	1,000 / Tape & Reel
NSS60601MZ4T3G	SOT−223 (Pb−Free)	4,000 / Tape & Reel
NSV60601MZ4T3G*	SOT−223 (Pb−Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector – Emitter Breakdown Voltage (I_C = 10 mAdc, I_B = 0)	$V_{(BR)CEO}$	60	–	–	Vdc
Collector – Base Breakdown Voltage (I_C = 0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	100	–	–	Vdc
Emitter – Base Breakdown Voltage (I_E = 0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	6.0	–	–	Vdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	–	–	0.1	μAdc
Emitter Cutoff Current (V_{EB} = 6.0 Vdc)	I_{EBO}	–	–	0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain (Note 4) (I_C = 500 mA, V_{CE} = 2.0 V) (I_C = 1.0 A, V_{CE} = 2.0 V) (I_C = 2.0 A, V_{CE} = 2.0 V) (I_C = 6.0 A, V_{CE} = 2.0 V)	h_{FE}	 150 120 100 50	 – – – –	 – 360 – –	–
Collector – Emitter Saturation Voltage (Note 4) (I_C = 0.1 A, I_B = 2.0 mA) (I_C = 1.0 A, I_B = 0.100 A) (I_C = 2.0 A, I_B = 0.200 A) (I_C = 3.0 A, I_B = 60 mA) (I_C = 6.0 A, I_B = 0.6 A)	$V_{CE(sat)}$	 – – – – –	 – 0.045 0.085 – –	 0.040 0.060 0.100 0.220 0.300	V
Base – Emitter Saturation Voltage (Note 4) (I_C = 1.0 A, I_B = 0.1 A)	$V_{BE(sat)}$	–	–	0.900	V
Base – Emitter Turn–on Voltage (Note 4) (I_C = 1.0 A, V_{CE} = 2.0 V)	$V_{BE(on)}$	–	–	0.900	V
Cutoff Frequency (I_C = 500 mA, V_{CE} = 10 V, f = 1.0 MHz)	f_T	100	–	–	MHz
Input Capacitance (V_{EB} = 5.0 V, f = 1.0 MHz)	Cibo	–	400	–	pF
Output Capacitance (V_{CB} = 10 V, f = 1.0 MHz)	Cobo	–	37	–	pF
SWITCHING CHARACTERISTICS					
Delay (V_{CC} = 30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_d	–	85	–	ns
Rise (V_{CC} = 30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_r	–	115	–	ns
Storage (V_{CC} = 30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_s	–	1350	–	ns
Fall (V_{CC} = 30 V, I_C = 750 mA, I_{B1} = 15 mA)	t_f	–	125	–	ns

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.

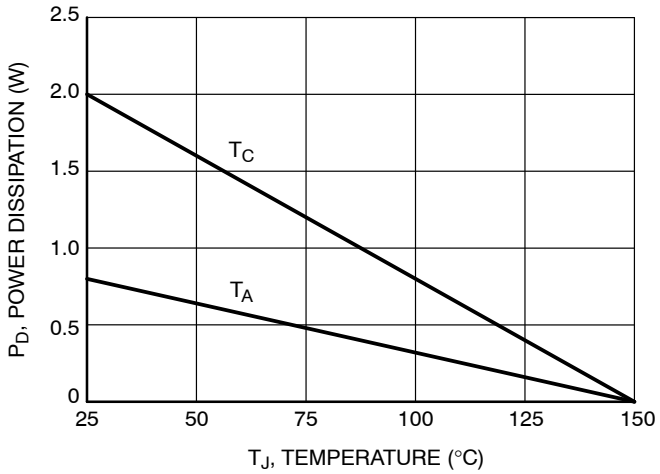


Figure 1. Power Derating

TYPICAL CHARACTERISTICS

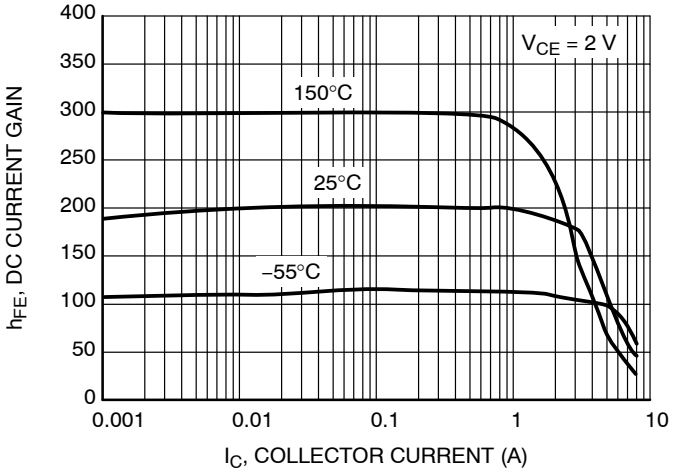


Figure 2. DC Current Gain

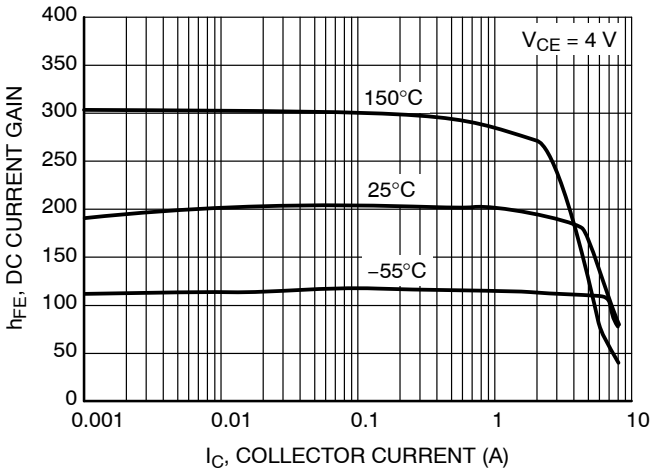


Figure 3. DC Current Gain

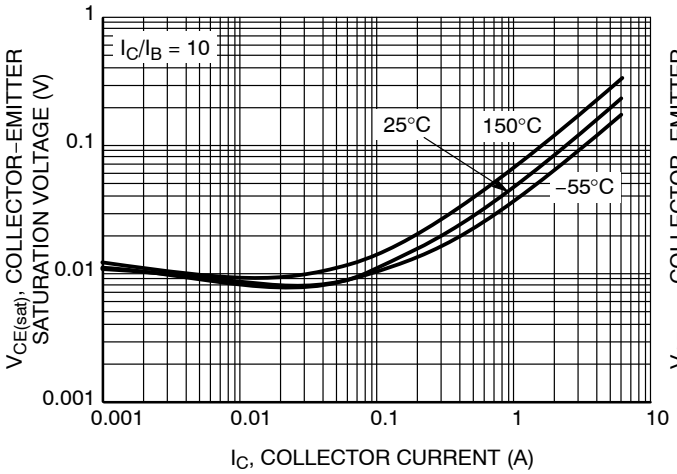


Figure 4. Collector−Emitter Saturation Voltage

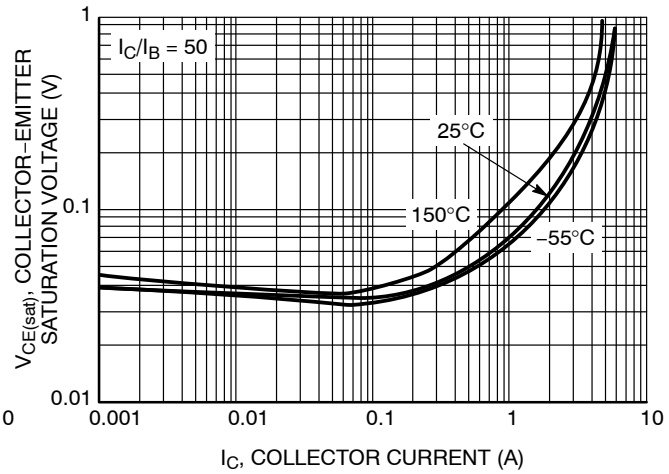


Figure 5. Collector−Emitter Saturation Voltage

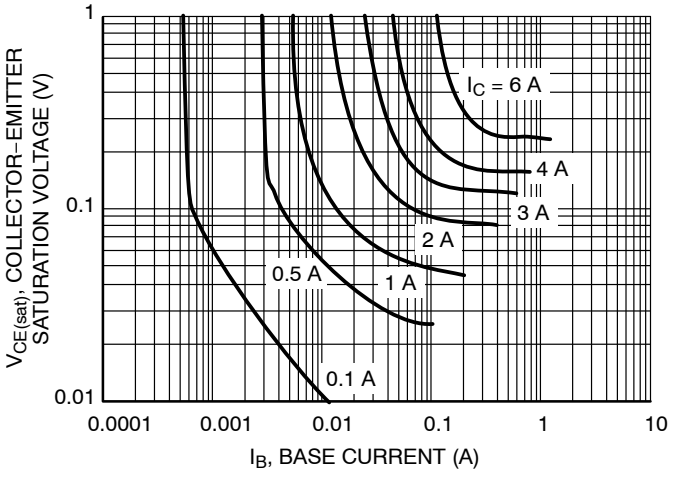


Figure 6. Collector Saturation Region

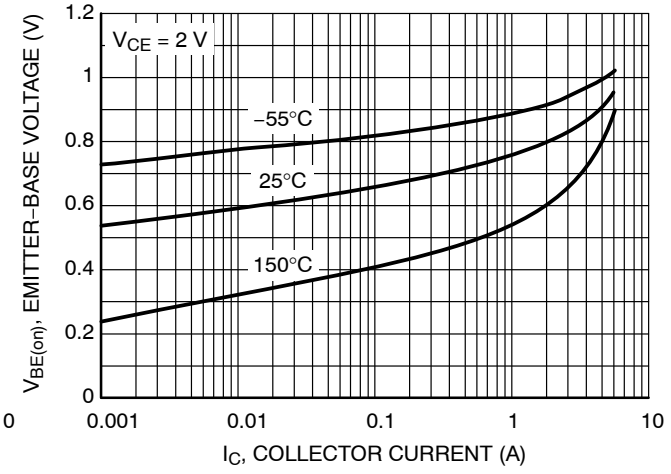


Figure 7. $V_{BE(on)}$ Voltage

TYPICAL CHARACTERISTICS

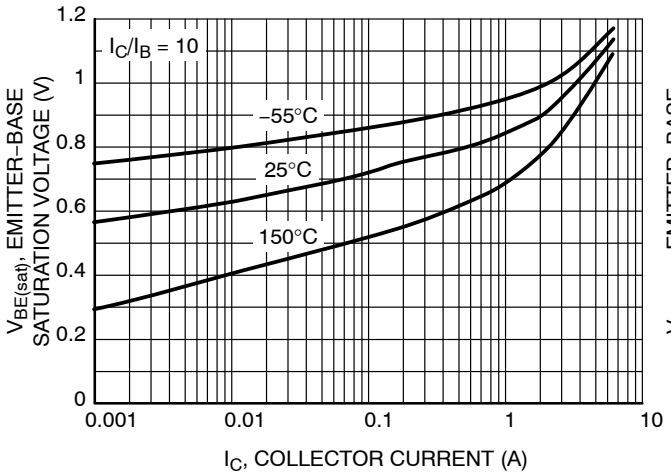


Figure 8. Base−Emitter Saturation Voltage

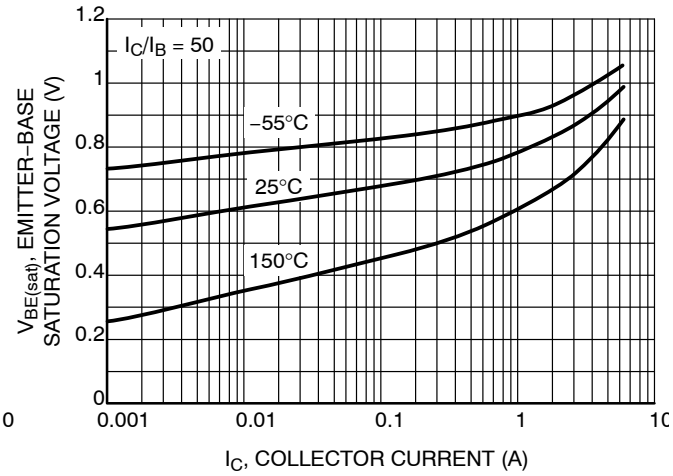


Figure 9. Base−Emitter Saturation Voltage

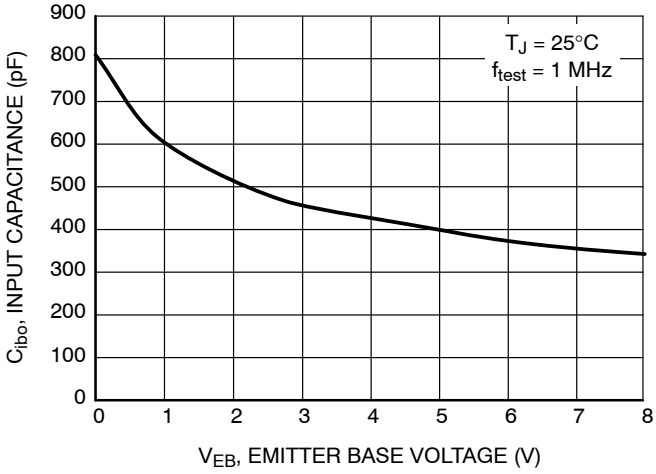


Figure 10. Input Capacitance

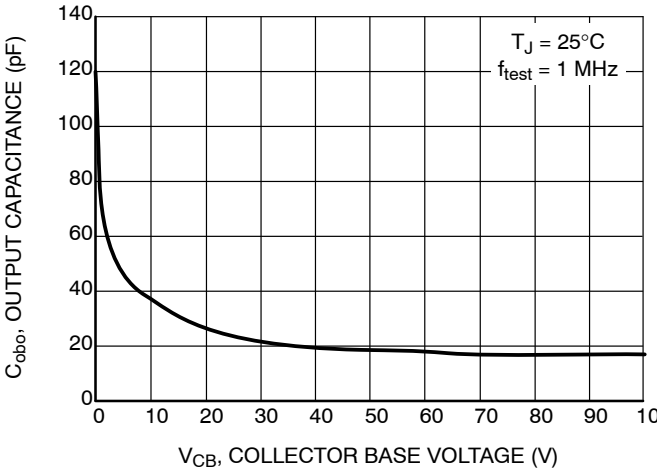


Figure 11. Output Capacitance

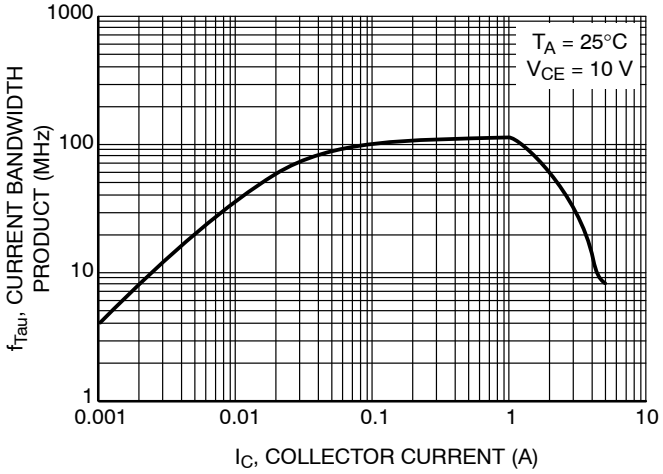


Figure 12. Current−Gain Bandwidth Product

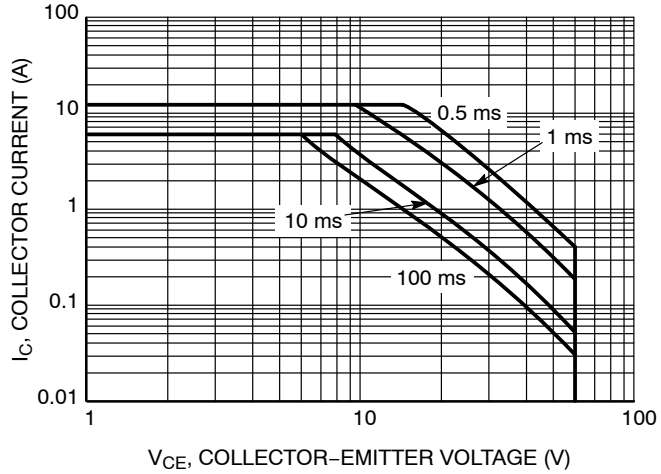
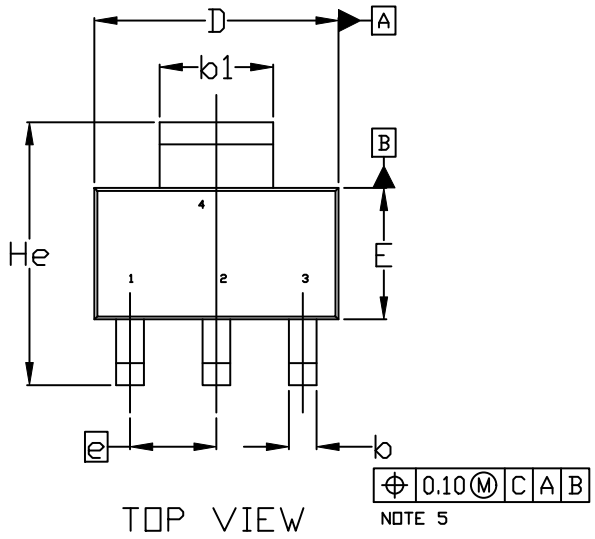


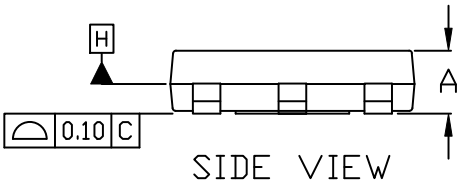
Figure 13. Safe Operating Area

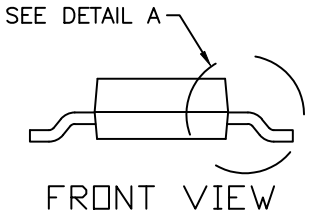
SCALE 1:1

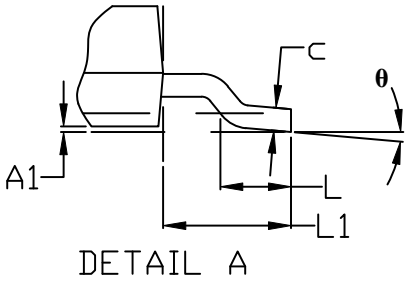
SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



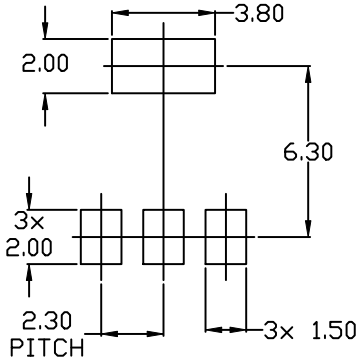






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

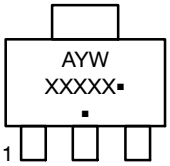
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	SOT−223 (TO−261)	PAGE 2 OF 2

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