XGS12M_LGA171_SER_FBD_HEAD

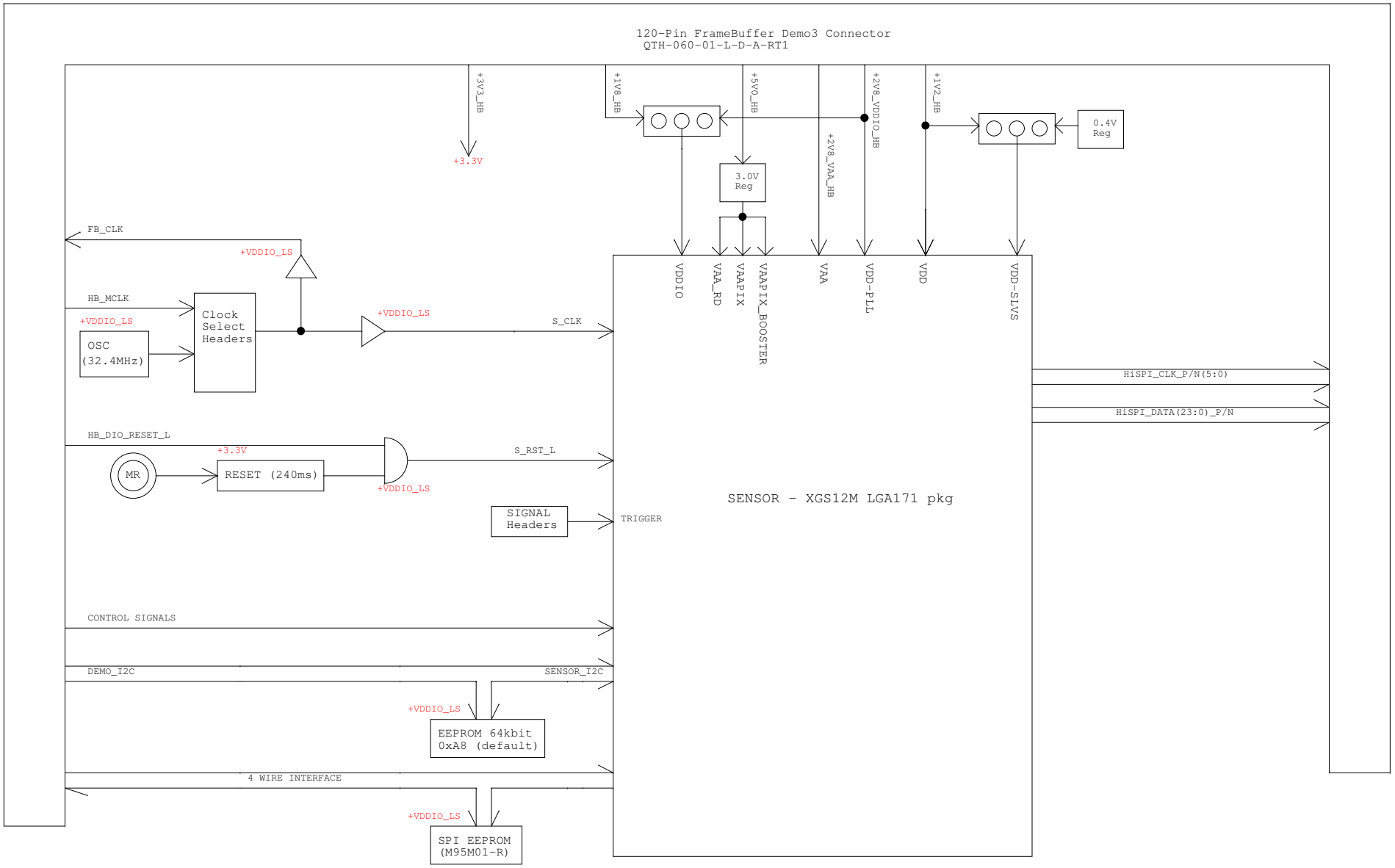
Rev	Who	Date	Description
Rev 0.0	aralex	03/10/17	Initial; Reuse of AR1810 in LGA171 package Framebuffer demo headboard design
	aralex	03/27/17	Updated the XGS12M symbol from MDB -Deleted C82 from 3.3V supply -Added jumpers P5 and P6 for power supplies -Added P7, P8, C82 and C100 to ATEST pins -Deleted C18-20; C52-54; C35 extra caps
	aralex	03/28/17	-Added header circuits for DSPARE pins and TRIGGER 1 & 2 pins -Added Test points for MONITOR pins -Added two caps each for the booster supplies
	aralex	04/04/17	-Updated text near U10 to indicate maximum current - Deleted Trigger header P2 - Added JP9 to VAA-PIX - connected MONITOR[0:2] pins to Demo connector P1 - changed P25 header text: default setting is now 4 wire I/F - Y1 supply changed to 1.8V - R70 made as DNP - changed P11 to a two pin header - updated block diagram
	aralex	04/20/17	- retained the C82 to +3.3V _Bulk cap which was deleted earlier - C139 now added to ATEST_BOT - swapped ZTP2 and ZTP3 to keep the layout same as the AR1810 Demo board - rearranged ref des of some caps connected to the booster supply pins of the sensor to maintain same layout - changed lens mount to new cmount
	aralex	04/21/17	- retained the Trigger header P2 - Deleted Test points TP3-5; Added Monitor header P27 - Added net names to Booster supply signals - mirrored P3 to ease layout
Rev 0.1	aralex	04/25/17	- Changed the 4.7uF caps to 0603 size from 0805. (C71, C75, C77, C 133, C135, C140, C142, C145)
Rev 0.2	aralex	04/28/17	- Made C133, C135 and C107 as DNP
	aralex	05/02/17	- Added net names to VREF_T and VREF_B
	aralex	08/23/17	- Changed default position of P6 to 2-3 as per Gerd's advice
	aralex	11/10/17	Changed default Jumper settings as per Raf's feedback P3: 1-2 (Default); P15: 2-3 (Default) ; No electrical change
Rev 0.3	aralex	11/16/17	Flipped the conn P3 to make it look similar to the other 3 pin headers. swapped the nets on pins 1 and 3. No electrical change
Rev 1.0	aralex	05/04/18	Modifications to the XGS12M Symbol to comply with the latest datasheet - Deleted ATEST(P7, P8, C139, C100); Vref(TP1, TP2); TEST(P3, R16); DSPARE(P12, P13, P15, R12, R14, R6) ; VPP (P11, C107); R1 connections as per new symbol following latest datasheet - S_TRIGGER0 net name changed to TRIGGER_INT - TRIGGER2 net name changed to TRIGGER_INT; TRIGGER1 net deleted - P2 connection changed; P7 and R7 added for TRIGGER_RD net
		05/09/18	Changed the 0.4V regulator to ON semiconductor part Deleted the net alias HB_MCLK from P1.111(Duplicate) C130, R37 deleted from FWSI circuit as per review feedback Removed DNP from C134; made C135 as DNP; C152 is deleted
	aralex	05/11/18	Deleted bulk caps C38, C58, C87, C88, C89, C94, C96, C101, C104, C105 as per Jeff's review. Moved C56 to VDDIO
Rev 1.1	aralex	05/18/18	Changed Ref des of R4 to R72, P7 to P28 and P3 to P27. No electrical change
	aralex	05/21/18	Changed Ref des of R6 to R63. No electrical change

ON Semiconductor

Title	Title Page	
Size C	Document Name XGS12M_LGA171_SER_FBD_HEAD	Rev 1.1
Date: Tuesday, May 22, 2018	Sheet 1 of 6	

Script executed

Block Diagram

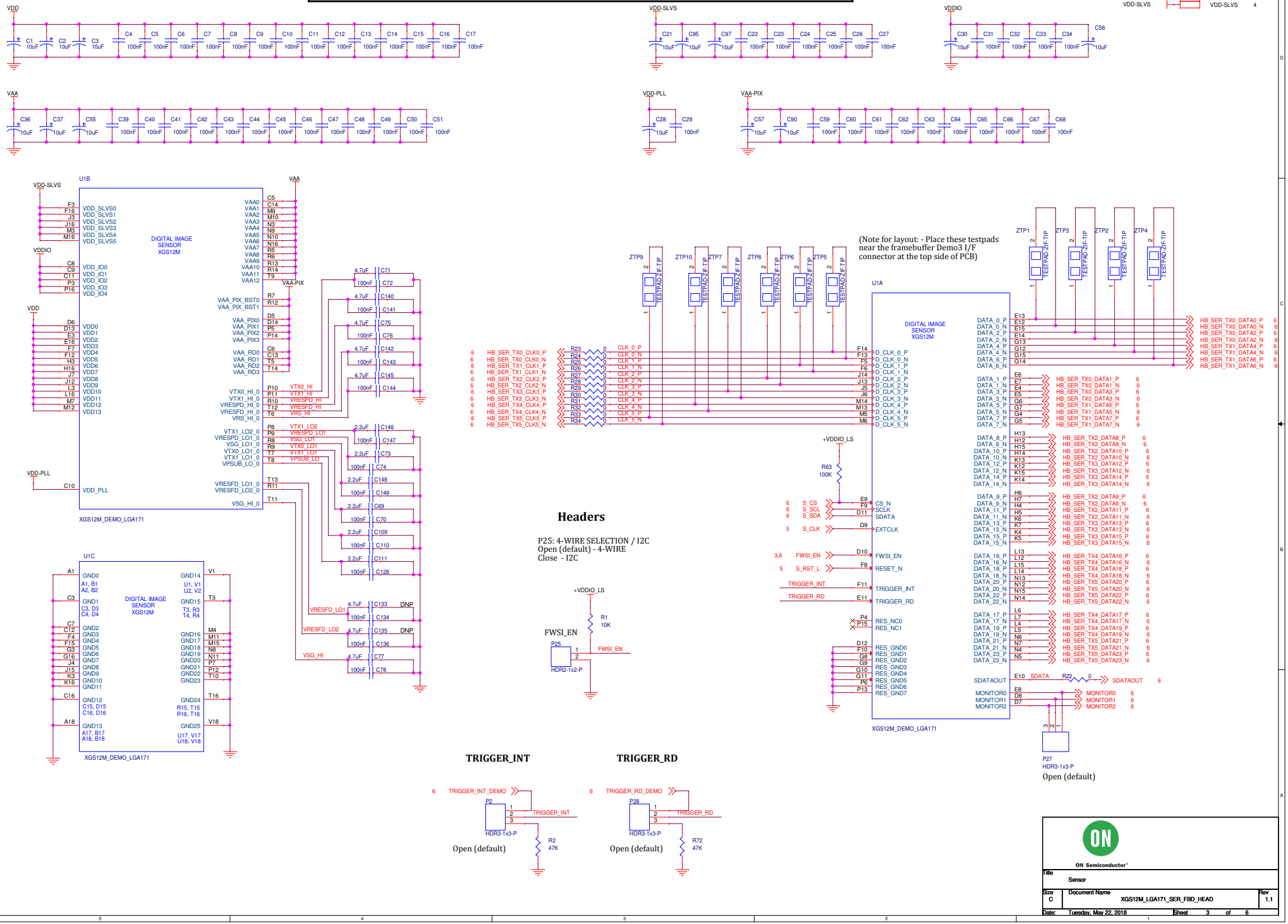


ON Semiconductor

Title: Block Diagram		
Size: C	Document Name: XGS12M_LGA171_SER_FBD_HEAD	Rev: 1.1
Date: Tuesday, May 22, 2018	Sheet 2 of 6	

Script executed

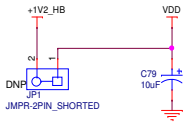
XGS12M in LGA171 pkg



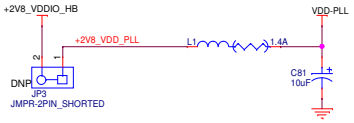
Power

Debug Headers: Cut away the shorted trace and mount header for power debugging

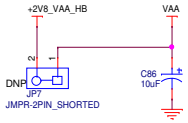
VDD 1.2V SUPPLY



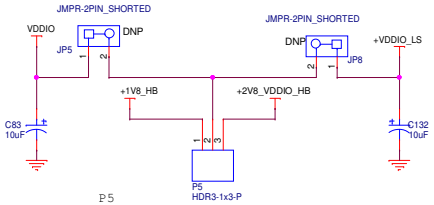
VDD-PLL 2.8V SUPPLY



VAA 2.8V SUPPLY



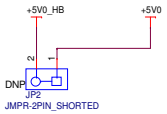
VDDIO 1.8V / 2.8V SUPPLY



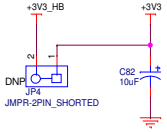
P5

2-3 (Default) --> 2.8V operation
1-2 --> 1.8V operation

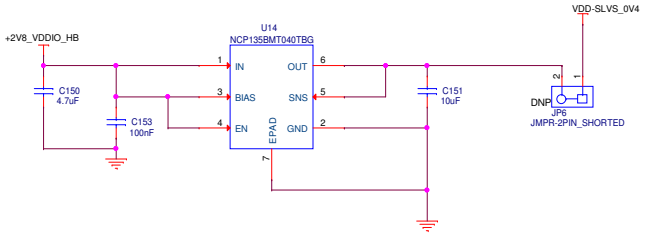
PERIPHERAL 5.0V SUPPLY



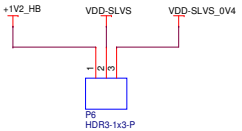
PERIPHERAL 3.3V SUPPLY



VDDSLVSPHY 0.4V SUPPLY



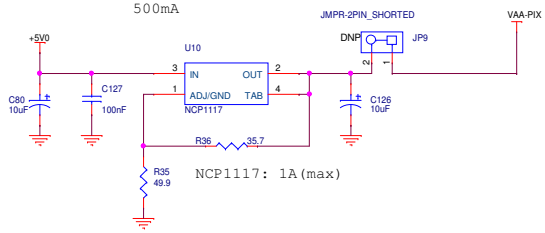
VDD-SLVS 1.2V / 0.4V SUPPLY



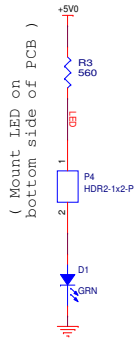
Default: Jumper 2-3

VAAPIX 3.0V SUPPLY

500mA



5V LED



+5V0_HB — +5V0_HB 6
+3V3_HB — +3V3_HB 6
+2V8_VAA_HB — +2V8_VAA_HB 6
+2V8_VDDIO_HB — +2V8_VDDIO_HB 6
+1V8_HB — +1V8_HB 5,6
+1V2_HB — +1V2_HB 6

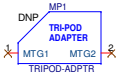
+3V3 — +3V3 5
+VDDIO_LS — +VDDIO_LS 3,5,6

VDD — VDD 3
VDD-PLL — VDD-PLL 3

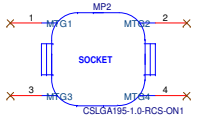
VDDIO — VDDIO 3
VAA — VAA 3
VAA-PIX — VAA-PIX 3

VDD-SLVS — VDD-SLVS 3

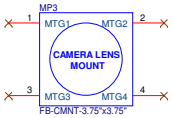
Tripod Mount

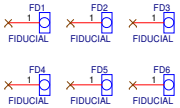


Socket

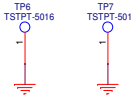


Lens Mount

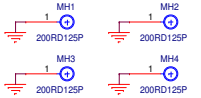




Ground Testpoints



Mounting Holes



ON Semiconductor

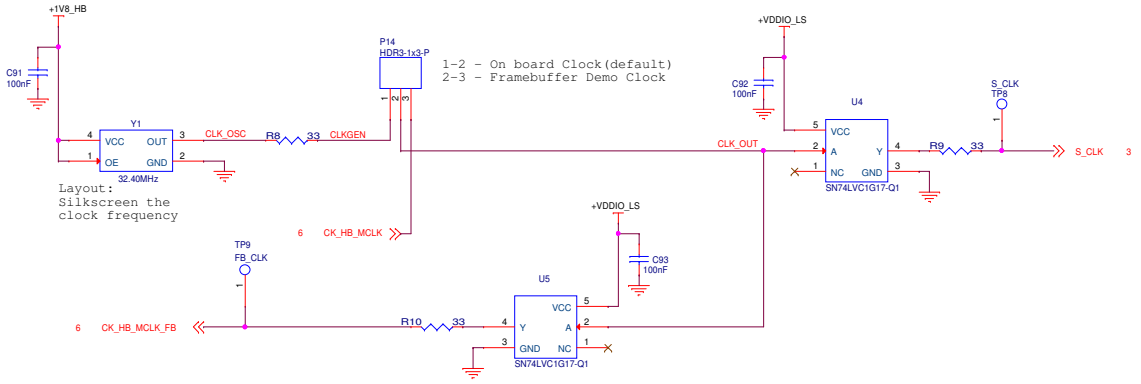
Title	Power	
Size C	Document Name XGS12M_LGA171_SER_FBD_HEAD	Rev 1.1
Date: Tuesday, May 22, 2018	Sheet 4 of 6	

Script executed

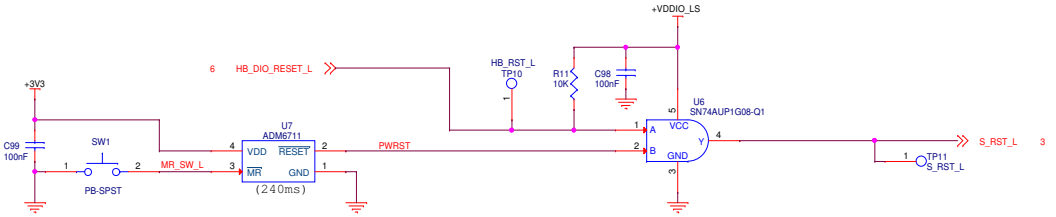
Clock and Reset

+5V0 +3V3 +VDDIO_LS — +5V0 4, +3V3 4, +VDDIO_LS 3,4,6

CLOCK CIRCUIT



RESET CIRCUIT

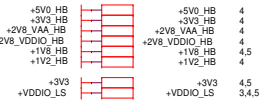


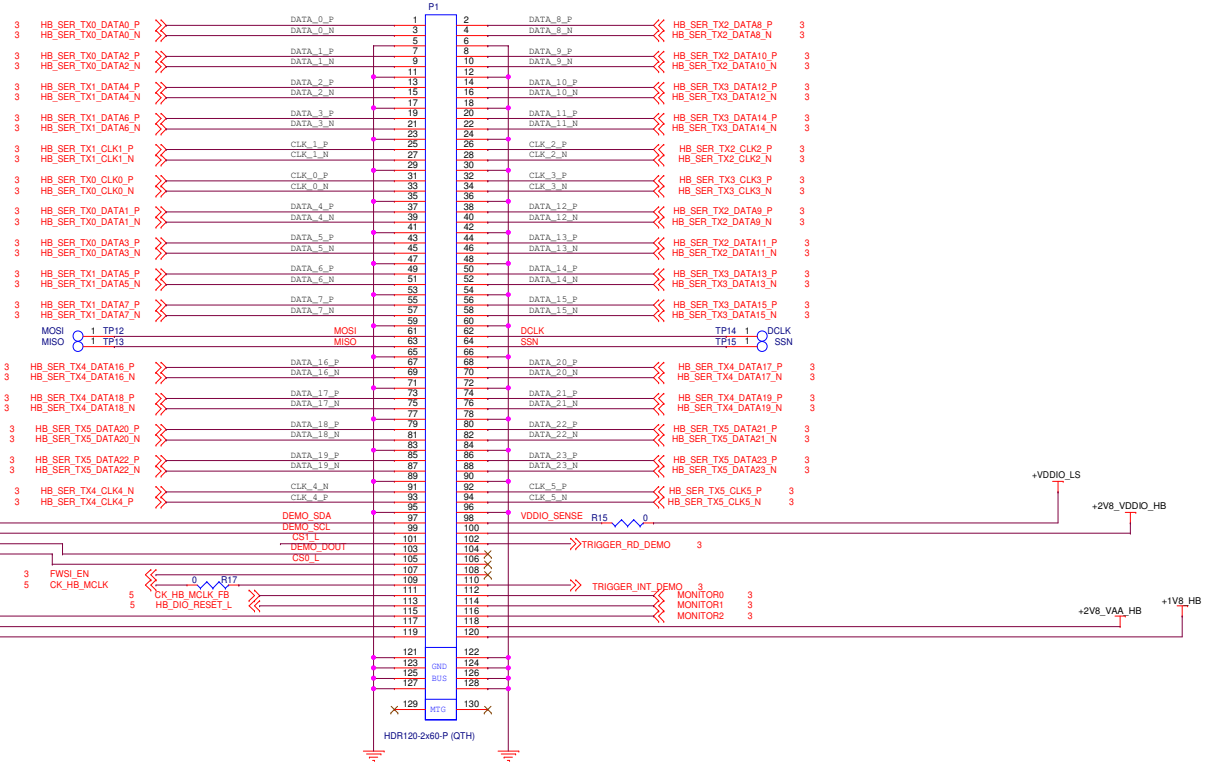
Script executed

ON Semiconductor

Title	Clock and Reset	
Size C	Document Name XGS12M_LGA171_SER_FBD_HEAD	Rev 1.1
Date: Tuesday, May 22, 2018	Sheet 5 of 6	

External Interface

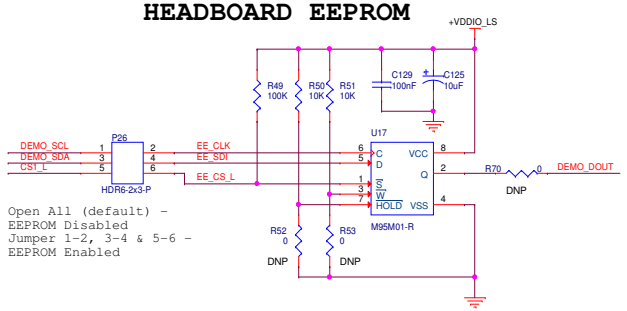




I2C / 4-WIRE DEBUG HEADER

P23
Jumper 1-2, 3-4, 5-6 & 7-8(default) - 4-WIRE Enabled
Jumper 1-2, 3-4 & 7-9 - I2C Enabled
Open All & Connect to external debugger - Test purpose

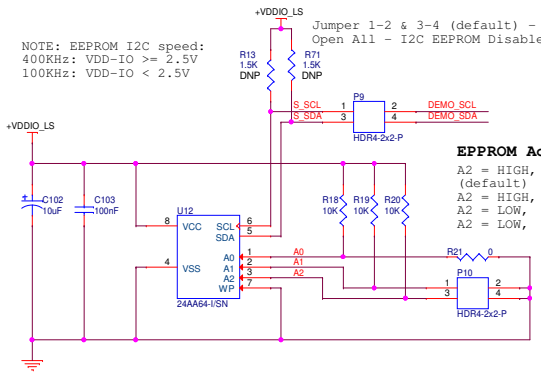
HEADBOARD EEPROM



LENS CORRECTION EEPROM

NOTE: EEPROM I2C speed:
400KHz: VDD-IO >= 2.5V
100KHz: VDD-IO < 2.5V

Jumper 1-2 & 3-4 (default) - I2C EEPROM Enabled
Open All - I2C EEPROM Disabled



EPPROM Address Switch Settings(P10):

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

ON Semiconductor

Title	External Interface	
Size C	Document Name XGS12M_LGA171_SER_FBD_HEAD	Rev 1.1
Date: Tuesday, May 22, 2018	Sheet 6 of 6	

Script executed

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:
NOIX1SE012KBLFB-GEVB