

# Intelligent Power Module (IPM)

Inverter, 1200 V, 25 A

## NFA32512L72

### General Description

NFA32512L72 is an advanced IPM module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's internal IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.

### Features

- 1200 V/25 A 3-phase FS7 IGBT Inverter with Integral Gate Drivers and Protections
- Built-in Under-Voltage Protection (UVP)
- Separated Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- LVIC Temperature-Sensing Built-In for Temperature Monitoring
- Isolation Rating: 2500 Vrms / 1 min.
- This Device is Pb-Free and is RoHS Compliant

### Typical Applications

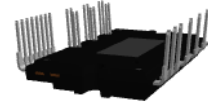
- Industrial Drives
- Industrial Pumps
- Industrial Fans
- Industrial Automation

### Integrated Power Functions

- 1200 V – 25 A IGBT inverter for three-phase DC / AC power conversion (Please refer to Figure 1)

### Integrated Drive, Protection and System Control Functions

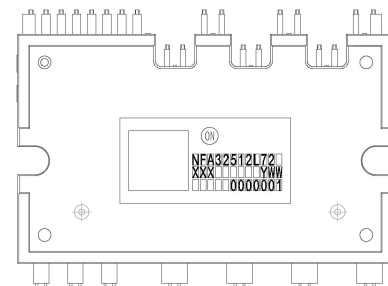
- For Inverter High-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out Protection (UVLO)
- For Inverter Low-side IGBTs: gate drive circuit, Over Current Protection (OCP) control supply circuit Under-Voltage Lock-Out Protection (UVLO)
- Fault Signaling: corresponding to UVLO (low-side supply) and over current faults
- Input Interface: active-HIGH interface, works with 3.3 / 5 V logic, Schmitt-trigger input



3D Package Drawing  
(Click to Active 3D Content)

SPMCA-027 / PDD STD, SPM27-CA, DBC TYPE  
CASE MODFJ

### MARKING DIAGRAM



NFA32512L72 = Specific Device Code  
 XXX = Last 3 Digits of Lot No  
 YWW = Year and Work Week Code  
 0000001 = Serial Number

### ORDERING INFORMATION

| Device      | Package  | Shipping        |
|-------------|----------|-----------------|
| NFA32512L72 | SPM27-CA | 10 Units / Tube |

# NFA32512L72

## PACKAGE MARKING AND ORDERING INFORMATION

| Device      | Device Marking | Package  | Packing Type | Quantity |
|-------------|----------------|----------|--------------|----------|
| NFA32512L72 | NFA32512L72    | SPM27-SB | Tube         | 10       |

## PIN CONFIGURATION

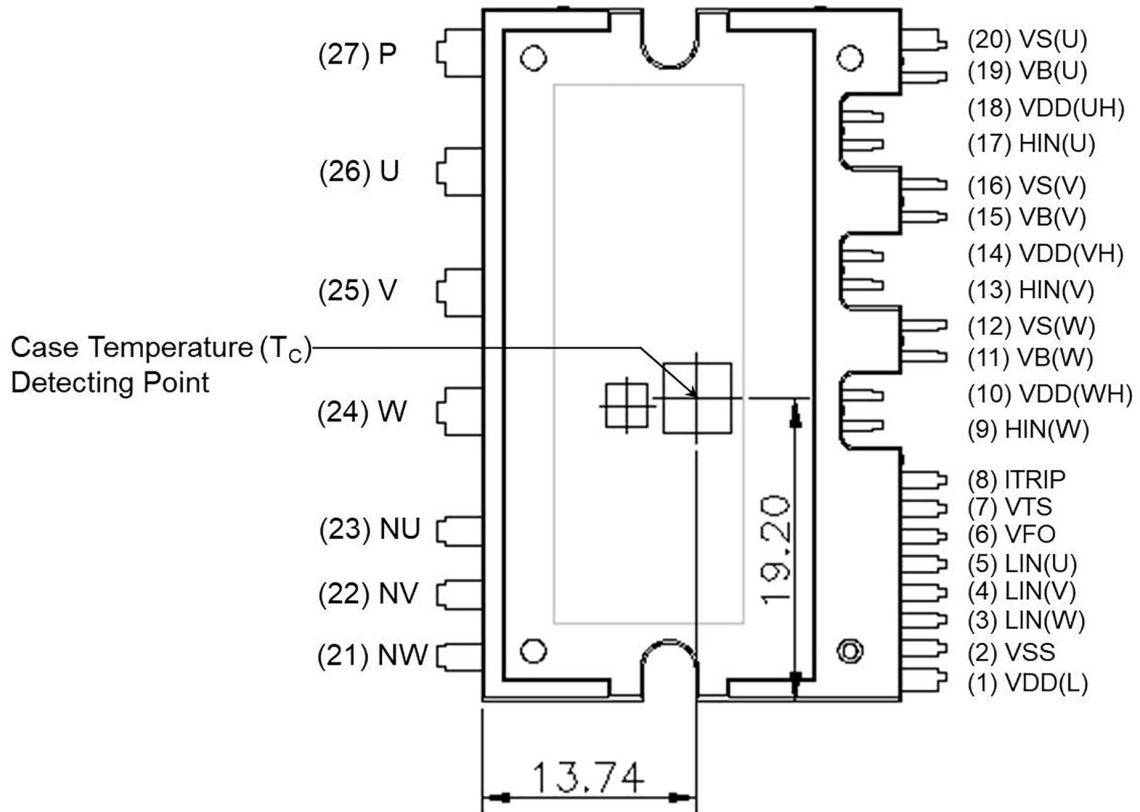


Figure 1. Pin Configuration

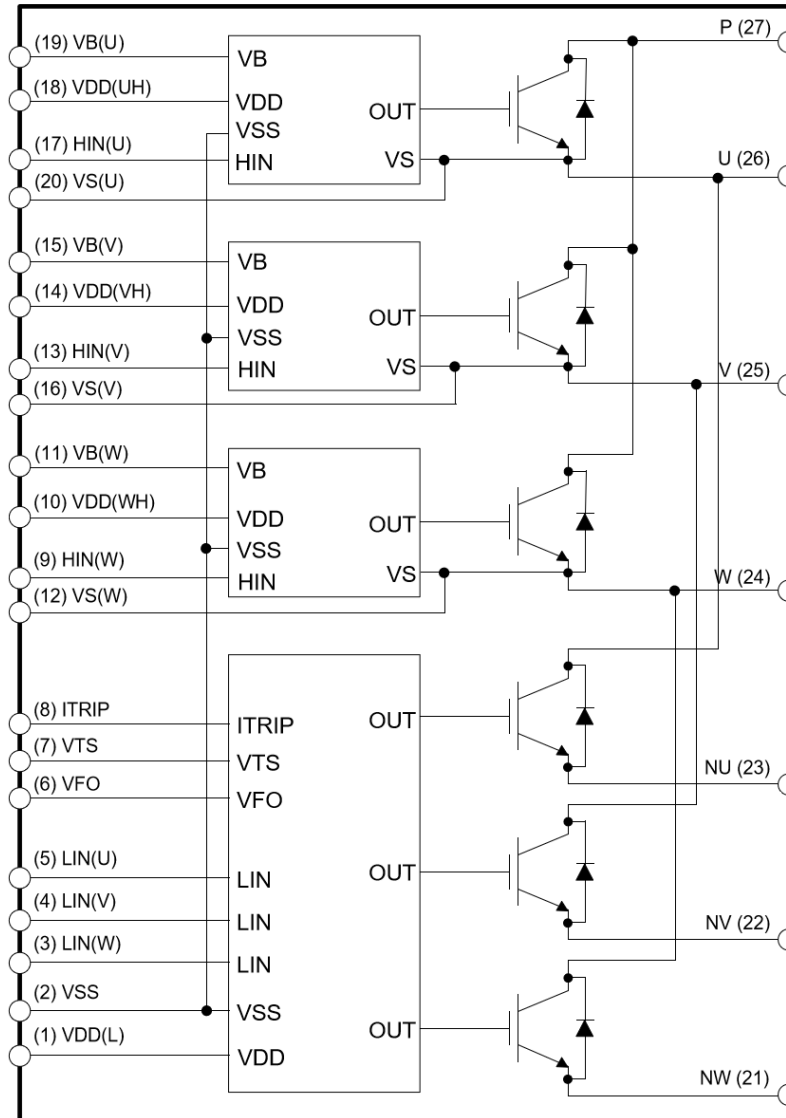
# NFA32512L72

## PIN DESCRIPTION

| Pin No. | Symbol  | Description                                            |
|---------|---------|--------------------------------------------------------|
| 1       | VDD(L)  | Low-Side Bias Voltage for IC and IGBTs Driving         |
| 2       | VSS     | Low-Side Common Supply Ground                          |
| 3       | LIN(W)  | Signal Input for Low-Side W-Phase                      |
| 4       | LIN(V)  | Signal Input for Low-Side V-Phase                      |
| 5       | LIN(U)  | Signal Input for Low-Side U-Phase                      |
| 6       | VFO     | Fault Output                                           |
| 7       | VTs     | Output for LVIC Temperature Sensing Voltage Output     |
| 8       | ITRIP   | Input for Over Current Protection                      |
| 9       | HIN(W)  | Signal Input for High-Side W-Phase                     |
| 10      | VDD(WH) | High-Side Bias Voltage for W-Phase IC                  |
| 11      | VB(W)   | High-Side Bias Voltage for W-Phase IGBT Driving        |
| 12      | VS(W)   | High-Side Bias Voltage Ground for W-Phase IGBT Driving |
| 13      | HIN(V)  | Signal Input for High-Side V-Phase                     |
| 14      | VDD(VH) | High-Side Bias Voltage for V-Phase IC                  |
| 15      | VB(V)   | High-Side Bias Voltage for V-Phase IGBT Driving        |
| 16      | VS(V)   | High-Side Bias Voltage Ground for V-Phase IGBT Driving |
| 17      | HIN(U)  | Signal Input for High-Side U-Phase                     |
| 18      | VDD(UH) | High-Side Bias Voltage for U-Phase IC                  |
| 19      | VB(U)   | High-Side Bias Voltage for U-Phase IGBT Driving        |
| 20      | VS(U)   | High-Side Bias Voltage Ground for U-Phase IGBT Driving |
| 21      | NW      | Negative DC-Link Input for W-Phase                     |
| 22      | NV      | Negative DC-Link Input for V-Phase                     |
| 23      | NU      | Negative DC-Link Input for U-Phase                     |
| 24      | W       | Output for W-Phase                                     |
| 25      | V       | Output for V-Phase                                     |
| 26      | U       | Output for U-Phase                                     |
| 27      | P       | Positive DC-Link Input                                 |

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## INTERNAL EQUIVALENT CIRCUIT AND INPUT/OUTPUT PINS



**Figure 2. Internal Block Diagram**

### NOTES:

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT, and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes, and three drive ICs for each IGBT.

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## ABSOLUTE MAXIMUM RATINGS (T<sub>j</sub> = 25°C unless otherwise specified)

| Symbol               | Parameter                          | Test Condition                                                                | Rating    | Unit |
|----------------------|------------------------------------|-------------------------------------------------------------------------------|-----------|------|
| <b>INVERTER PART</b> |                                    |                                                                               |           |      |
| VPN                  | Supply Voltage                     | Applied between P – NU, NV, NW                                                | 900       | V    |
| VPN (surge)          | Supply Voltage (Surge)             | Applied between P – NU, NV, NW                                                | 1000      | V    |
| V <sub>ces</sub>     | Collector–Emitter Voltage          | (Note 4)                                                                      | 1200      | V    |
| ±I <sub>c</sub>      | Each IGBT Collector Current        | T <sub>c</sub> = 25°C, T <sub>j</sub> ≤ 150°C (Note 5)                        | 25        | A    |
| ±I <sub>cp</sub>     | Each IGBT Collector Current (Peak) | T <sub>c</sub> = 25°C, T <sub>j</sub> ≤ 150°C, under 1ms Pulse Width (Note 5) | 50        | A    |
| P <sub>c</sub>       | Collector Dissipation              | T <sub>c</sub> = 25°C per One Chip (Note 5)                                   | 100       | W    |
| T <sub>j</sub>       | Operating Junction Temperature     |                                                                               | –40 ~ 150 | °C   |

## CONTROL PART

|        |                                |                                                                      |                  |    |
|--------|--------------------------------|----------------------------------------------------------------------|------------------|----|
| VDD    | Control Supply Voltage         | Applied between VDD(H), VDD(L) – VSS                                 | 20               | V  |
| VBS    | High–Side Control Bias Voltage | Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)          | 20               | V  |
| VIN    | Input Signal Voltage           | Applied between HIN(U), HIN(V), HIN(W), LIN(U), LIN(V), LIN(W) – VSS | –0.3 ~ VDD + 0.3 | V  |
| VFO    | Fault Output Supply Voltage    | Applied between VFO – VSS                                            | –0.3 ~ VDD + 0.3 | V  |
| IFO    | Fault Output Current           | Sink Current at VFO pin                                              | 2                | mA |
| VITRIP | Current Sensing Input Voltage  | Applied between ITRIP – VSS                                          | –0.3 ~ VDD + 0.3 | V  |

## TOTAL SYSTEM

|                  |                                                                           |                                                                           |           |                  |
|------------------|---------------------------------------------------------------------------|---------------------------------------------------------------------------|-----------|------------------|
| VPN (PROT)       | Self–Protection Supply Voltage Limit (Over Current Protection Capability) | VDD = VBS = 13.5 ~ 16.5 V, T <sub>j</sub> = 150°C, Non–repetitive, < 2 μs | 800       | V                |
| T <sub>c</sub>   | Case Operation Temperature                                                | See Figure 1                                                              | –40 ~ 125 | °C               |
| T <sub>stg</sub> | Storage Temperature                                                       |                                                                           | –40 ~ 125 | °C               |
| V <sub>iso</sub> | Isolation Voltage                                                         | 60 Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat Sink Plate        | 2500      | V <sub>rms</sub> |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. This is not for continuous DC voltage. Recommend to use max 960 V (80% of rated voltage) for continuous DC voltage.

5. These values had been made by the calculation considered to design factor.

## THERMAL RESISTANCE

| Symbol                | Parameter                           | Test Condition                      | Min | Typ | Max  | Unit |
|-----------------------|-------------------------------------|-------------------------------------|-----|-----|------|------|
| R <sub>th(j–c)Q</sub> | Junction to Case Thermal Resistance | Inverter IGBT part (per 1/6 module) | –   | –   | 1.25 | °C/W |
| R <sub>th(j–c)F</sub> |                                     | Inverter FWDi part (per 1/6 module) | –   | –   | 1.75 | °C/W |
| L <sub>σ</sub>        | Package Stray Inductance            | P to NU, NV, NW (Note 6)            | –   | 24  | –    | nH   |

6. Stray inductance per phase measured per IEC 60747–15.

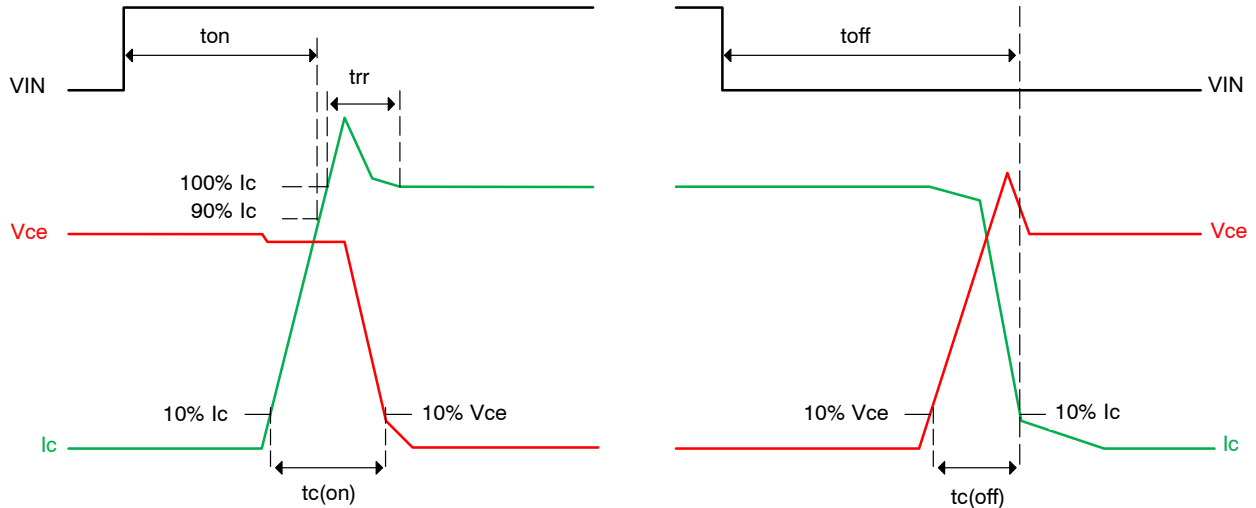
**ELECTRICAL CHARACTERISTICS** ( $T_j = 25^\circ\text{C}$  unless otherwise specified)

| Symbol               | Parameter                            | Test Condition                                                                                               | Min  | Typ  | Max  | Unit |
|----------------------|--------------------------------------|--------------------------------------------------------------------------------------------------------------|------|------|------|------|
| <b>INVERTER PART</b> |                                      |                                                                                                              |      |      |      |      |
| VCE(sat)             | Collector-Emitter Saturation Voltage | VDD = VBS = 15 V, VIN = 5 V, Ic = 20 A, Tj = 25°C                                                            | –    | 1.5  | 1.9  | V    |
|                      |                                      | VDD = VBS = 15 V, VIN = 5V, Ic = 20 A, Tj = 150°C                                                            | –    | 1.75 | –    |      |
| VF                   | FWDi Forward Voltage                 | VIN = 0 V, IF = 20 A, Tj = 25°C                                                                              | –    | 1.7  | 2.1  | V    |
|                      |                                      | VIN = 0 V, IF = 20 A, Tj = 150°C                                                                             | –    | 1.65 | –    |      |
| HS                   | ton                                  | VPN = 600 V, VDD = 15 V, Ic = 20 A, Tj = 25°C<br>VIN = 0 V ↔ 5 V, Inductive Load<br>See Figure 3<br>(Note 7) | 0.90 | 1.05 | 1.20 | μs   |
|                      | tc(on)                               |                                                                                                              | –    | 0.12 | 0.30 |      |
|                      | toff                                 |                                                                                                              | –    | 1.15 | 1.25 |      |
|                      | tc(off)                              |                                                                                                              | –    | 0.25 | 0.35 |      |
|                      | trr                                  |                                                                                                              | –    | 0.20 | –    |      |
| LS                   | ton                                  | VPN = 600 V, VDD = 15 V, Ic = 20 A, Tj = 25°C<br>VIN = 0 V ↔ 5 V, Inductive Load<br>See Figure 3<br>(Note 7) | 0.60 | 0.75 | 0.95 | μs   |
|                      | tc(on)                               |                                                                                                              | –    | 0.18 | 0.30 |      |
|                      | toff                                 |                                                                                                              | –    | 1.07 | 1.17 |      |
|                      | tc(off)                              |                                                                                                              | –    | 0.25 | 0.35 |      |
|                      | trr                                  |                                                                                                              | –    | 0.20 | –    |      |
| Ices                 | Collector – Emitter Leakage Current  | Tj = 25°C, VCE = VCES                                                                                        | –    | –    | 1    | mA   |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay time of the internal drive IC.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 3.

**SWITCHING TIME DEFINITION**



**Figure 3. Switching Time Definition**

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## ELECTRICAL CHARACTERISTICS (T<sub>j</sub> = 25°C unless otherwise specified)

| Symbol              | Parameter                               | Test Condition                                                                                      | Min                                               | Typ  | Max  | Unit    |
|---------------------|-----------------------------------------|-----------------------------------------------------------------------------------------------------|---------------------------------------------------|------|------|---------|
| <b>CONTROL PART</b> |                                         |                                                                                                     |                                                   |      |      |         |
| IQDDH               | Quiescent VDD Supply Current            | VDD(H) = 15 V,<br>HIN(U,V,W) = 0 V                                                                  | VDD(H) – VSS                                      | –    | –    | 0.15 mA |
| IQDDL               |                                         | VDD(L) = 15 V,<br>LIN(U,V,W) = 0 V                                                                  | VDD(L) – VSS                                      | –    | –    | 5.00 mA |
| IPDDH               | Operating VDD Supply Current            | VDD(H) = 15 V, fPWM = 20 kHz,<br>duty = 50%, applied to one PWM<br>signal input for High-Side       | VDD(H) – VSS                                      | –    | –    | 0.30 mA |
| IPDDL               |                                         | VDD(L) = 15 V, fPWM = 20 kHz,<br>duty = 50%, applied to one PWM<br>signal input for Low-Side        | VDD(L) – VSS                                      | –    | –    | 6 mA    |
| IQBS                | Quiescent VBS Supply Current            | VBS = 15 V, HIN(U,V,W) = 0 V                                                                        | VB(U) – VS(U),<br>VB(V) – VS(V),<br>VB(W) – VS(W) | –    | –    | 0.30 mA |
| IPBS                | Operating VBS Supply Current            | VDD = VBS = 15 V,<br>fPWM = 20 kHz, duty = 50%,<br>applied to one PWM signal input<br>for High-Side | VB(U) – VS(U),<br>VB(V) – VS(V),<br>VB(W) – VS(W) | –    | –    | 2.50 mA |
| VFOH                | Fault Output Voltage                    | VDD = 15 V, VITRIP = 0 V, 4.7 kΩ Pull-up to 5 V                                                     | 4.5                                               | –    | –    | V       |
| VFOL                |                                         | VDD = 15 V, VITRIP = 1 V, 4.7 kΩ Pull-up to 5 V                                                     | –                                                 | –    | 0.5  | V       |
| VITRIP              | Over Current Trip Level                 | VDD = 15 V (Note 8)                                                                                 | ITRIP – VSS                                       | 0.45 | 0.50 | 0.55 V  |
| UVDDD               | Supply Circuit Under-Voltage Protection | Detection Level                                                                                     | 10.3                                              | –    | 12.8 | V       |
| UVDDR               |                                         | Reset Level                                                                                         | 10.8                                              | –    | 13.3 | V       |
| UVBSD               |                                         | Detection Level                                                                                     | 9.5                                               | –    | 12.0 | V       |
| UVBSR               |                                         | Reset Level                                                                                         | 10.0                                              | –    | 12.5 | V       |
| tFOD                | Fault-Out Pulse Width                   |                                                                                                     | 50                                                | –    | –    | μs      |
| VTS                 | LVIC Temperature Sensing Voltage Output | VDD(L) = 15 V, TLVIC = 25°C (Note 9)<br>See Figure 4                                                | 0.88                                              | 0.98 | 1.08 | V       |
| VIN(ON)             | ON Threshold Voltage                    | Applied between HIN(U,V,W) – VSS,<br>LIN(U,V,W) – VSS                                               | –                                                 | –    | 2.6  | V       |
| VIN(OFF)            | OFF Threshold Voltage                   |                                                                                                     | 0.8                                               | –    | –    | V       |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Over current protection is functioning only at the low-sides.

9. T<sub>LVIC</sub> is the temperature of LVIC itself. V<sub>TS</sub> is only for sensing temperature of LVIC and can not shutdown IGBTs automatically.

RECOMMENDED OPERATING CONDITIONS

| Symbol                  | Parameter                                | Test Conditions                                                                                                   | Min  | Min  | Max  | Unit               |
|-------------------------|------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------|------|------|--------------------|
| VPN                     | Supply Voltage                           | Applied between P – NU, NV, NW                                                                                    | –    | 600  | 800  | V                  |
| VDD                     | Control Supply Voltage                   | Applied between VDD(H) – VSS, VDD(L) – VSS                                                                        | 13.5 | 15.0 | 16.5 | V                  |
| VBS                     | High-Side Bias Voltage                   | Applied between VB(U) – VS(U), VB(V) – VS(V), VB(W) – VS(W)                                                       | 13.0 | 15.0 | 18.5 | V                  |
| dVDD / dt,<br>dVBS / dt | Control Supply Variation                 |                                                                                                                   | –1   | –    | 1    | V/ $\mu$ s         |
| Tdead                   | Blanking Time for Preventing Arm – Short | For Each Input Signal                                                                                             | 1.5  | –    | –    | $\mu$ s            |
| fPWM                    | PWM Input Signal                         | $-40^{\circ}\text{C} \leq T_c \leq 125^{\circ}\text{C}$ , $-40^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$ | –    | –    | 20   | kHz                |
| VSEN                    | Voltage for Current Sensing              | Applied between NU, NV, NW – VSS (Including Surge Voltage)                                                        | –5   | –    | 5    | V                  |
| PWIN(ON)                | Minimum Input Pulse Width                | VDD = VBS = 15 V, $I_c \leq 50$ A, Wiring Inductance between NU, V, W and DC Link N < 10 nH (Note 10)             | 1.5  | –    | –    | $\mu$ s            |
| PWIN(OFF)               |                                          |                                                                                                                   | 2.0  | –    | –    | $\mu$ s            |
| Tj                      | Junction Temperature                     |                                                                                                                   | –40  | –    | 150  | $^{\circ}\text{C}$ |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

10. This product might not make response if input pulse width is less than the recommended value.

TEMPERATURE PROFILE OF VTS (TYPICAL)

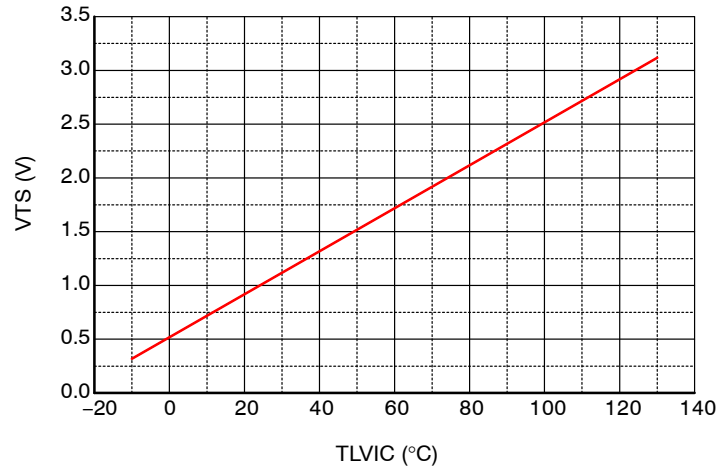


Figure 4. Temperature Profile of VTS (Typical)

# MECHANICAL CHARACTERISTICS AND RATINGS

| Parameter                 | Conditions                         |                          | Min | Typ | Max  | Unit    |
|---------------------------|------------------------------------|--------------------------|-----|-----|------|---------|
| Device Flatness           | See Figure 5                       |                          | 0   | –   | +150 | μm      |
| Mounting Torque           | Mounting Screw: M3<br>See Figure 6 | Recommended 0.7 N • m    | 0.6 | 0.7 | 0.8  | N • m   |
|                           |                                    | Recommended 7.1 kg N • m | 6.2 | 7.1 | 8.1  | kg • cm |
| Terminal Pulling Strength | Load 19.6 N                        |                          | 10  | –   | –    | s       |
| Terminal Bending Strength | Load 9.8 N, 90 deg. bend           |                          | 2   | –   | –    | times   |
| Weight                    |                                    |                          | –   | 15  | –    | g       |

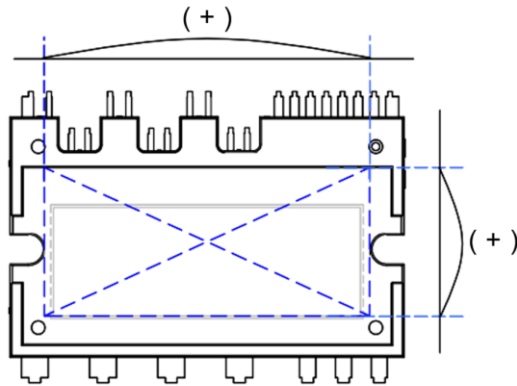


Figure 5. Flatness Measurement Position

## MOUNTING SCREW TORQUE ORDER

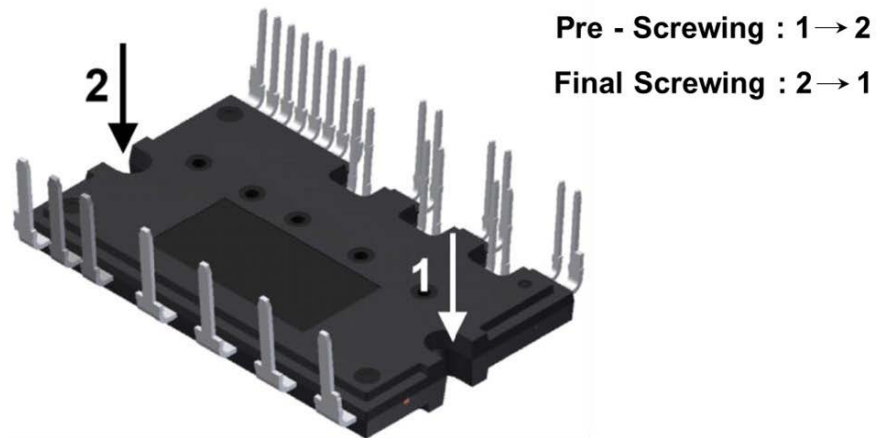
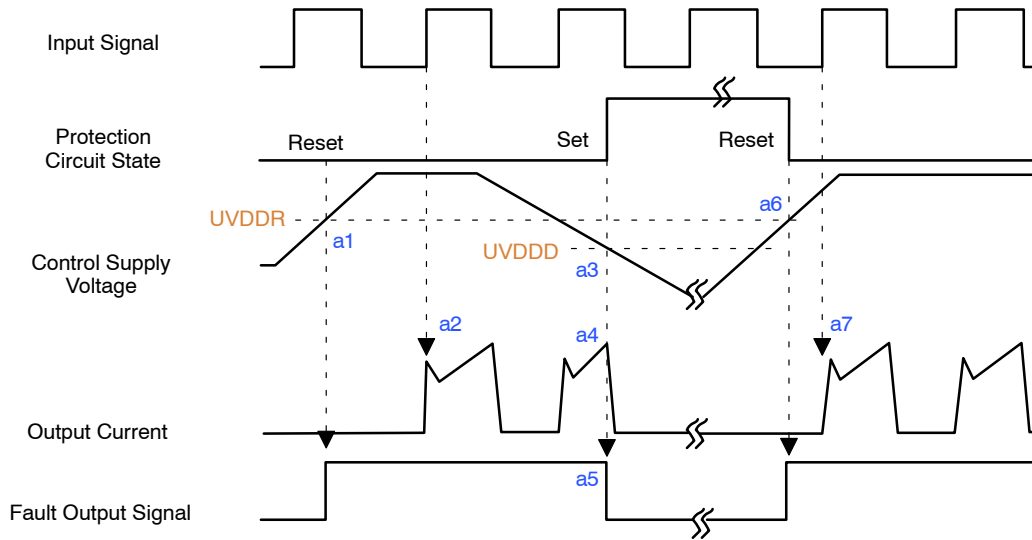


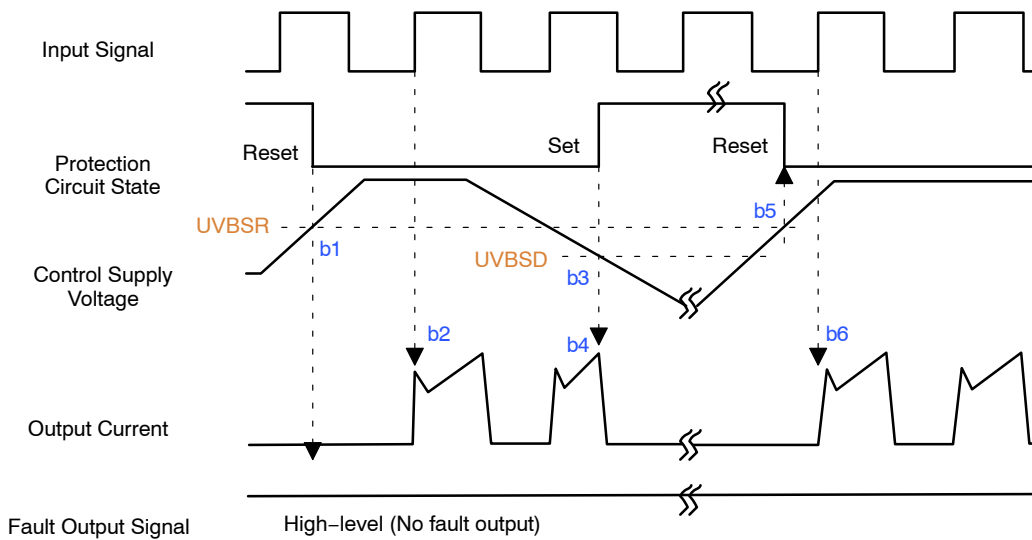
Figure 6. Mounting Screws Torque Order

# TIME CHARTS OF PROTECTIVE FUNCTION



**Figure 7. Under-Voltage Protection (Low-Side)**

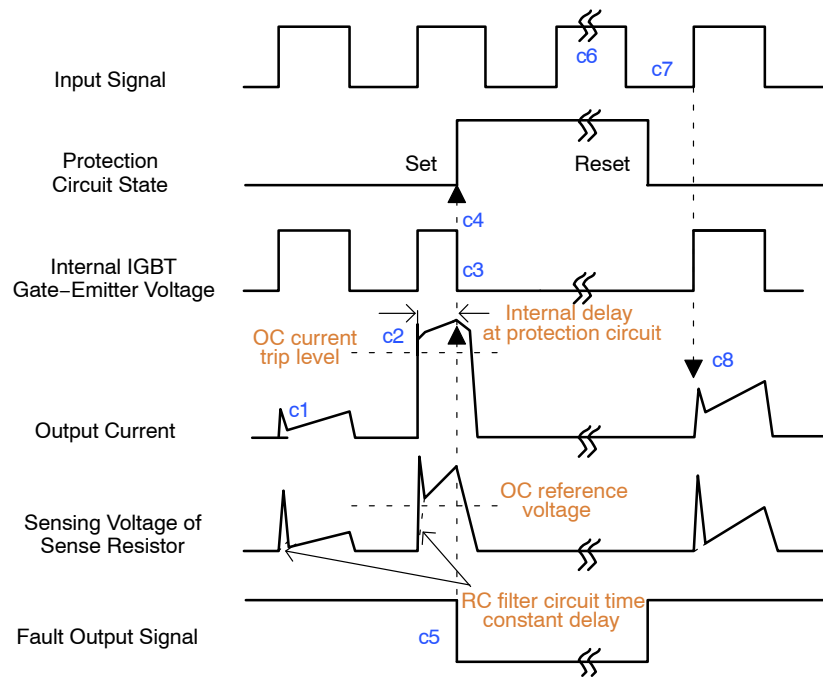
- a1: Control supply voltage rises: After the voltage rises UVDDR, the circuits start to operate when next input is applied.
- a2: Normal operation: IGBT ON and carrying current.
- a3: Under voltage detection (UVDDD).
- a4: IGBT OFF in spite of control input condition.
- a5: Fault output operation starts with a fixed pulse width.
- a6: Under voltage reset (UVDDR).
- a7: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.



**Figure 8. Under-Voltage Protection (High-Side)**

- b1: Control supply voltage rises: After the voltage reaches UVBSR, the circuits start to operate when next input is applied.
- b2: Normal operation: IGBT ON and carrying current.
- b3: Under voltage detection (UVBSD).
- b4: IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5: Under voltage reset (UVBSR).
- b6: Normal operation: IGBT ON and carrying current by triggering next signal from LOW to HIGH.

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**Figure 9. Over Current Protection (Low –Side Operation Only)**

(with the external sense resistance and RC filter connection)

c1: Normal operation: IGBT ON and carrying current.

c2: Over current detection (OC trigger).

c3: All low-side IGBT gate are hard interrupted.

c4: All low-side IGBTs turn OFF.

c5: Fault output operation starts with a fixed pulse width.

c6: Input HIGH: IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c7: Fault output operation finishes, but IGBT doesn't turn on until triggering next signal from LOW to HIGH.

c8: Normal operation: IGBT ON and carrying current.

## TYPICAL APPLICATION CIRCUIT

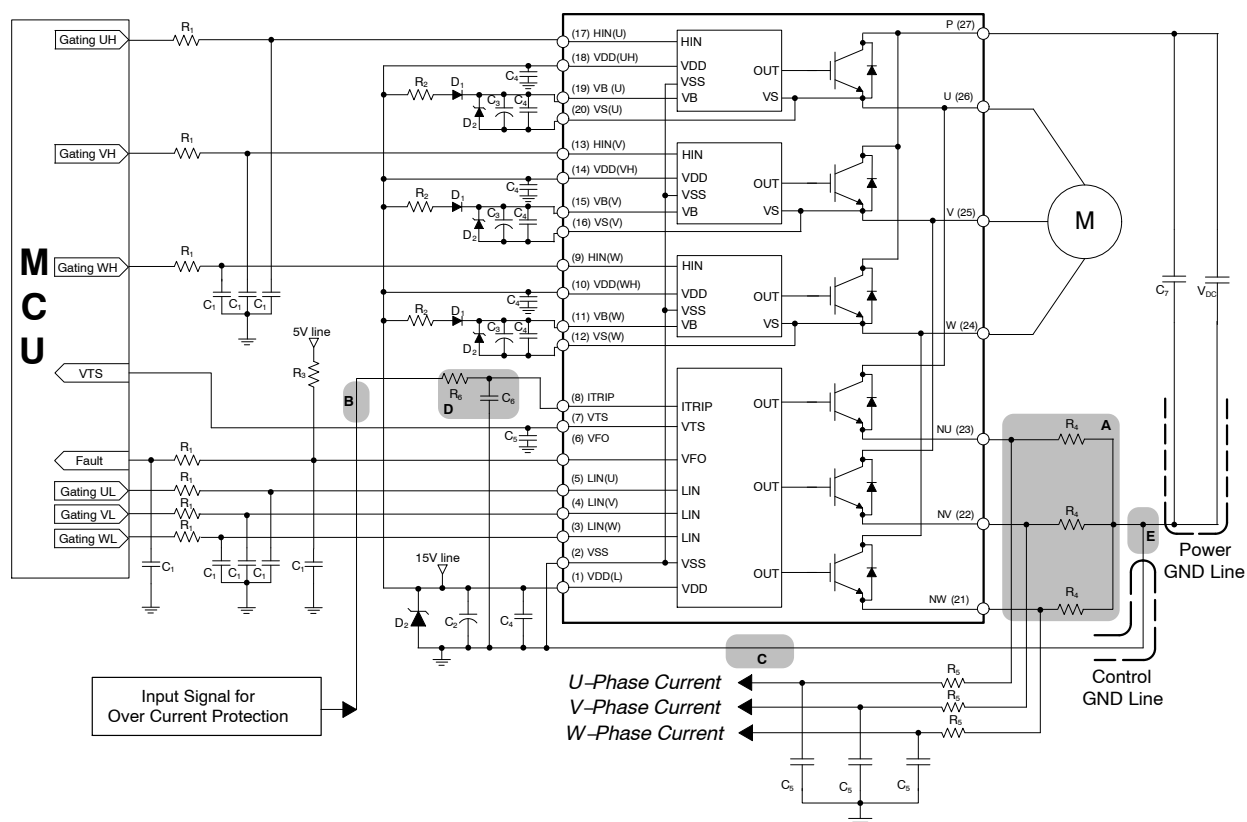


Figure 10. Typical Application Circuit

## NOTES:

11. To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 ~ 3 cm)
12.  $V_{FO}$  output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes  $I_{FO}$  up to 2 mA.
13. Input signal is active-HIGH type. There is a 5 k $\Omega$  resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation.  $R_1C_1$  time constant should be selected in the range 50 ~ 150 ns. (Recommended  $R_1 = 100 \Omega$ ,  $C_1 = 1 \text{ nF}$ )
14. Each wiring pattern inductance of A point should be minimized (Recommend less than 10 nH). Use the shunt resistor  $R_4$  of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring of point E should be connected to the terminal of the shunt resistor  $R_4$  as close as possible.
15. To prevent errors of the protection function, the wiring of B, C, and D point should be as short as possible.
16. In the over current protection circuit, please select the  $R_6C_6$  time constant in the range 1.5 ~ 2  $\mu\text{s}$ . Do enough evaluation on the real system because over current protection time may vary wiring pattern layout and value of the  $R_6C_6$  time constant.
17. Each capacitor should be mounted as close to the pins of the product as possible.
18. To prevent surge destruction, the wiring between the snubber capacitor  $C_7$  and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22  $\mu\text{F}$  between the P & GND pins is recommended.
19. Relays are used at almost every systems of electrical equipment at industrial application. In these cases, there should be sufficient distance between the CPU and the relays.
20. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15  $\Omega$ ).
21.  $C_2$  of around 7 times larger than bootstrap capacitor  $C_3$  is recommended.
22. Please choose the electrolytic capacitor with good temperature characteristic in  $C_3$ . Also, choose 0.1 ~ 0.2  $\mu\text{F}$  R-category ceramic capacitors with good temperature and frequency characteristics in  $C_4$ .

TYPICAL CHARACTERISTICS

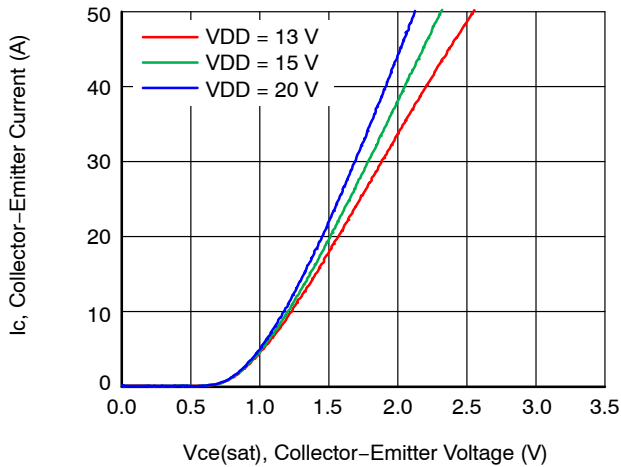


Figure 11. Typ. Collector-Emitter Saturation Voltage

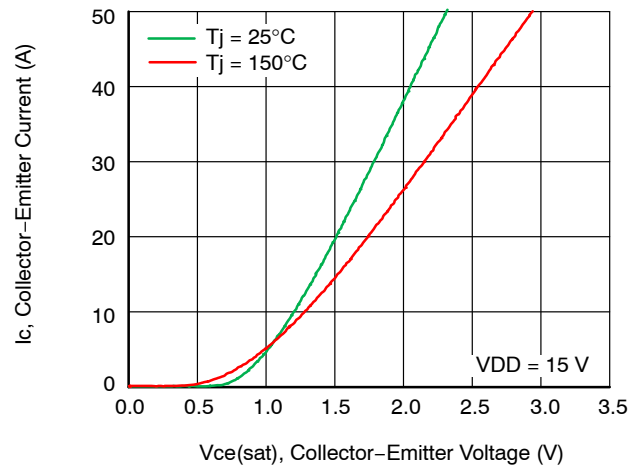


Figure 12. Typ. Collector-Emitter Saturation Voltage

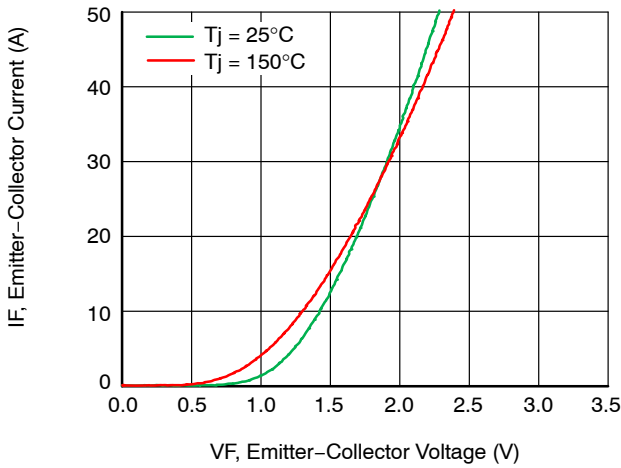


Figure 13. Typ. Emitter-Collector Forward Voltage

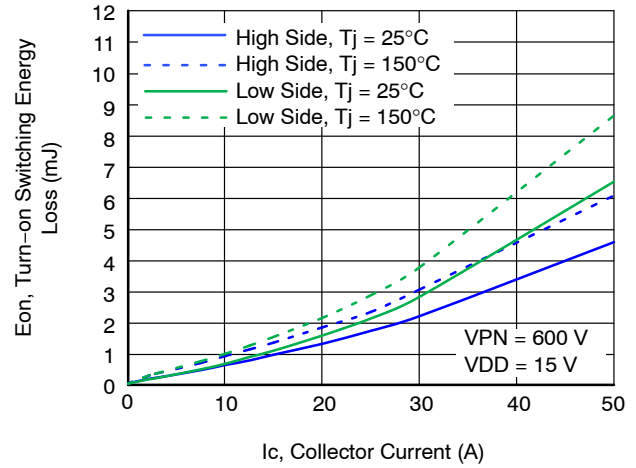


Figure 14. Typ. Turn-on Switching Energy Loss

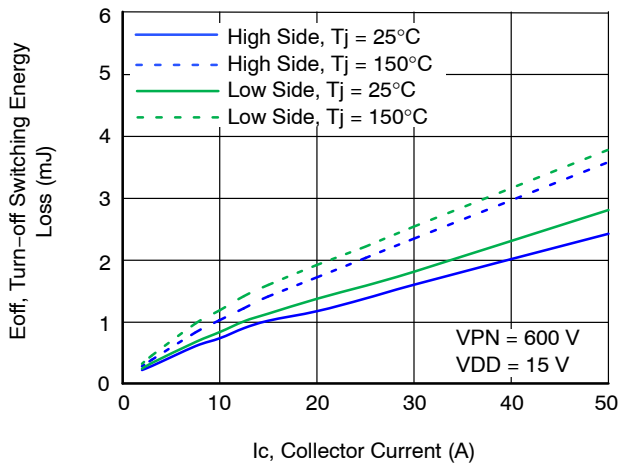


Figure 15. Typ. Turn-off Switching Energy Loss

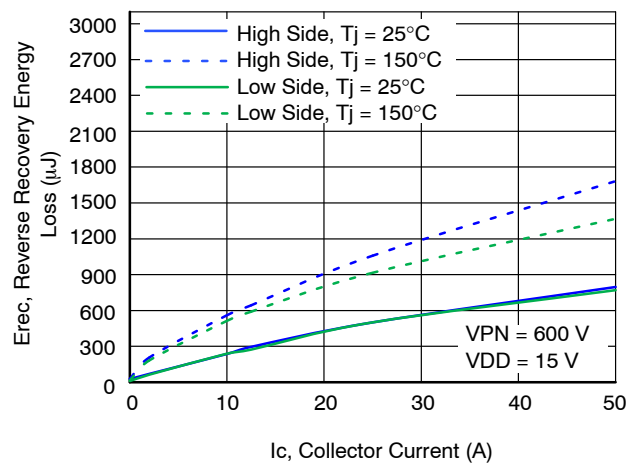


Figure 16. Typ. Reverse Recovery Energy Loss

## TYPICAL CHARACTERISTICS

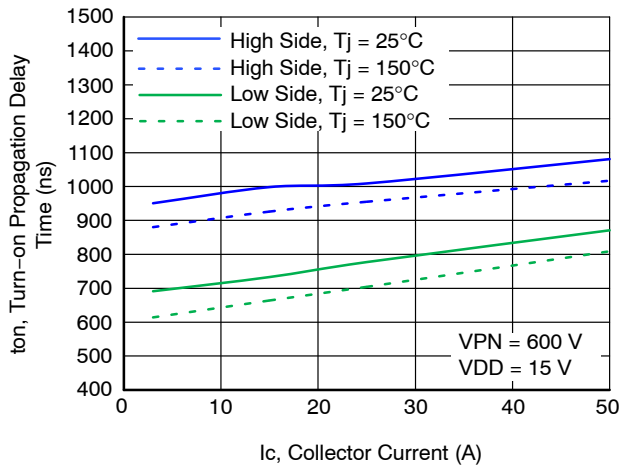


Figure 17. Typ. Turn-on Propagation Delay Time

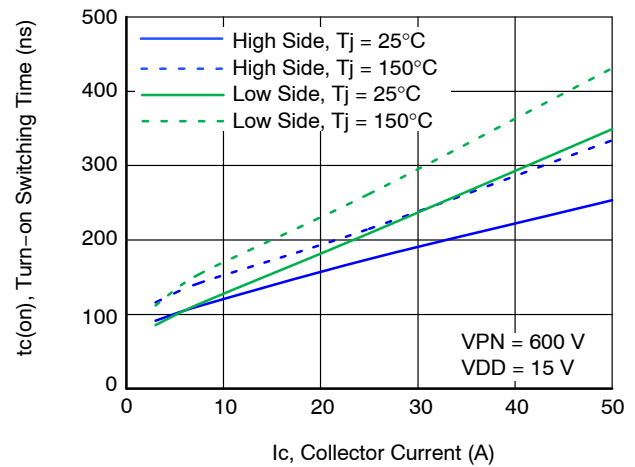


Figure 18. Typ. Turn-on Switching Time

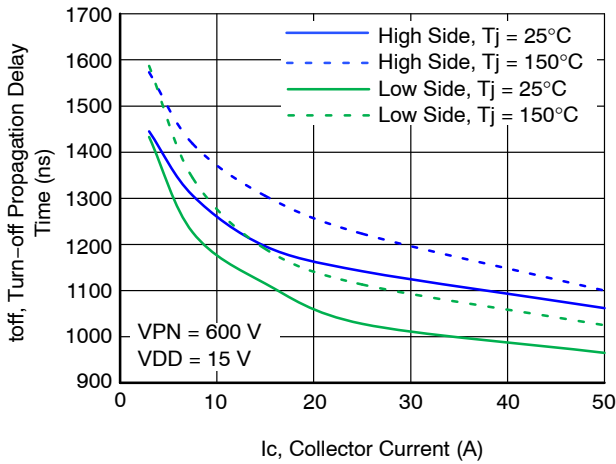


Figure 19. Typ. Turn-off Propagation Delay Time

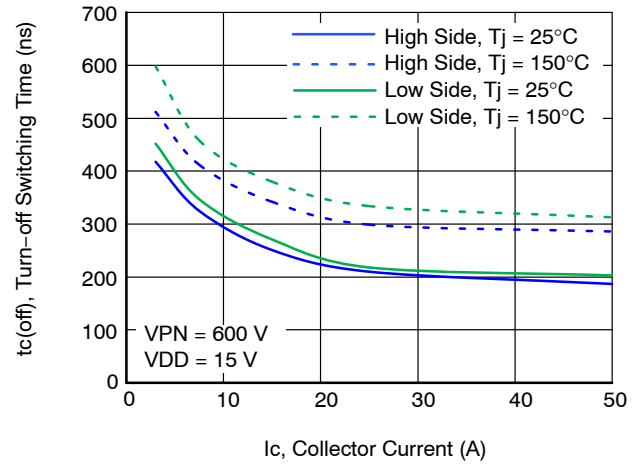


Figure 20. Typ. Turn-off Switching Time

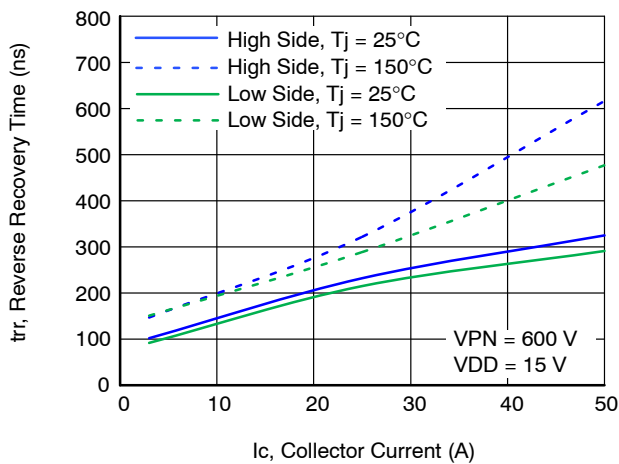


Figure 21. Typ. Reverse Recovery Time

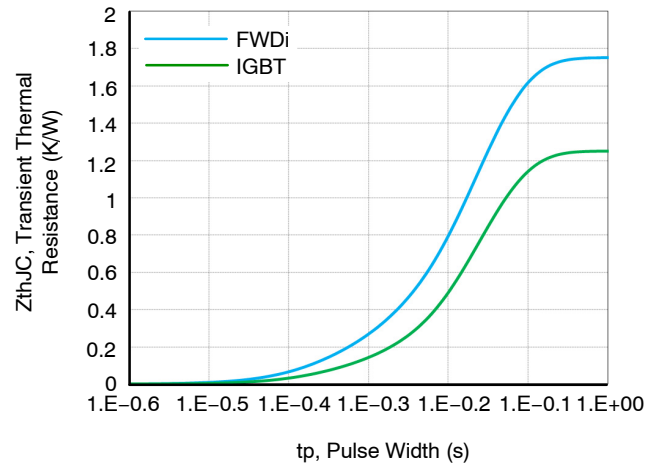


Figure 22. Transient Thermal Resistance

TURN-ON/OFF SWITCHING WAVEFORM

Switching conditions:  $V_{DC} = 600\text{ V}$ ,  $V_{DD} = 15\text{ V}$ ,  $T_j = 25^\circ\text{C}$ ,  $I_c = 20\text{ A}$

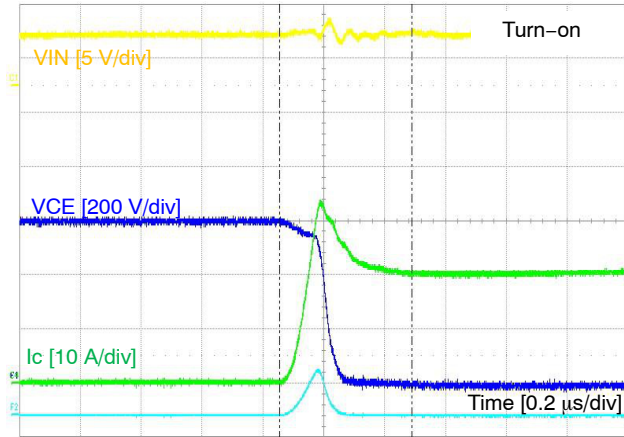


Figure 23. Turn-on Switching Waveform

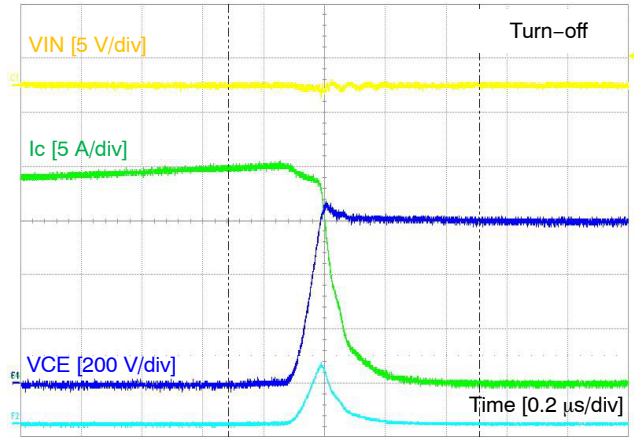
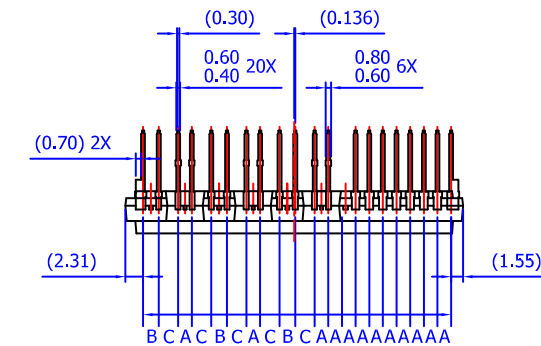


Figure 24. Turn-off Switching Waveform

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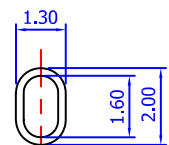
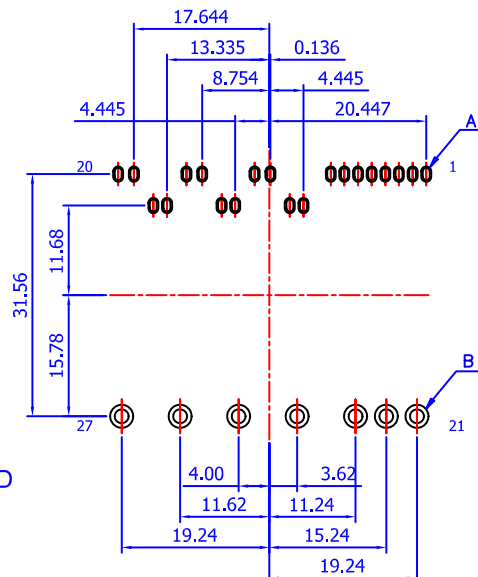
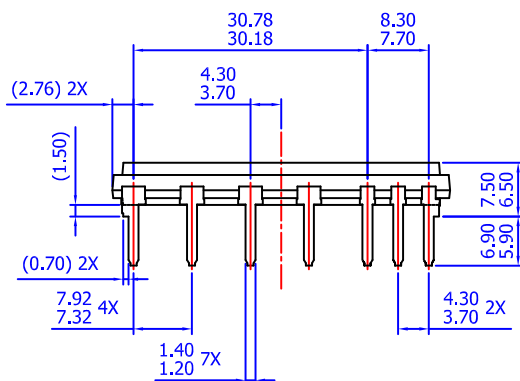
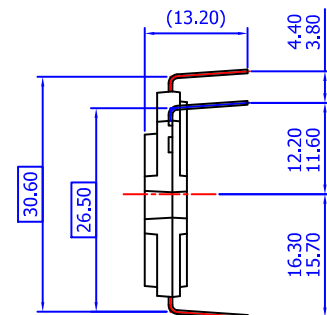
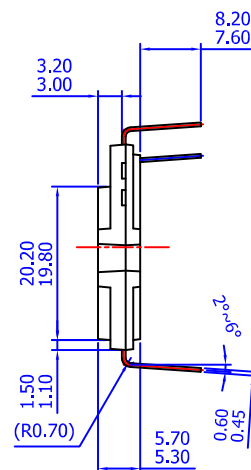
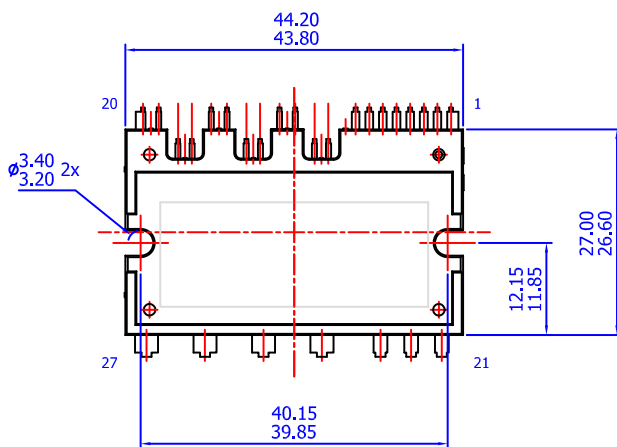


LEAD PITCH (TOLERANCE :  $\pm 0.30$ )

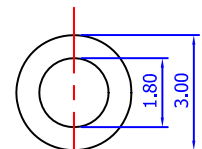
A : 1.778

B : 2.050

C : 2.531



DETAIL A  
(SCALE N/A)



DETAIL B  
(SCALE N/A)

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