NCP3170

Synchronous PWM Switching Converter

The NCP3170 is a flexible synchronous PWM Switching Buck Regulator. The NCP3170 operates from 4.5 V to 18 V, sourcing up to 3 A and is capable of producing output voltages as low as 0.8 V. The NCP3170 also incorporates current mode control. To reduce the number of external components, a number of features are internally set including soft start, power good detection, and switching frequency. The NCP3170 is currently available in an SOIC−8 package.

Features

- 4.5 V to 18 V Operating Input Voltage Range
- 90 mΩ High-Side, 25 mΩ Low-Side Switch
- FMEA Fault Tolerant During Pin Short Test
- 3 A Continuous Output Current
- Fixed 500 kHz and 1 MHz PWM Operation
- Cycle-by-Cycle Current Monitoring
- 1.5% Initial Output Accuracy
- Internal 4.6 ms Soft-Start
- Short-Circuit Protection
- Turn on Into Pre-bias
- Power Good Indication
- Light Load Efficiency
- Thermal Shutdown
- These are Pb-Free Devices

Typical Applications

- Set Top Boxes
- DVD/Blu−ray™ Drives and HDD
- LCD Monitors and TVs
- Cable Modems
- PCIe Graphics Cards
- Telecom/Networking/Datacom Equipment
- Point of Load DC/DC Converters

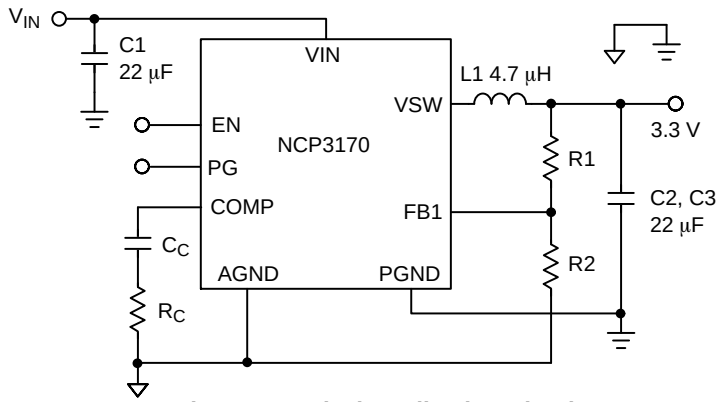


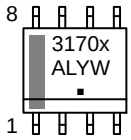
Figure 1. Typical Application Circuit

ON Semiconductor®

www.onsemi.com

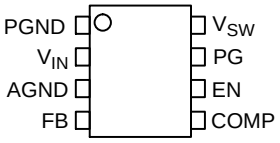
SOIC−8 NB
CASE 751

MARKING DIAGRAM



3170x	= Specific Device Code
x	= A or B
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP3170ADR2G	SOIC−8 (Pb−Free)	2,500/Tape & Reel
NCP3170BDR2G	SOIC−8 (Pb−Free)	2,500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

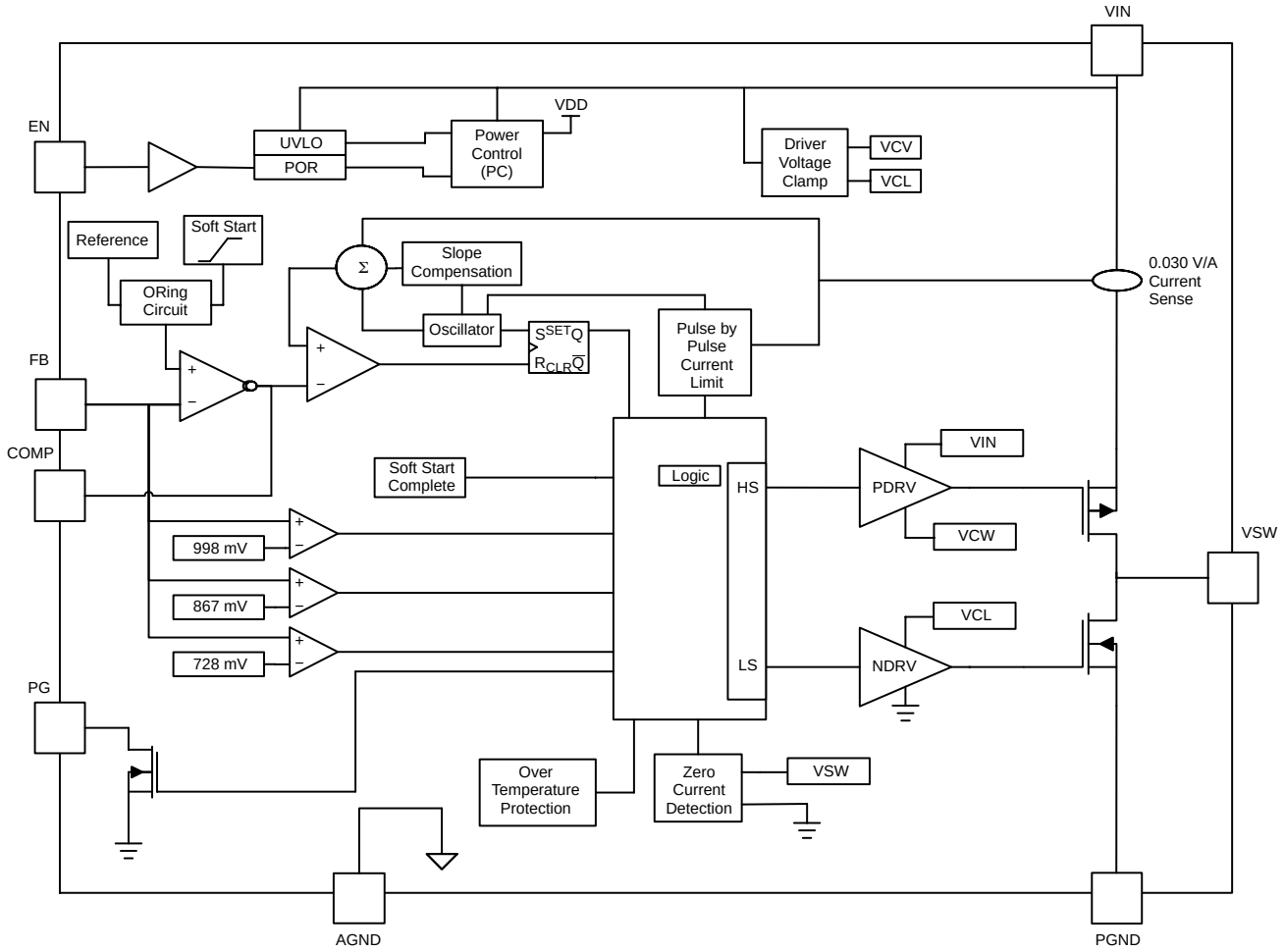


Figure 2. NCP3170 Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Pin Name	Description
1	PGND	The power ground pin is the high current path for the device. The pin should be soldered to a large copper area to reduce thermal resistance. PGND needs to be electrically connected to AGND.
2	VIN	The input voltage pin powers the internal control circuitry and is monitored by multiple voltage comparators. The VIN pin is also connected to the internal power PMOS switch and linear regulator output. The VIN pin has high di/dt edges and must be decoupled to ground close to the pin of the device.
3	AGND	The analog ground pin serves as small-signal ground. All small-signal ground paths should connect to the AGND pin and should also be electrically connected to power ground at a single point, avoiding any high current ground returns.
4	FB	Inverting input to the OTA error amplifier. The FB pin in conjunction with the external compensation serves to stabilize and achieve the desired output voltage with current mode compensation.
5	COMP	The loop compensation pin is used to compensate the transconductance amplifier which stabilizes the operation of the converter stage. Place compensation components as close to the converter as possible. Connect a RC network between COMP and AGND to compensate the control loop.
6	EN	Enable pin. Pull EN to logic high to enable the device. Pull EN to logic low to disable the device. Do not leave it open.
7	PG	Power good is an open drain 500 μA pull down indicating output voltage is within the power good window. If the power good function is not used, it can be connected to the VSW node to reduce thermal resistance. Do not connect PG to the VSW node if the application is turning on into pre-bias.
8	VSW	The VSW pin is the connection of the drains of the internal N and P MOSFETS. At switch off, the inductor will drive this pin below ground as the body diode and the NMOS conducts with a high dv/dt.

Table 2. ABSOLUTE MAXIMUM RATINGS (measured vs. GND pin 3, unless otherwise noted)

Rating	Symbol	V_{MAX}	V_{MIN}	Unit
Main Supply Voltage Input	V_{IN}	20	−0.3	V
Voltage between PGND and AGND	V_{PAG}	0.3	−0.3	V
PWM Feedback Voltage	F_B	6	−0.3	V
Error Amplifier Voltage	COMP	6	−0.3	V
Enable Voltage	EN	V_{IN} + 0.3 V	−0.3	V
PG Voltage	PG	V_{IN} + 0.3 V	−0.3	V
VSW to AGND or PGND	V_{SW}	V_{IN} + 0.3 V	−0.7	V
VSW to AGND or PGND for 35ns	V_{SWST}	V_{IN} + 10 V	−5	V
Junction Temperature (Note 1)	T_J	+150		°C
Operating Ambient Temperature Range	T_A	−40 to +85		°C
Storage Temperature Range	T_{stg}	− 55 to +150		°C
Thermal Characteristics (Note 2) SOIC−8 Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction-to-Air Thermal Resistance Junction-to-Case	 P_D $R_{\theta JA}$ RθJC	 1.15 87 37.8		 W °C/W °C/W
Lead Temperature Soldering (10 sec): Reflow (SMD Styles Only) Pb-Free (Note 3)	RF	260 peak		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

2. The value of θJA is measured with the device mounted on 2in x 2in FR−4 board with 2oz. copper, in a still air environment with T_A = 25°C. The value in any given application depends on the user's specific board design.
3. 60−180 seconds minimum above 237°C.

Table 3. RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Min	Max	Unit
Main Supply Voltage Input	VIN	4.5	18	V
Power Good Pin Voltage	PG	0	18	V
Switch Pin Voltage	V_{SW}	−0.3	18	V
Enable Pin Voltage	EN	0	18	V
Comp Pin Voltage	COMP	−0.1	5.5	V
Feedback Pin Voltage	FB	−0.1	5.5	V
Power Ground Pin Voltage	PGND	−0.1	−0.1	V
Junction Temperature Range	T_J	−40	125	°C
Operating Temperature Range	T_A	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS

(T_A = 25°C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V for min/max values unless otherwise noted (Note 7))

Characteristic		Conditions	Min	Typ	Max	Unit
Input Voltage Range		(Note 5)	4.5	–	18	V
SUPPLY CURRENT						
Quiescent Supply Current	NCP3170A NCP3170B	V_{IN} = EN = 12 V V_{FB} = 0.8 V (Note 5)	– –	1.7 1.7	2.0 2.0	mA
Shutdown Supply Current		EN = 0 V (Note 5)	–	13	17	μA
UNDER VOLTAGE LOCKOUT						
VIN UVLO Threshold		V_{IN} Rising Edge (Note 5)	–	4.41	–	V
VIN UVLO Threshold		V_{IN} Falling Edge (Note 5)	–	4.13	–	V
MODULATOR						
Oscillator Frequency	NCP3170A NCP3170B	Enable = V_{IN}	450 900	500 1000	550 1100	kHz
Maximum Duty Ratio	NCP3170A NCP3170B		91 90	– –	96 96	%
Minimum Duty Ratio	NCP3170A NCP3170B	V_{IN} = 12 V	6.0 4.0	– –	11 11.5	%
VIN Soft Start Ramp Time		V_{FB} = VCOMP	3.5	4.6	6.0	ms
OVER CURRENT						
Current Limit		(Note 4)	4.0	–	6.0	A
PWM COMPENSATION						
VFB Feedback Voltage		T_A = 25°C	0.792	0.8	0.808	V
Line Regulation		(Note 4)	–	1	–	%
GM			–	201	–	μS
AOL DC gain		(Note 4)	40	55	–	dB
Unity Gain BW (C_{OUT} = 10 pF)		(Note 4)	2.0	–	–	MHz
Input Bias Current (Current Out of FB IB Pin)		(Note 4)	–	–	286	nA
IEAOP Output Source Current		V_{FB} = 0 V	–	20.1	–	μA
IEAOM Output Sink Current		V_{FB} = 2 V	–	21.3	–	μA
ENABLE						
Enable Threshold		(Note 5)	–	1.41	–	V
POWER GOOD						
Power Good High On Threshold			–	875	–	mV
Power Good High Off Threshold			–	859	–	mV
Power Good Low On Threshold			–	712	–	mV
Power Good Low Off Threshold			–	728	–	mV
Over Voltage Protection Threshold			–	998	–	mV
Power Good Low Voltage		V_{IN} = 12 V, IPG = 500 μA	–	0.195	–	V
PWM OUTPUT STAGE						
High-Side Switch On-Resistance		V_{IN} = 12 V V_{IN} = 4.5 V	– –	90 100	130 150	mΩ
Low-Side Switch On-Resistance		V_{IN} = 12 V V_{IN} = 4.5 V	– –	25 29	35 39	mΩ
THERMAL SHUTDOWN						
Thermal Shutdown		(Notes 4 and 6)	–	164	–	°C
Hysteresis			–	43	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Guaranteed by design
5. Ambient temperature range of −40°C to +85°C.
6. This is not a protection feature.
7. The device is not guaranteed to operate beyond the maximum operating ratings.

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit from Figure 1, T_A = 25°C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V unless otherwise specified)

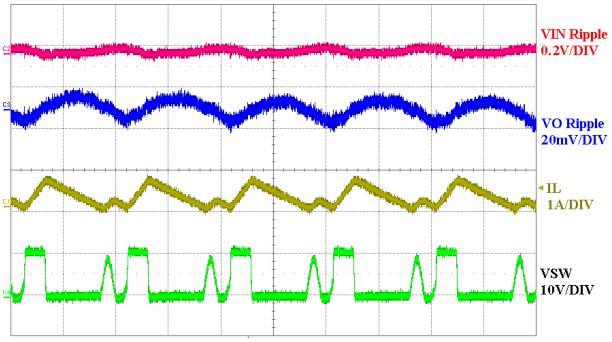


Figure 3. Light Load (DCM) Operation 1 μs/DIV

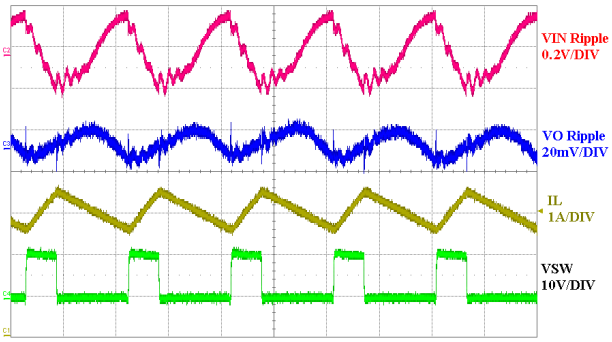


Figure 4. Full Load (CCM) Operation 1 μs/DIV

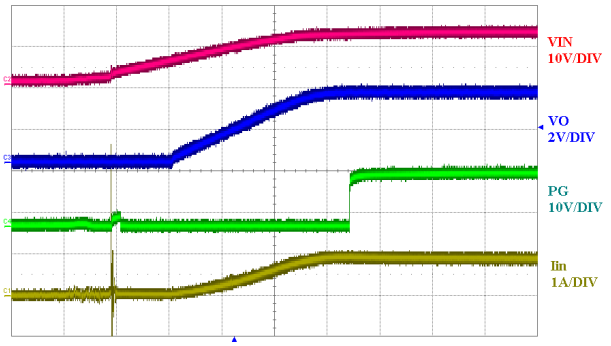


Figure 5. Start−Up into Full Load 1 ms/DIV

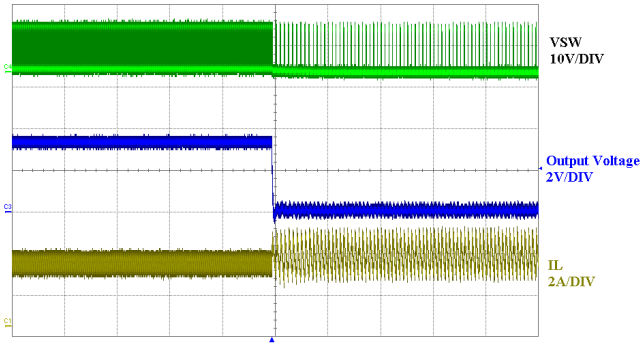


Figure 6. Short−Circuit Protection 200 μs /DIV

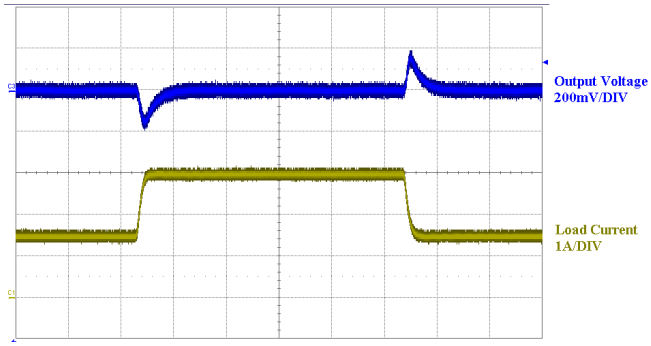


Figure 7. 50% to 100% Load Transient 100 μs/DIV

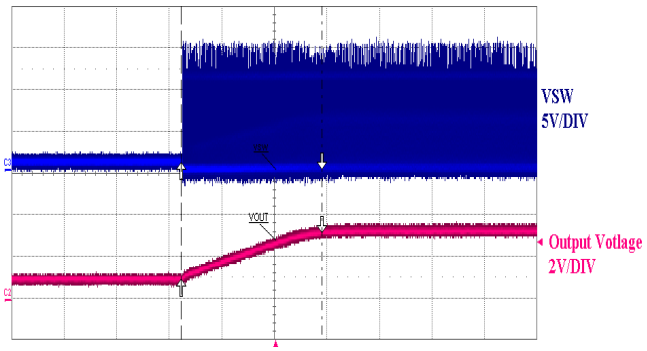


Figure 8. 3.3 V Turn on into 1 V Pre−Bias 1 ms /DIV

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit from Figure 1, T_A = 25°C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V unless otherwise specified)

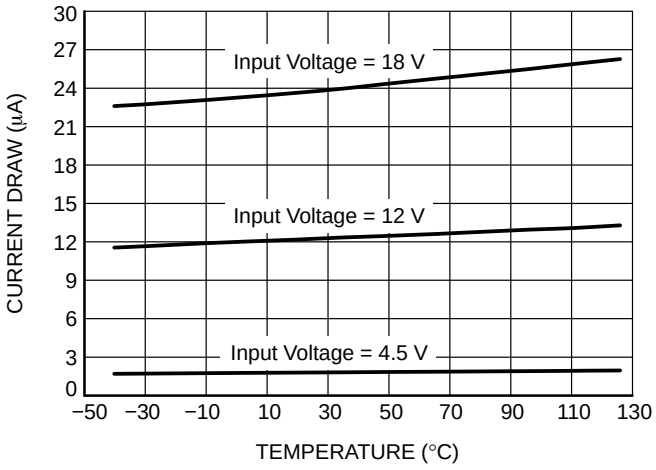


Figure 9. ICC Shut Down Current vs. Temperature

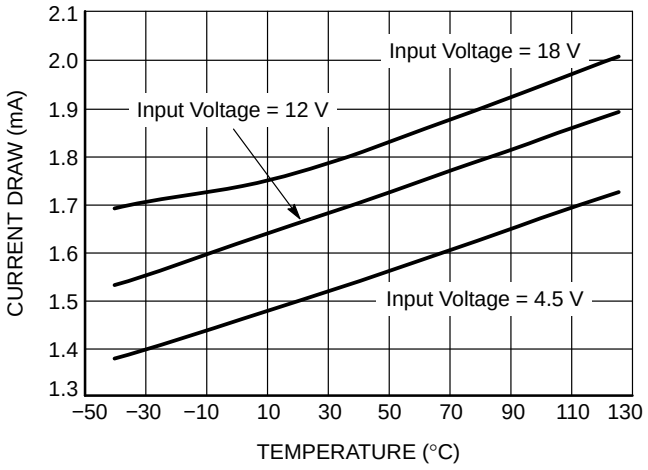


Figure 10. NCP3170 Enabled Current vs. Temperature

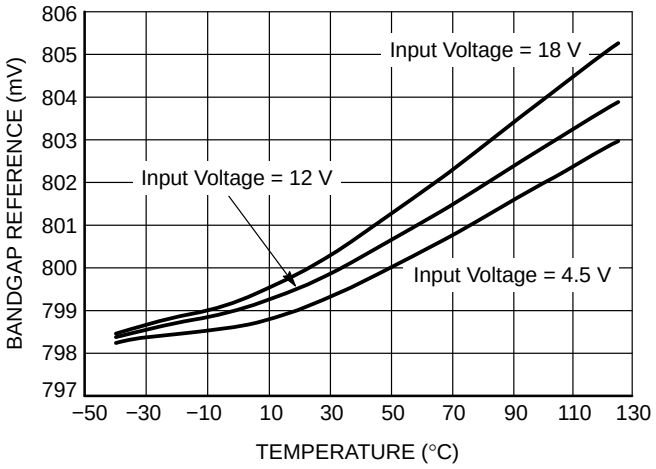


Figure 11. Bandgap Reference Voltage vs. Temperature

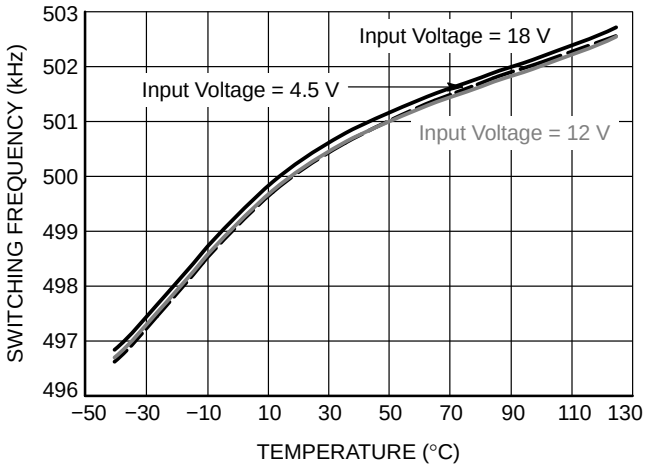


Figure 12. Switching Frequency vs. Temperature

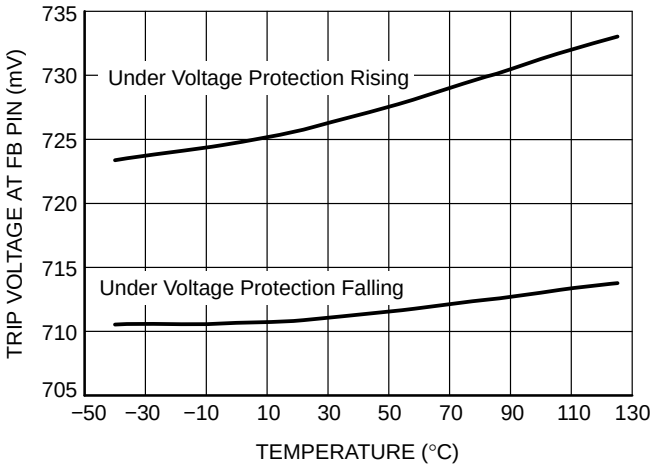


Figure 13. Input Under Voltage Protection at 12 V vs. Temperature

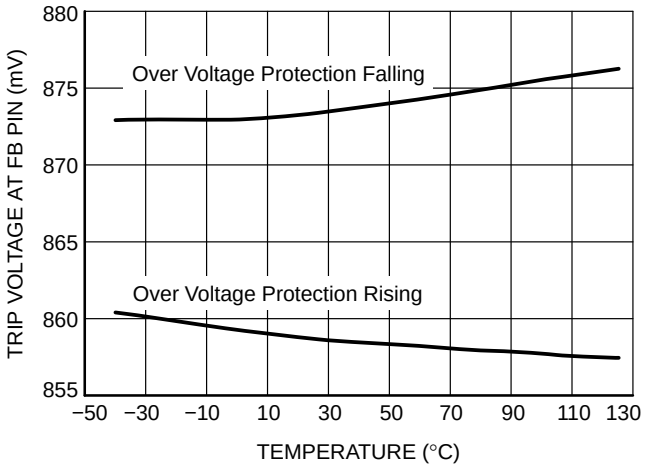


Figure 14. Input Over Voltage Protection at 12 V vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

(Circuit from Figure 1, T_A = 25°C, V_{IN} = V_{EN} = 12 V, V_{OUT} = 3.3 V unless otherwise specified)

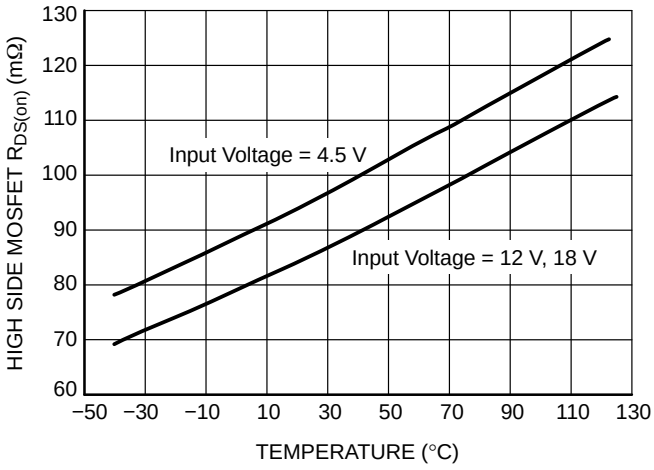


Figure 15. High Side MOSFET $R_{DS(on)}$ vs. Temperature

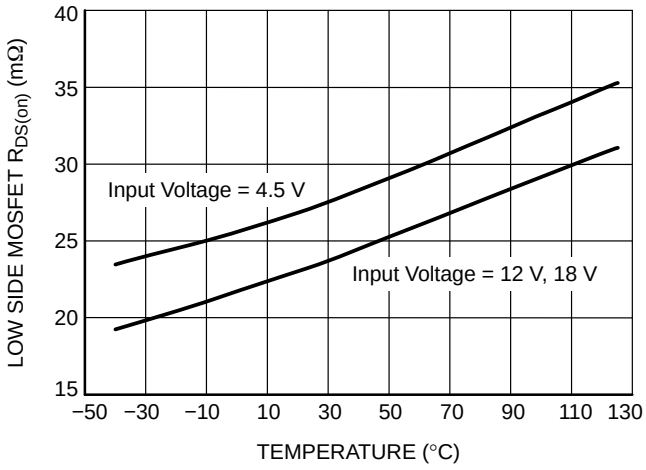


Figure 16. Low Side MOSFET $R_{DS(on)}$ vs. Temperature

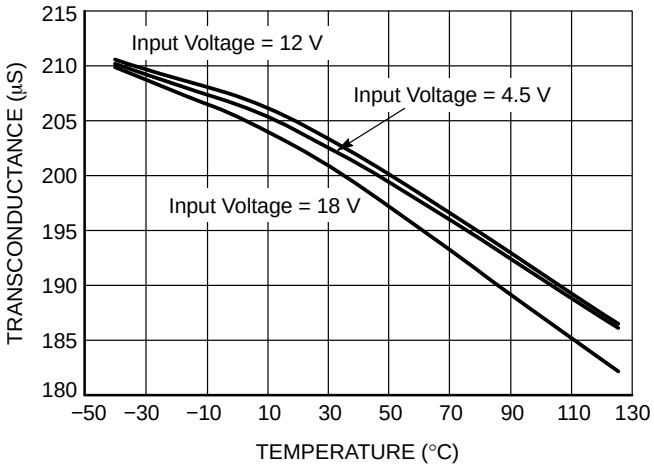


Figure 17. Transconductance vs. Temperature

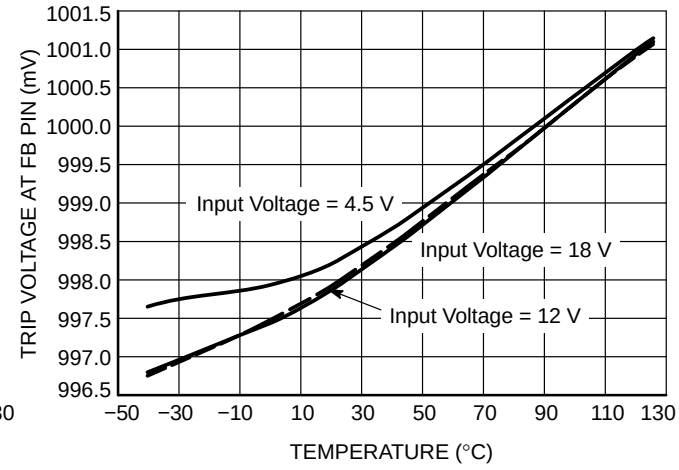


Figure 18. Over Voltage Protection vs. Temperature

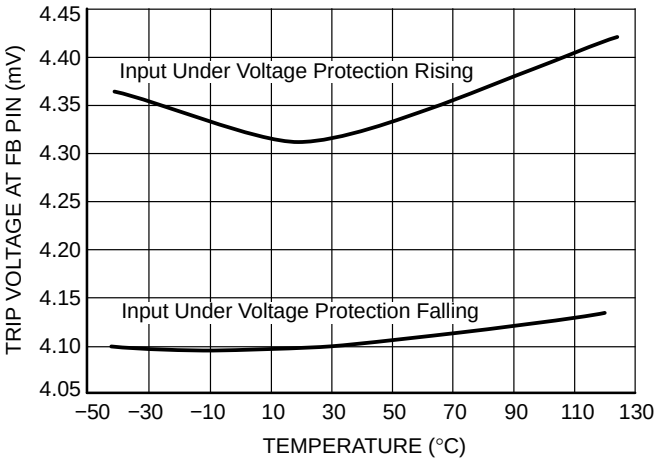


Figure 19. Input Under Voltage Protection vs. Temperature

NCP3170A Efficiency and Thermal Derating

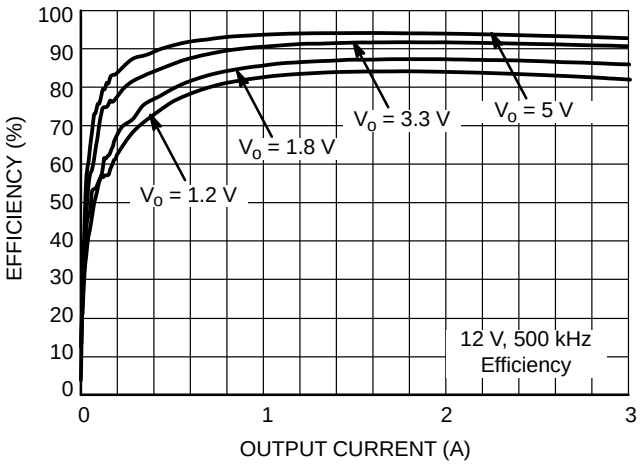


Figure 20. Efficiency (V_{IN} = 12 V) vs. Load Current

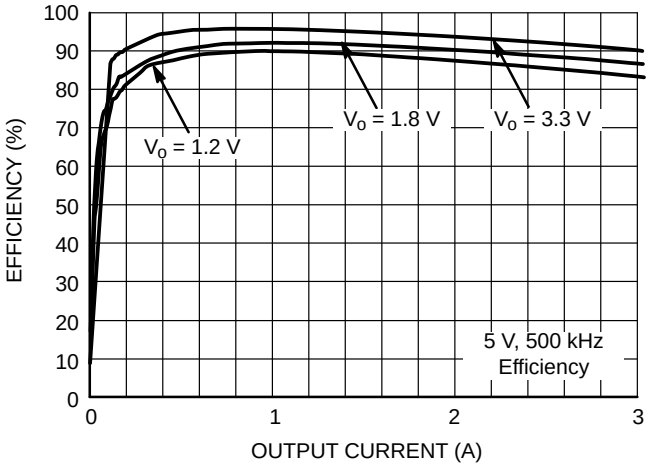


Figure 21. Efficiency (V_{IN} = 5 V) vs. Load Current

Thermal derating curves for the SOIC−8 package part under typical input and output conditions based on the evaluation board. The ambient temperature is 25°C with natural convection (air speed < 50 LFM) unless otherwise specified.

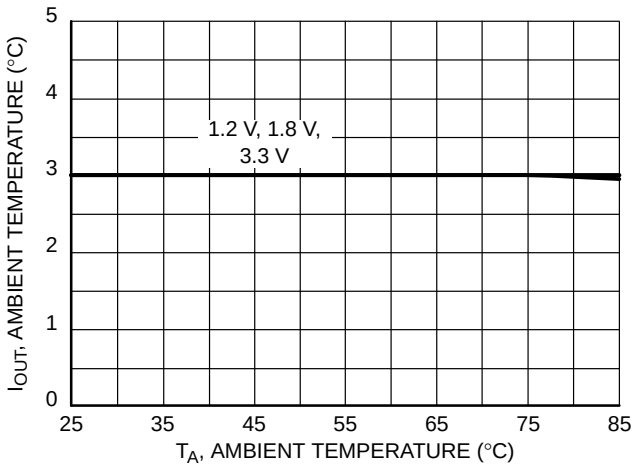


Figure 22. 500 kHz Derating Curves at 5 V

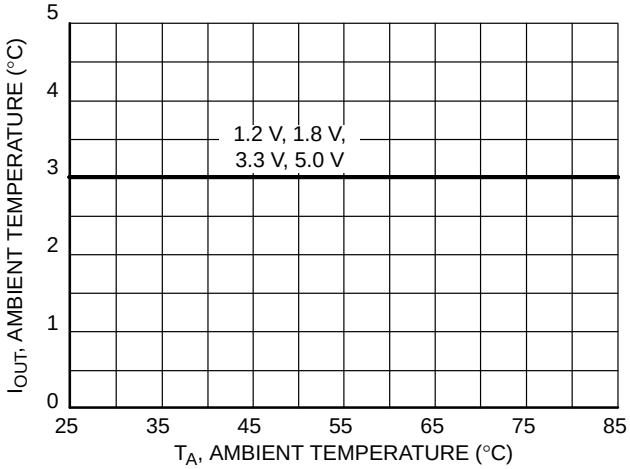


Figure 23. 500 kHz Derating Curves at 12 V

NCP3170B Efficiency and Thermal Derating

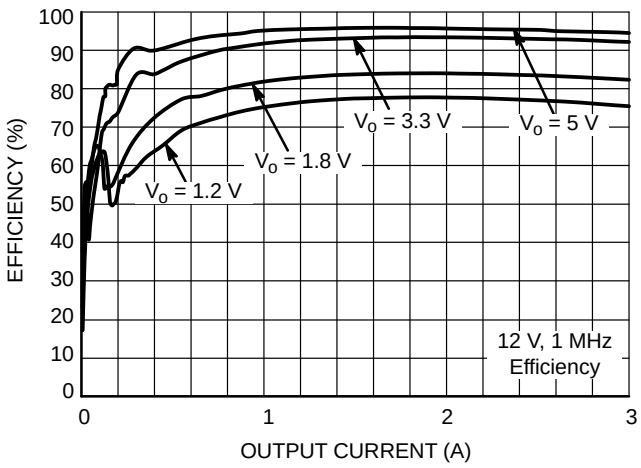


Figure 24. 12 V, 1 MHz Efficiency

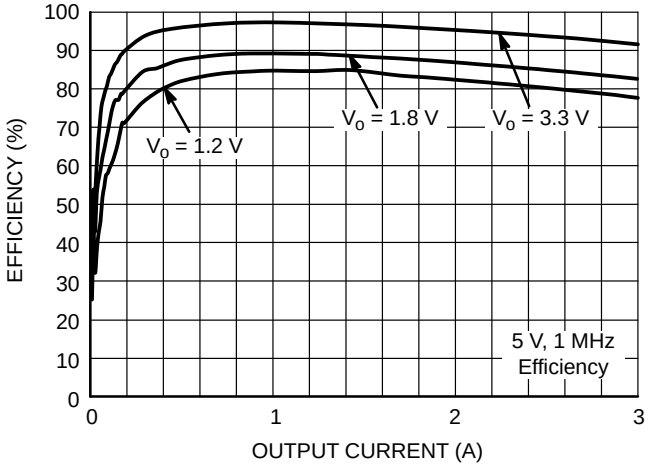


Figure 25. 5 V, 1 MHz Efficiency

Thermal derating curves for the SOIC−8 package part under typical input and output conditions based on the evaluation board. The ambient temperature is 25°C with natural convection (air speed < 50 LFM) unless otherwise specified.

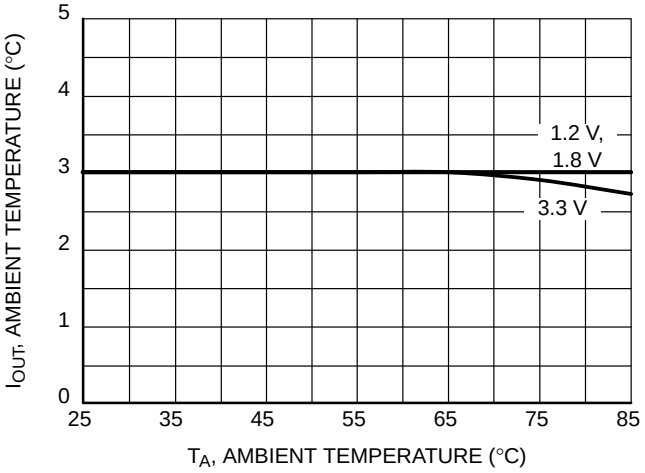


Figure 26. 1 MHz Derating Curves at 5 V Input

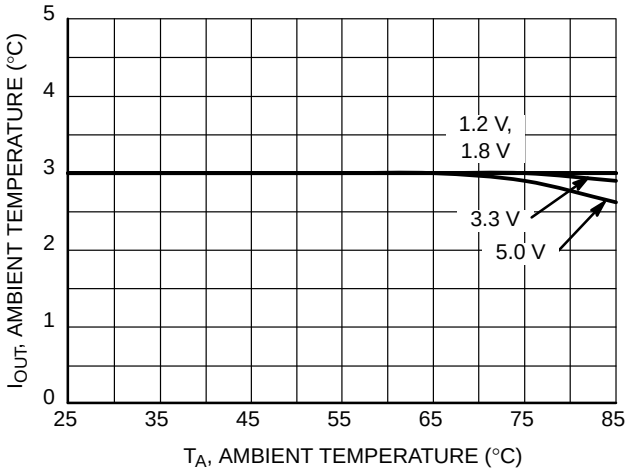


Figure 27. 1 MHz Derating Curves at 12 V Input

DETAILED DESCRIPTION

The NCP3170 is a current-mode, step down regulator with an integrated high-side PMOS switch and a low-side NMOS switch. It operates from a 4.5 V to 18 V input voltage range and supplies up to 3 A of load current. The duty ratio can be adjusted from 8% to 92% allowing a wide output voltage range. Features include enable control, Power-On Reset (POR), input under voltage lockout, fixed internal soft start, power good indication, over voltage protection, and thermal shutdown.

Enable and Soft-Start

An internal input voltage comparator not shown in Figure 28 will force the part to disable below the minimum input voltage of 4.13 V. The input under voltage disable feature is used to prevent improper operation of the converter due to insufficient voltages. The converter can be turned on by tying the enable pin high and the part will default to be input voltage enabled. The enable pin should never be left floating.

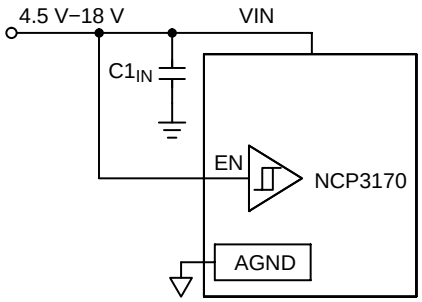


Figure 28. Input Voltage Enable

If an adjustable Under Voltage Lockout (UVLO) threshold is required, the EN pin can be used. The trip voltage of the EN pin comparator is 1.38 V typical. Upon application of an input voltage greater than 4.41 V, the VIN UVLO will release and the enable will be checked to determine if switching can commence. Once the 1.38 V trip voltage is crossed, the part will enable and the soft start sequence will initiate. If large resistor values are used, the EN pin should be bypassed with a 1 nF capacitor to prevent coupling problems from the switch node.

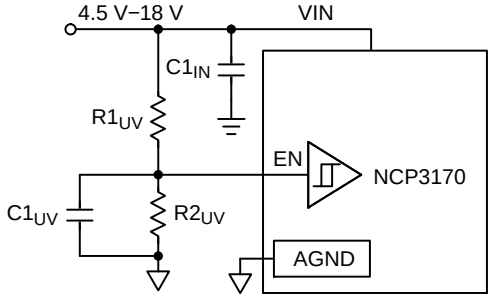


Figure 29. Input Under Voltage Lockout Enable

The enable pin can be used to delay a turn on by connecting a capacitor as shown in Figure 30.

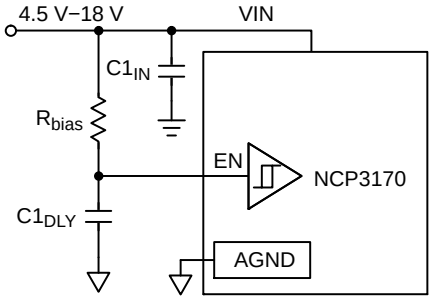


Figure 30. Delay Enable

If the designer would like to add hysteresis to the enable threshold it can be added by use of a bias resistor to the output. The hysteresis is created once soft start has initiated. With the output voltage rising, current flows into the enable node, raising the voltage. The thresholds for enable as well as hysteresis can be calculated using Equation 1.

$$VIN_{HYS} = VIN_{Start} - EN_{TH} + R1_{UV} \times \times \left[\frac{V_{OUT} - EN_{TH}}{R3_{UV}} - \frac{EN_{TH}}{R2_{UV}}\right] \quad \text{(eq. 1)}$$

$$VIN_{Start} = EN_{TH} \times \left[1 + \frac{R1_{UV} \times (R2_{UV} + R3_{UV})}{R2_{UV} \times R3_{UV}}\right] \quad \text{(eq. 2)}$$

where:

EN_{TH}	= Enable Threshold
VIN_{START}	= Input Voltage Start Threshold
$R1_{UV}$	= High Side Resistor
$R2_{UV}$	= Low Side Resistor
$R3_{UV}$	= Hysteresis Bias Resistor
V_{OUT}	= Regulated Output Voltage

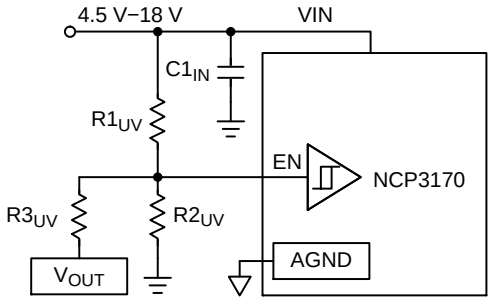


Figure 31. Added Hysteresis to the Enable UVLO

The part can be enabled with standard TTL or high voltage logic by using the configuration below.

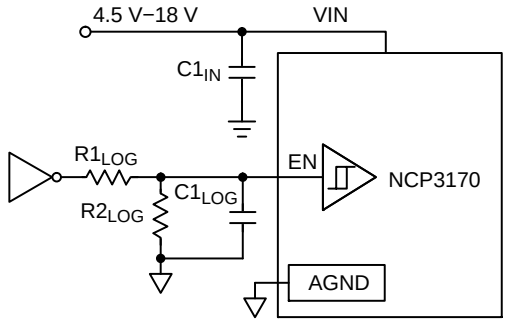


Figure 32. Logic Turn-on

The enable can also be used for power sequencing in conjunction with the Power Good (PG) pin as shown in Figure 33. The enable pin can either be tied to the output voltage of the master voltage or tied to the input voltage with a resistor to the PG pin of the master regulator.

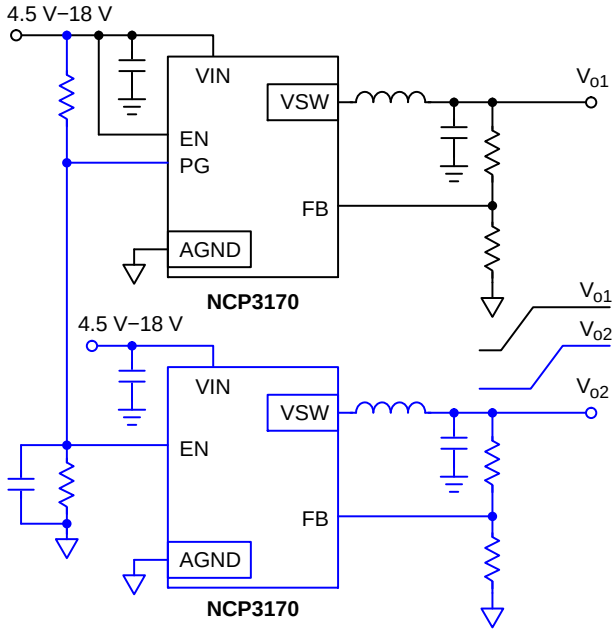


Figure 33. Enable Two Converter Power Sequencing

Once the part is enabled, the internal reference voltage is slewed from ground to the set point of 800 mV. The slewing process occurs over a 4.5 ms period, reducing the current draw from the upstream power source, reducing stress on internal MOSFETS, and ensuring the output inductor does not saturate during start-up.

Pre-Bias Start-up

When starting into a pre-bias load, the NCP3170 will not discharge the output capacitors. The soft start begins with the internal reference at ground. Both the high side switch and low side switches are turned off. The internal reference slowly raises and the OTA regulates the output voltage to the divided reference voltage. In a pre-biased condition, the voltage at the FB pin is higher than the internal reference voltage, so the OTA will keep the COMP voltage at ground potential. As the internal reference is slewed up, the COMP pin is held low until the FB pin voltage surpasses the internal reference voltage, at which time the COMP pin is allowed to respond to the OTA error signal. Since the bottom of the PWM ramp is at 0.6 V there will be a slight delay between the time the internal reference voltage passes the FB voltage and when the part starts to switch. Once the COMP error signal intersects with the bottom of the ramp, the high side switch is turned on followed by the low side switch. After the internal reference voltage has surpassed the FB voltage, soft start proceeds normally without output voltage discharge.

Power Good

The output voltage of the buck converter is monitored at the feedback pin of the output power stage. Two comparators are placed on the feedback node of the OTA to monitor the operating window of the feedback voltage as shown in Figure 34. All comparator outputs are ignored during the soft start sequence as soft start is regulated by the OTA since false trips would be generated. Further, the PG pin is held low until the comparators are evaluated. PG state does not affect the switching of the converter. After the soft start period has ended, if the feedback is below the reference voltage of comparator 1 ($V_{FB} < 0.726$), the output is considered operational undervoltage (OUV). The device will indicate the under voltage situation by the PG pin remaining low with a 100 kΩ pull-up resistance. When the feedback pin voltage rises between the reference voltages of comparator 1 and comparator 2 ($0.726 < V_{FB} < 0.862$), then the output voltage is considered power good and the PG pin is released. Finally, if the feedback voltage is greater than comparator 2 ($V_{FB} > 0.862$), the output voltage is considered operational overvoltage (OOV). The OOV will be indicated by the PG pin remaining low. A block diagram of the OOV and OUV functionality as well as a graphical representation of the PG pin functionality is shown in Figures 34 through 36.

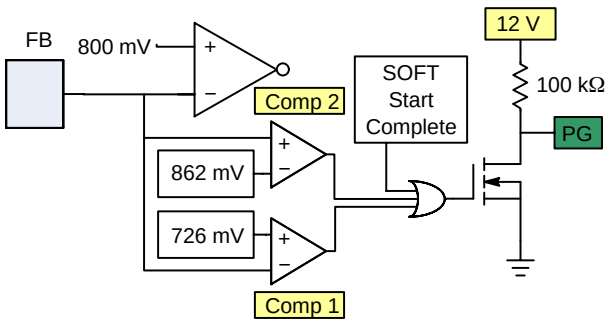


Figure 34. OOV and OUV System

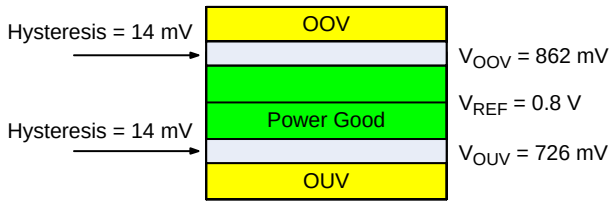


Figure 35. OOV and OUV Window

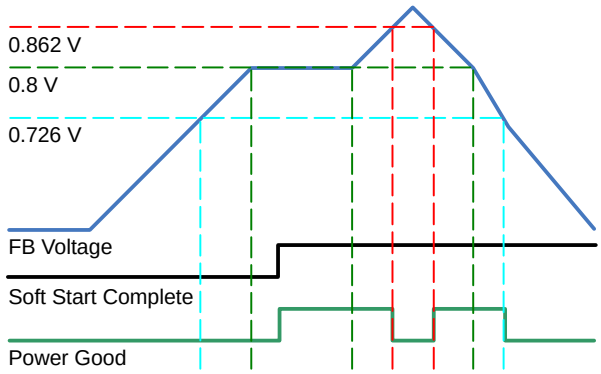


Figure 36. OOV and OUV Diagram

If the power good function is not used, it can be connected to the VSW node to reduce thermal resistance. Do not connect PG to the VSW node if the application is turning on into pre-bias.

Switching Frequency

The NCP3170 switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 450 kHz to 550 kHz for the NCP3170A and 900 kHz to 1.1 MHz for the NCP3170B due to device variation.

Light Load Operation

Light load operation is generally a load that is 1 mA to 300 mA where a load is in standby mode and requires very little power. During light load operation, the regulator emulates the operation of a non-synchronous buck converter and the regulator is allowed to skip pulses. The non-synchronous buck emulation is accomplished by detecting the point at which the current flowing in the inductor goes to zero and turning the low side switch off. At the point when the current goes to zero, if the low side switch is not turned off, current would reverse, discharging the output capacitor. Since the low side switch is shutoff, the only conduction path is through the body diode of the low side MOSFET, which is back biased. Unlike traditional synchronous buck converters, the current in the inductor will become discontinuous. As a result, the switch node will oscillate with the parasitic inductances and capacitances connected to the switch node. The OTA will continue to regulate the output voltage, but will skip pulses based on the output load shown in Figure 37.

The quiescent supply current of the NCP3170 varies from 1.7 mA typically to 2 mA maximum. The variation in inductance, capacitance, and resistance, and supply current typically results in a light load efficiencies variation of 3%.

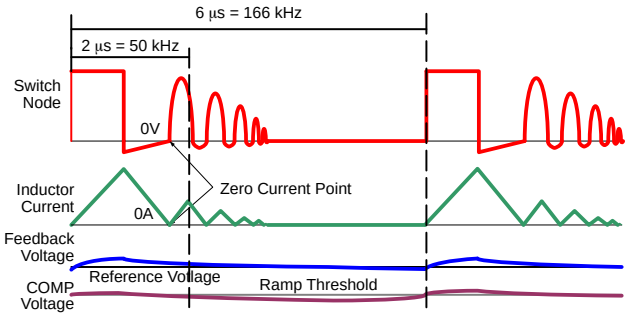


Figure 37. Light Load Operation

PROTECTION FEATURES

Over Current Protection

Current is limited to the load on a pulse by pulse basis. During each high side on period, the current is compared against an internally set limit. If the current limit is exceeded, the high side and low side MOSFETS are shutoff and no pulses are issued for 13.5 μs. During that time, the output voltage will decay and the inductor current will discharge. After the discharge period, the converter will initiate a soft start. If the load is not released, the current will build in the inductor until the current limit is exceeded, at which time the high side and low side MOSFETS will be shut off and the process will continue. If the load has been released, a normal soft start will commence and the part will continue switching normally until the current limit is exceeded.

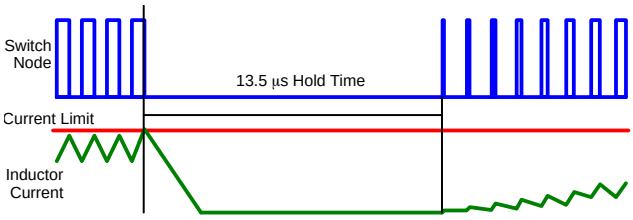


Figure 38. Over Current Protection

The current limit has a positives voltage influence where the peak current trip level increases 0.2%/V from the 5 V trip level.

Thermal Shutdown

The thermal limit, while not a protection feature, engages at 150°C in case of thermal runaway. When the thermal comparator is tripped at a die temperature of 150°C, the part must cool to 120°C before a restart is allowed. When thermal trip is engaged, switching ceases and high side and low side MOSFETs are driven off. Further, the power good indicator will pull low until the thermal trip has been released. Once the die temperature reaches 120°C the part will reinitiate soft-start and begin normal operation.

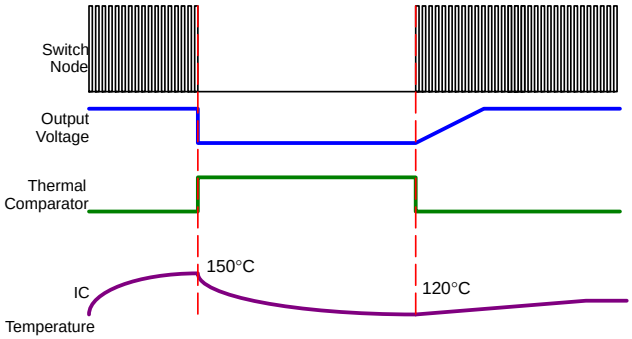


Figure 39. Over Temperature Shutdown

Over Voltage Protection

Upon the completion of soft start, the output voltage of the buck converter is monitored at the FB pin of the output power stage. One comparator is placed on the feedback node to provide over voltage protection. In the event an over voltage is detected, the high side switch turns off and the low side switch turns on until the feedback voltage falls below the OOV threshold. Once the voltage has fallen below the OOV threshold, switching continues normally as displayed in Figure 40.

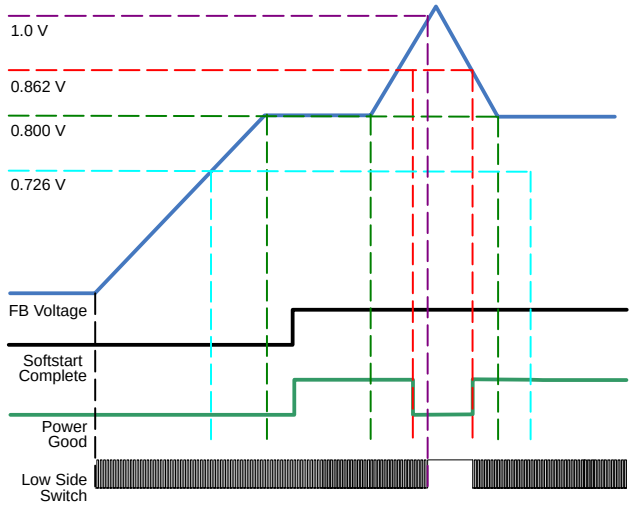


Figure 40. Over Voltage Low Side Switch Behavior

Duty Ratio

The duty ratio can be adjusted from 8% to 92% allowing a wide output voltage range. The low 8% duty ratio limit will restrict the PWM operation. For example if the application is converting to 1.2 V the converter will perform normally if the input voltage is below 15.5 V. If the input voltage exceeds 15.5 V while supplying 1.2 V output voltage the converter can skip pulses during operation. The skipping pulse operation will result in higher ripple voltage than when operating in PWM mode. Figure 41 and 42 below shows the safe operating area for the NCP3170A and B respectively. While not shown in the safe operating area graph, the output voltage is capable of increasing to the 93% duty ratio limitation providing a high output voltage such as 16 V. If the application requires a high duty ratio such as converting from 14 V to 10 V the converter will operate normally until the maximum duty ratio is reached. For example, if the input voltage were 16 V and the user wanted to produce the highest possible output voltage at full load, a good rule of thumb is to use 80% duty ratio. The discrepancy between the usable duty ratio and the actual duty ratio is due to the voltage drops in the system, thus leading to a maximum output voltage of 12.8 V rather than 14.8 V. The actual achievable output to input voltage ratio is dependent on layout, component selection, and acceptable output voltage tolerance.

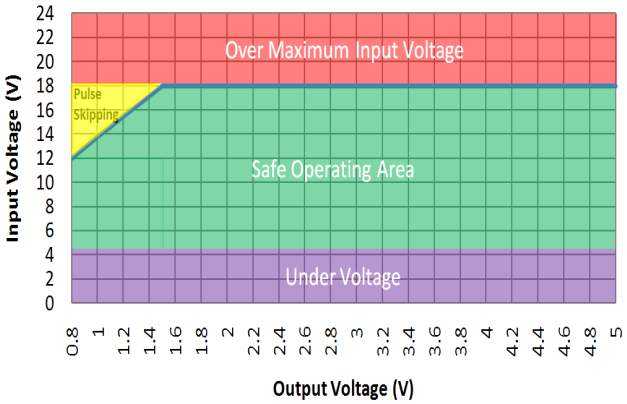


Figure 41. NCP3170A Safe Operating Area

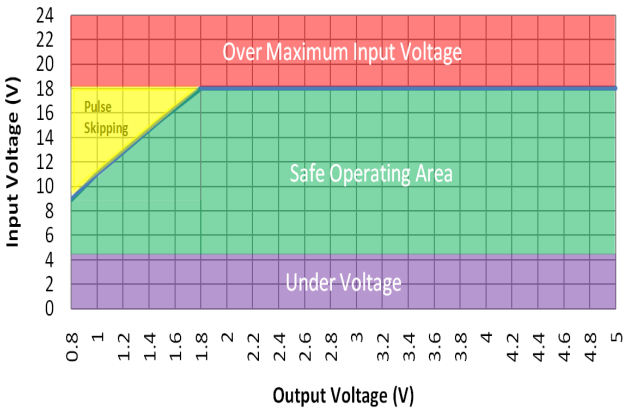


Figure 42. NCP3170B Safe Operating Area

Design Procedure

When starting the design of a buck regulator, it is important to collect as much information as possible about the behavior of the input and output before starting the design.

ON Semiconductor has a Microsoft Excel® based design tool available online under the design tools section of the NCP3170 product page. The tool allows you to capture your design point and optimize the performance of your regulator based on your design criteria.

Table 5. DESIGN PARAMETERS

Design Parameter	Example Value
Input Voltage (V_{IN})	9 V to 16 V
Output Voltage (V_{OUT})	3.3 V
Input Ripple Voltage (VCC_{RIPPLE})	200 mV
Output Ripple Voltage ($V_{OUTRIPPLE}$)	20 mV
Output Current Rating (I_{OUT})	3 A
Operating Frequency (F_{SW})	500 kHz

The buck converter produces input voltage (V_{IN}) pulses that are LC filtered to produce a lower DC output voltage (V_{OUT}). The output voltage can be changed by modifying the on time relative to the switching period (T) or switching frequency. The ratio of high side switch on time to the switching period is called duty ratio (D). Duty ratio can also be calculated using V_{OUT}, V_{IN}, the Low Side Switch Voltage Drop (V_{LSD}), and the High Side Switch Voltage Drop (V_{HSD}).

$$F_{SW} = \frac{1}{T} \quad \text{(eq. 3)}$$

$$D = \frac{T_{ON}}{T}(1 - D) = \frac{T_{OFF}}{T} \quad \text{(eq. 4)}$$

$$D = \frac{V_{OUT} + V_{LSD}}{V_{IN} - V_{HSD} + V_{LSD}} \approx \quad \text{(eq. 5)}$$

$$D = \frac{V_{OUT}}{V_{IN}} \rightarrow 27.5\% = \frac{3.3\ V}{12\ V}$$

where:

D	= Duty ratio
FSW	= Switching frequency
T	= Switching period
TOFF	= High side switch off time
TON	= High side switch on time
V_{IN}	= Input voltage
VHSD	= High side switch voltage drop
VLSD	= Low side switch voltage drop
VOUT	= Output voltage

Inductor Selection

When selecting an inductor, the designer may employ a rule of thumb for the design where the percentage of ripple current in the inductor should be between 10% and 40%. When using ceramic output capacitors, the ripple current can be greater because the ESR of the output capacitor is smaller, thus a user might select a higher ripple current. However, when using electrolytic capacitors, a lower ripple current will result in lower output ripple due to the higher ESR of electrolytic capacitors. The ratio of ripple current to maximum output current is given in Equation 6.

$$ra = \frac{\Delta I}{I_{OUT}} \quad \text{(eq. 6)}$$

where:

ΔI	= Ripple current
I_{OUT}	= Output current
ra	= Ripple current ratio

Using the ripple current rule of thumb, the user can establish acceptable values of inductance for a design using Equation 6.

$$L_{OUT} = \frac{V_{OUT}}{I_{OUT} \times ra \times F_{SW}} \times (1 - D) \rightarrow \quad \text{(eq. 7)}$$

$$4.7\ \mu H = \frac{3.3\ V}{3.0\ A \times 34\% \times 500\ kHz} \times (1 - 27.5\%)$$

where:

D	= Duty ratio
F_{SW}	= Switching frequency
I_{OUT}	= Output current
L_{OUT}	= Output inductance
ra	= Ripple current ratio

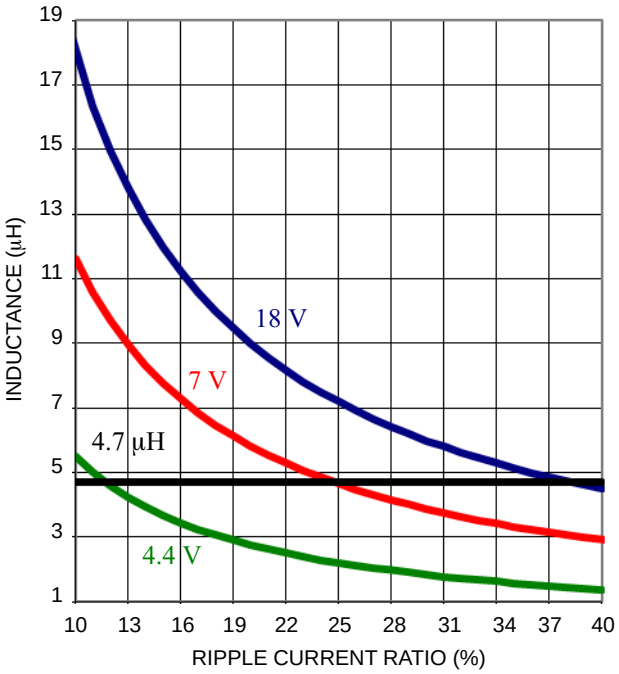


Figure 43. Inductance vs. Current Ripple Ratio

When selecting an inductor, the designer must not exceed the current rating of the part. To keep within the bounds of the part's maximum rating, a calculation of the RMS current and peak current are required.

$$I_{RMS} = I_{OUT} \times \sqrt{1 + \frac{ra^2}{12}} \rightarrow$$
$$3.01\ A = 3\ A \times \sqrt{1 + \frac{34\%^2}{12}} \rightarrow \quad \text{(eq. 8)}$$

where:

I_{OUT}	= Output current
I_{RMS}	= Inductor RMS current
ra	= Ripple current ratio

$$I_{PK} = I_{OUT} \times \left(1 + \frac{ra}{2}\right) \rightarrow$$
$$3.51\ A = 3\ A \times \left(1 + \frac{34\%}{2}\right) \quad \text{(eq. 9)}$$

where:

I_{OUT}	= Output current
I_{PK}	= Inductor peak current
ra	= Ripple current ratio

A standard inductor should be found so the inductor will be rounded to 4.7 μH. The inductor should support an RMS current of 3.01 A and a peak current of 3.51 A. A good design practice is to select an inductor that has a saturation current that exceeds the maximum current limit with some margin.

The final selection of an output inductor has both mechanical and electrical considerations. From a mechanical perspective, smaller inductor values generally correspond to smaller physical size. Since the inductor is often one of the largest components in the regulation system, a minimum inductor value is particularly important in space constrained applications. From an electrical perspective, the maximum current slew rate through the output inductor for a buck regulator is given by Equation 10.

$$SlewRate_{LOUT} = \frac{V_{IN} - V_{OUT}}{L_{OUT}} \rightarrow$$
$$1.85\ \frac{A}{\mu s} = \frac{12\ V - 3.3\ V}{4.7\ \mu H} \quad \text{(eq. 10)}$$

where:

L_{OUT}	= Output inductance
V_{IN}	= Input voltage
V_{OUT}	= Output voltage

Equation 10 implies that larger inductor values limit the regulator's ability to slew current through the output inductor in response to output load transients. Consequently, output capacitors must supply the load current until the inductor current reaches the output load current level. Reduced inductance to increase slew rates results in larger values of output capacitance to maintain tight output voltage regulation. In contrast, smaller values of inductance increase the regulator's maximum achievable slew rate and decrease the necessary capacitance at the expense of higher ripple current. The peak-to-peak ripple current for NCP3170 is given by the following equation:

$$I_{PP} = \frac{V_{OUT} \times (1 - D)}{L_{OUT} \times F_{SW}} \rightarrow$$
$$1.02\ A = \frac{3.3\ V \times (1 - 27.5\%)}{4.7\ \mu H \times 500\ kHz} \quad \text{(eq. 11)}$$

where:

D	= Duty ratio
F_{SW}	= Switching frequency
I_{PP}	= Peak-to-peak current of the inductor
L_{OUT}	= Output inductance
V_{OUT}	= Output voltage

From Equation 11, it is clear that the ripple current increases as L_{OUT} decreases, emphasizing the trade-off between dynamic response and ripple current.

The power dissipation of an inductor falls into two categories: copper and core losses. Copper losses can be further categorized into DC losses and AC losses. A good first order approximation of the inductor losses can be made using the DC resistance as shown below:

$$LP_{CU\_DC} = I_{RMS}^{\ 2} \times DCR \rightarrow$$
$$61\ mW = 3.01^2 \times 6.73\ m\Omega \quad \text{(eq. 12)}$$

where:

DCR	= Inductor DC resistance
I_{RMS}	= Inductor RMS current
LP_{CU_DC}	= Inductor DC power dissipation

The core losses and AC copper losses will depend on the geometry of the selected core, core material, and wire used. Most vendors will provide the appropriate information to make accurate calculations of the power dissipation at which point the total inductor losses can be captured by the equation below:

$$LP_{tot} = LP_{CU\_DC} + LP_{CU\_AC} + LP_{Core} \rightarrow$$
$$67\ mW = 61\ mW + 5\ mW + 1\ mW \quad \text{(eq. 13)}$$

where:

LP_{Core}	= Inductor core power dissipation
LP_{CU_AC}	= Inductor AC power dissipation
LP_{CU_DC}	= Inductor DC power dissipation
LP_{tot}	= Total inductor losses

Output Capacitor Selection

The important factors to consider when selecting an output capacitor are DC voltage rating, ripple current rating, output ripple voltage requirements, and transient response requirements.

The output capacitor must be able to operate properly for the life time of a product. When selecting a capacitor it is important to select a voltage rating that is de-rated to the guaranteed operating life time of a product. Further, it is important to note that when using ceramic capacitors, the capacitance decreases as the voltage applied increases; thus a ceramic capacitor rated at 100 μF 6.3 V may measure 100 μF at 0 V but measure 20 μF with an applied voltage of 3.3 V depending on the type of capacitor selected.

The output capacitor must be rated to handle the ripple current at full load with proper derating. The capacitor RMS ratings given in datasheets are generally for lower switching frequencies than used in switch mode power supplies, but a multiplier is given for higher frequency operation. The RMS current for the output capacitor can be calculated below:

$$CO_{RMS} = I_{OUT}\frac{ra}{\sqrt{12}} \rightarrow$$
$$0.294\ A = 3.0\ A\frac{34\%}{\sqrt{12}} \quad \text{(eq. 14)}$$

where:

Co_{RMS}	= Output capacitor RMS current
I_{OUT}	= Output current
ra	= Ripple current ratio

The maximum allowable output voltage ripple is a combination of the ripple current selected, the output capacitance selected, the Equivalent Series Inductance (ESL), and Equivalent Series Resistance (ESR).

The main component of the ripple voltage is usually due to the ESR of the output capacitor and the capacitance selected, which can be calculated as shown in Equation 14:

$$V_{ESR\_C} = I_{OUT} \times ra \times \left(CO_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \rightarrow \quad \text{(eq. 15)}$$
$$10.89\ mV = 3 \times 34\% \times \left(5\ m\Omega + \frac{1}{8 \times 500\ kHz \times 44\ \mu F}\right)$$

where:

Co_{ESR}	= Output capacitor ESR
C_{OUT}	= Output capacitance
F_{SW}	= Switching frequency
I_{OUT}	= Output current
ra	= Ripple current ratio
V_{ESR_C}	= Ripple voltage from the capacitor

The impedance of a capacitor is a function of the frequency of operation. When using ceramic capacitors, the ESR of the capacitor decreases until the resonant frequency is reached, at which point the ESR increases; therefore the ripple voltage might not be what one expected due to the switching frequency. Further, the method of layout can add resistance in series with the capacitance, increasing ripple voltage.

The ESL of capacitors depends on the technology chosen, but tends to range from 1 nH to 20 nH, where ceramic capacitors have the lowest inductance and electrolytic capacitors have the highest. The calculated contributing voltage ripple from ESL is shown for the switch on and switch off below:

$$V_{ESLON} = \frac{ESL \times I_{PP} \times F_{SW}}{D} \rightarrow$$
$$1.84\ mV = \frac{1\ nH \cdot 1.01\ A \cdot 500\ kHz}{27.5\%} \quad \text{(eq. 16)}$$

$$V_{ESLOFF} = \frac{ESL \times I_{PP} \times F_{SW}}{(1 - D)} \rightarrow$$
$$0.7\ mV = \frac{1\ nH \times 1.1\ A \times 500\ kHz}{(1 - 27.5\%)} \quad \text{(eq. 17)}$$

where:

D	= Duty ratio
ESL	= Capacitor inductance
F_{SW}	= Switching frequency
I_{PP}	= Peak-to-peak current

The output capacitor is a basic component for fast response of the power supply. For the first few microseconds of a load transient, the output capacitor supplies current to the load. Once the regulator recognizes a load transient, it adjusts the duty ratio, but the current slope is limited by the inductor value.

During a load step transient, the output voltage initially drops due to the current variation inside the capacitor and the ESR (neglecting the effect of the ESL).

$$\Delta V_{OUT-ESR} = I_{TRAN} \times CO_{ESR} \rightarrow$$
$$7.5\ mV = 1.5\ A \times 5\ m\Omega \quad \text{(eq. 18)}$$

where:

Co_{ESR}	= Output capacitor Equivalent Series Resistance
I_{TRAN}	= Output transient current
ΔV_{OUT_ESR}	= Voltage deviation of V_{OUT} due to the effects of ESR

A minimum capacitor value is required to sustain the current during the load transient without discharging it. The voltage drop due to output capacitor discharge is given by the following equation:

$$\Delta V_{OUT-DIS} = \frac{(I_{TRAN})^2 \times L_{OUT} \times F_{SW}}{2 \times F_{CROSS} \times C_{OUT} \times (V_{IN} - V_{OUT})} \rightarrow$$
$$138.1\ mV = \frac{(1.5)^2 \times 4.7\ \mu H \times 500\ kHz}{2 \times 50\ kHz \times 44\ \mu F \times (12\ V - 3.3\ V)} \quad \text{(eq. 19)}$$

where:

C_{OUT}	= Output capacitance
D	= Duty ratio
F_{SW}	= Switching frequency
F_{CROSS}	= Loop cross over frequency
I_{TRAN}	= Output transient current
L_{OUT}	= Output inductor value
V_{IN}	= Input voltage
V_{OUT}	= Output voltage
ΔV_{OUT_DIS}	= Voltage deviation of V_{OUT} due to the effects of capacitor discharge

In a typical converter design, the ESR of the output capacitor bank dominates the transient response. Please note that ΔV_{OUT_DIS} and ΔV_{OUT_ESR} are out of phase with each other, and the larger of these two voltages will determine the

maximum deviation of the output voltage (neglecting the effect of the ESL). It is important to note that the converters frequency response will change when the NCP3170 is operating in synchronous mode or non-synchronous mode due to the change in plant response from CCM to DCM. The effect will be a larger transient voltage excursion when transitioning from no load to full load quickly.

Input Capacitor Selection

The input capacitor has to sustain the ripple current produced during the on time of the upper MOSFET, so it must have a low ESR to minimize losses and input voltage ripple. The RMS value of the input ripple current is:

$$Iin_{RMS} = I_{OUT} \times \sqrt{D \times (1 - D)} \rightarrow$$
$$1.34\ A = 3\ A \times \sqrt{27.5\% \times (1 - 27.5\%)} \quad \text{(eq. 20)}$$

where:

D	= Duty ratio
Iin_{RMS}	= Input capacitance RMS current
I_{OUT}	= Load current

The equation reaches its maximum value with D = 0.5 at which point the input capacitance RMS current is half the output current. Loss in the input capacitors can be calculated with the following equation:

$$P_{CIN} = CIN_{ESR} \times \left(Iin_{RMS}\right)^2$$
$$18\ mW = 10\ m\Omega \times \left(1.34\ A\right)^2 \quad \text{(eq. 21)}$$

where:

CIN_{ESR}	= Input capacitance Equivalent Series Resistance
Iin_{RMS}	= Input capacitance RMS current
P_{CIN}	= Power loss in the input capacitor

Due to large di/dt through the input capacitors, electrolytic or ceramics should be used. If a tantalum capacitor must be used, it must be surge protected, otherwise capacitor failure could occur.

POWER MOSFET DISSIPATION

Power dissipation, package size, and the thermal environment drive power supply design. Once the dissipation is known, the thermal impedance can be calculated to prevent the specified maximum junction temperatures from being exceeded at the highest ambient temperature.

Power dissipation has two primary contributors: conduction losses and switching losses. The high-side MOSFET will display both switching and conduction losses. The switching losses of the low side MOSFET will not be calculated as it switches into nearly zero voltage and the losses are insignificant. However, the body diode in the low-side MOSFET will suffer diode losses during the non-overlap time of the gate drivers.

Starting with the high-side MOSFET, the power dissipation can be approximated from:

$$P_{D\_HS} = P_{COND} + P_{SW\_TOT} \quad \text{(eq. 22)}$$

where:

P_{COND}	= Conduction losses
P_{D_HS}	= Power losses in the high side MOSFET
P_{SW_TOT}	= Total switching losses

The first term in Equation 21 is the conduction loss of the high-side MOSFET while it is on.

$$P_{COND} = \left(I_{RMS\_HS}\right)^2 \times R_{DS(on)\_HS} \quad \text{(eq. 23)}$$

where:

I_{RMS_HS}	= RMS current in the high side MOSFET
$R_{DS(ON)\_HS}$	= On resistance of the high side MOSFET
P_{COND}	= Conduction power losses

Using the ra term from Equation 6, I_{RMS} becomes:

$$I_{RMS\_HS} = I_{OUT} \times \sqrt{D \times \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 24)}$$

where:

D	= Duty ratio
ra	= Ripple current ratio
I_{OUT}	= Output current
I_{RMS_HS}	= High side MOSFET RMS current

The second term from Equation 22 is the total switching loss and can be approximated from the following equations.

$$P_{SW\_TOT} = P_{SW} + P_{DS} + P_{RR} \quad \text{(eq. 25)}$$

where:

P_{DS}	= High side MOSFET drain to source losses
P_{RR}	= High side MOSFET reverse recovery losses
P_{SW}	= High side MOSFET switching losses
P_{SW_TOT}	= High side MOSFET total switching losses

The first term for total switching losses from Equation 25 are the losses associated with turning the high-side MOSFET on and off and the corresponding overlap in drain voltage and current.

$$P_{SW} = P_{TON} + P_{TOFF} =$$
$$= \frac{1}{2} \times \left(I_{OUT} \times V_{IN} \times F_{SW}\right) \times \left(t_{RISE} + t_{FALL}\right) \quad \text{(eq. 26)}$$

where:

F_{SW}	= Switching frequency
I_{OUT}	= Load current
P_{SW}	= High side MOSFET switching losses
P_{TON}	= Turn on power losses
P_{TOFF}	= Turn off power losses

t_{FALL} = MOSFET fall time
t_{RISE} = MOSFET rise time
V_{IN} = Input voltage

When calculating the rise time and fall time of the high side MOSFET, it is important to know the charge characteristic shown in Figure 44.

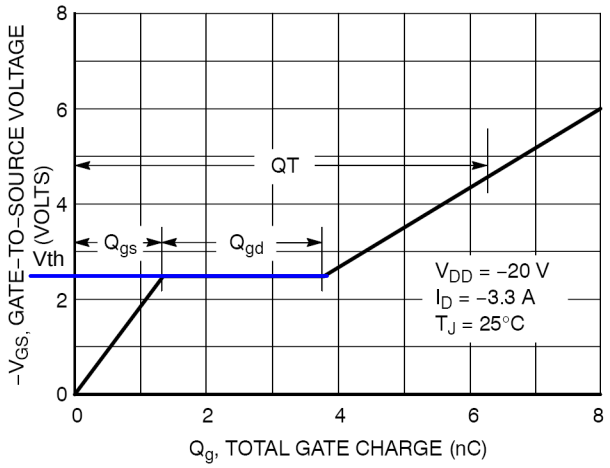


Figure 44. High Side MOSFET Total Charge

$$t_{RISE} = \frac{Q_{GD}}{I_{G1}} = \frac{Q_{GD}}{(V_{CL} - V_{TH})/(R_{HSPU} + R_G)} \quad \text{(eq. 27)}$$

where:
IG1 = Output current from the high-side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_{HSPU} = Drive pull up resistance
R_G = MOSFET gate resistance
t_{RISE} = MOSFET rise time
V_{CL} = Clamp voltage
V_{TH} = MOSFET gate threshold voltage

$$t_{FALL} = \frac{Q_{GD}}{I_{G2}} = \frac{Q_{GD}}{(V_{CL} - V_{TH})/(R_{HSPD} + R_G)} \quad \text{(eq. 28)}$$

where:
IG2 = Output current from the low-side gate drive
Q_{GD} = MOSFET gate to drain gate charge
R_G = MOSFET gate resistance
R_{HSPD} = Drive pull down resistance
t_{FALL} = MOSFET fall time
V_{CL} = Clamp voltage
V_{TH} = MOSFET gate threshold voltage

Next, the MOSFET output capacitance losses are caused by both the high-side and low-side MOSFETs, but are dissipated only in the high-side MOSFET.

$$P_{DS} = \frac{1}{2} \times C_{OSS} \times V_{IN}^{\ 2} \times F_{SW} \quad \text{(eq. 29)}$$

where:
C_{OSS} = MOSFET output capacitance at 0 V
F_{SW} = Switching frequency
P_{DS} = MOSFET drain to source charge losses
V_{IN} = Input voltage

Finally, the loss due to the reverse recovery time of the body diode in the low−side MOSFET is shown as follows:

$$P_{RR} = Q_{RR} \times V_{IN} \times F_{SW} \quad \text{(eq. 30)}$$

where:
F_{SW} = Switching frequency
P_{RR} = High side MOSFET reverse recovery losses
Q_{RR} = Reverse recovery charge
V_{IN} = Input voltage

The low-side MOSFET turns on into small negative voltages so switching losses are negligible. The low-side MOSFET's power dissipation only consists of conduction loss due to $R_{DS(on)}$ and body diode loss during non-overlap periods.

$$P_{D\_LS} = P_{COND} + P_{BODY} \quad \text{(eq. 31)}$$

where:
P_{BODY} = Low side MOSFET body diode losses
P_{COND} = Low side MOSFET conduction losses
P_{D_LS} = Low side MOSFET losses

Conduction loss in the low-side MOSFET is described as follows:

$$P_{COND} = \left(I_{RMS\_LS}\right)^2 \times R_{DS(on)\_LS} \quad \text{(eq. 32)}$$

where:
I_{RMS_LS} = RMS current in the low side
$R_{DS(ON)\_LS}$ = Low-side MOSFET on resistance
P_{COND} = High side MOSFET conduction losses

$$I_{RMS\_LS} = I_{OUT} \times \sqrt{(1 - D) \times \left(1 + \frac{ra^2}{12}\right)} \quad \text{(eq. 33)}$$

where:
D = Duty ratio
I_{OUT} = Load current
I_{RMS_LS} = RMS current in the low side
ra = Ripple current ratio

The body diode losses can be approximated as:

$$P_{BODY} = V_{FD} \times I_{OUT} \times F_{SW} \times \left(NOL_{LH} + NOL_{HL}\right) \quad \text{(eq. 34)}$$

where:

F_{SW} = Switching frequency
I_{OUT} = Load current
NOL_{HL} = Dead time between the high-side MOSFET turning off and the low-side MOSFET turning on, typically 30 ns
NOLLH = Dead time between the low-side MOSFET turning off and the high-side MOSFET turning on, typically 30 ns
P_{BODY} = Low-side MOSFET body diode losses
V_{FD} = Body diode forward voltage drop typically 0.92 V

Compensation Network

To create a stable power supply, the compensation network around the transconductance amplifier must be used in conjunction with the PWM generator and the power stage. Since the power stage design criteria is set by the application, the compensation network must correct the overall output to ensure stability. The NCP3170 is a current mode regulator and as such there exists a voltage loop and a current loop. The current loop causes the inductor to act like a current source which governs most of the characteristics of current mode control. The output inductor and capacitor of the power stage form a double pole but because the inductor is treated like a current source in closed loop, it becomes a single pole system. Since the feedback loop is controlling the inductor current, it is effectively like having a current source feeding a capacitor; therefore the pole is controlled by the load and the output capacitance. A table of compensation values for 500 kHz and 1 MHz is provided below for two 22 μF ceramic capacitors. The table also provides the resistor value for CompCalc at the defined operating point.

Table 6. COMPENSATION VALUES

	VIN (V)	V_{out} (V)	L_{out} (μF)	R1 (kΩ)	R2 (kΩ)	Rf (kΩ)	Cf (pF)	Cc (nF)	Rc (kΩ)	Cp (pF)	Resistance for Current Gain
NCP3170A	12	0.8	1.8	24.9	NI	NI	NI	NI	NI	15	3.6
	12	1.0	2.5	24.9	100	1	150	15	0.825	NI	4
	12	1.1	2.5	24.9	66.5	1	150	10	2	NI	20
	12	1.2	2.5	24.9	49.9	1	150	10	2	NI	20
	12	1.5	3.6	24.9	28.7	1	150	10	2.49	NI	20
	12	1.8	3.6	24.9	20	1	150	10	2.49	NI	20
	12	2.5	4.7	24.9	11.8	1	150	8.2	3.74	NI	25
	12	3.3	4.7	24.9	7.87	1	150	6.8	4.99	NI	27
	12	5.0	7.2	24.9	4.75	1	150	3.9	10	NI	27
	12	10.68	7.2	24.9	2.05	1	150	3.9	10	NI	30
	18	14.8	7.2	24.9	1.43	1	150	6.8	6.98	NI	30
	5	0.8	1.8	24.9	NI	NI	NI	NI	NI	15	15
	5	1.0	2.5	24.9	100	1	150	15	0.825	NI	28
	5	1.1	2.5	24.9	66.5	1	150	10	2	NI	30
	5	1.2	2.5	24.9	49.9	1	150	10	2	NI	30
	5	1.5	3.6	24.9	28.7	1	150	10	2.49	NI	30
	5	1.8	3.6	24.9	20	1	150	10	2.49	NI	30
	5	2.5	3.6	24.9	11.8	1	150	6.8	4.99	NI	50
	5	3.3	3.6	24.9	7.87	1	150	6.8	4.99	NI	50

Table 6. COMPENSATION VALUES (continued)

	VIN (V)	V_{out} (V)	L_{out} (μF)	R1 (kΩ)	R2 (kΩ)	Rf (kΩ)	Cf (pF)	Cc (nF)	Rc (kΩ)	Cp (pF)	Resistance for Current Gain
NCP3170B	12	1.2	1.5	24.9	49.9	1	82	2.7	6.04	NI	20
	12	1.5	1.8	24.9	28.7	1	82	2.7	6.04	NI	22
	12	1.8	1.8	24.9	20	1	82	2.7	6.04	NI	22
	12	2.5	2.7	24.9	11.8	1	82	1.8	10	NI	32
	12	3.3	3.3	24.9	7.87	1	82	1.5	12.1	NI	52
	12	5.0	3.3	24.9	4.75	1	82	2.2	8.25	NI	52
	12	10.68	1.5	24.9	2.05	1	82	2.2	5.1	NI	52
	18	14.8	3.3	24.9	1.43	1	82	2.2	5.1	NI	52
	5	0.8	1.0	24.9	NI	NI	NI	15	0.499	NI	20
	5	1.0	1.0	24.9	100	NI	NI	6.8	1.69	NI	28
	5	1.1	1.0	24.9	66.5	NI	NI	3.9	3.61	NI	42
	5	1.2	1.5	24.9	49.9	1	82	2.7	6.04	NI	55
	5	1.5	1.5	24.9	28.7	1	82	2.7	6.04	NI	55
	5	1.8	1.5	24.9	20	1	82	1.8	10	NI	55
	5	2.5	1.8	24.9	11.8	1	82	1.8	10	NI	55
	5	3.3	1.8	24.9	7.87	1	82	1.8	10	NI	55

To compensate the converter we must first calculate the current feedback

$$M = \frac{F_{SW} \times L_{OUT} \times V_{RAMP}}{R_{MAP} \times VIN} + 1 \rightarrow \quad \text{(eq. 35)}$$

$$6.299 = \frac{500\ kHz \times 4.7\ \mu H \times 0.33\ V}{\frac{\left(32 \times \frac{3.3\ V}{12\ V} + 1.46\right)}{1000}\ \Omega \times 12\ V} + 1$$

where:

F_{SW} = Switching Frequency
L_{OUT} = Output inductor value
M = Current feedback
Vin = Input Voltage
V_{OUT} = Output Voltage
V_{RAMP} = Slope Compensation Ramp
R_{MAP} = Current Sense Resistance

The un-scaled gain of the converter also needs to be calculated as follows:

$$A = \frac{1}{\frac{I_{OUT}}{V_{OUT}} + \frac{M - 0.5 - M \times \frac{V_{OUT}}{V_{IN}}}{L_{OUT} \times FSW}} \quad \text{(eq. 36)}$$

$$0.379\ \Omega = \frac{1}{\frac{3.0\ A}{3.3\ V} + \frac{6.299 - 0.5 - 6.299 \times \frac{3.3\ V}{12\ V}}{4.7\ \mu H \times 500\ kHz}}$$

where:

A = Un-scaled gain
F_{SW} = Switching Frequency
I_{OUT} = Output Current
L_{OUT} = Output inductor value
M = Current feedback
V_{IN} = Input Voltage
V_{OUT} = Output Voltage

Next the DC gain of the plant must be calculated.

$$G = \frac{A}{R_{MAP}} \rightarrow \quad \text{(eq. 37)}$$

$$36.925 = \frac{0.379\ \Omega}{\frac{\left(32 \times \frac{3.3\ V}{12\ V} + 1.46\right)}{1000}\ \Omega}$$

where:

G = DC gain of the plant
A = Un−scaled gain

The amplitude ratio can be calculated using the following equation:

$$Y = \frac{VREF}{V_{OUT}} \rightarrow 0.242 = \frac{0.8\ V}{3.3\ V} \quad \text{(eq. 38)}$$

where:

Vo = Output voltage
VREF = Regulator reference voltage
Y = Amplitude ratio

The ESR of the output capacitor creates a “zero” at the frequency as shown in Equation 39:

$$FZ_{ESR} = \frac{1}{2\pi \times CO_{ESR} \times C_{OUT}} \rightarrow$$

$$723\ kHz = \frac{1}{2\pi \times 5\ m\Omega \times 44\ \mu F} \quad \text{(eq. 39)}$$

where:

CO_{ESR} = Output capacitor ESR
C_{OUT} = Output capacitor
FZ_{ESR} = Output capacitor zero ESR frequency

$$F_P = \frac{1}{2\pi \times A \times C_{OUT}} \rightarrow$$

$$9.548\ kHz = \frac{1}{2\pi \times 0.379\ \Omega \times 44\ \mu F} \quad \text{(eq. 40)}$$

where:

A = Un-scaled gain
C_{OUT} = Output capacitor
F_P = Current mode pole frequency

The two equations above define the bode plot that the power stage has created or open loop response of the system. The next step is to close the loop by considering the feedback values. The closed loop crossover frequency should be less than 1/10 of the switching frequency, which would place the maximum crossover frequency at 50 kHz.

Figure 45 shows a pseudo Type III transconductance error amplifier.

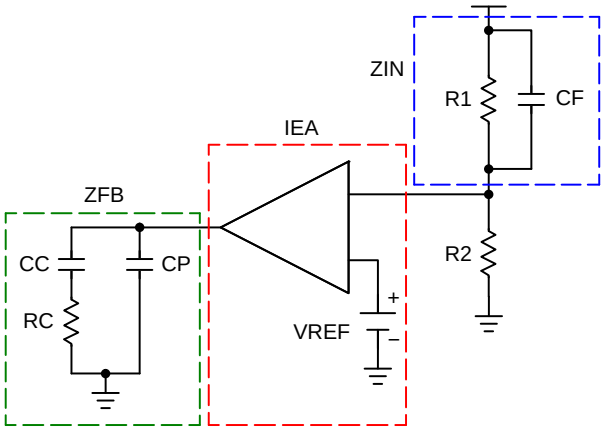


Figure 45. Pseudo Type III Transconductance Error Amplifier

The compensation network consists of the internal error amplifier and the impedance networks Z_{IN} (R_1, R_2, and C_F) and external Z_{FB} (R_C, C_C, and C_P). The compensation network has to provide a closed loop transfer function with the highest 0 dB crossing frequency to have fast response and the highest gain in DC conditions, so as to minimize load regulation issues. A stable control loop has a gain crossing with −20 dB/decade slope and a phase margin greater than 45°. Include worst-case component variations when determining phase margin. To start the design, a resistor value should be chosen for R_1 from which all other components can be chosen. A good starting value is 24.9 kΩ.

The NCP3170 allows the output of the DC−DC regulator to be adjusted down to 0.8 V via an external resistor divider network. The regulator will maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to V_{OUT}, the regulator will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin.

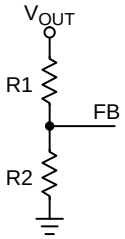


Figure 46. Feedback Resistor Divider

The relationship between the resistor divider network above and the output voltage is shown in Equation 41:

$$R_2 = R_1 \times \left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right) \quad \text{(eq. 41)}$$

where:

R_1 = Top resistor divider
R_2 = Bottom resistor divider
V_{OUT} = Output voltage
V_{REF} = Regulator reference voltage

The most frequently used output voltages and their associated standard R_1 and R_2 values are listed in the table below.

Table 7. OUTPUT VOLTAGE SETTINGS

V_O (V)	R_1 (kΩ)	R_2 (kΩ)
0.8	24.9	Open
1.0	24.9	100
1.1	24.9	66.5
1.2	24.9	49.9
1.5	24.9	28.7
1.8	24.9	20
2.5	24.9	11.8
3.3	24.9	8.06
5.0	24.9	4.64

The compensation components for the Pseudo Type III Transconductance Error Amplifier can be calculated using the method described below. The method serves to provide a good starting place for compensation of a power supply. The values can be adjusted in real time using the compensation tool CompCalc
http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP

The first pole to crossover at the desired frequency should be setup at FPO to decrease at −20 dB per decade:

$$F_{PO} = \frac{F_{CROSS}}{G} \rightarrow \quad \text{(eq. 42)}$$

$$1.354\ kHz = \frac{50\ kHz}{36.925} \rightarrow$$

where:

F_{cross} = Cross over frequency
F_{PO} = Pole frequency to meet crossover frequency
G = DC gain of the plant

The crossover combined compensation network can be used to calculate the transconductance output compensation network as follows:

$$C_C = \frac{y \times gm}{2 \times \pi \times F_{PO}} \rightarrow \quad \text{(eq. 43)}$$

$$5.70\ nF = \frac{0.242 \times 200\ \mu s}{2\pi \times 1.354\ kHz}$$

where:

C_C = Compensation capacitor
F_{PO} = Pole frequency
gm = Transconductance of amplifier
y = Amplitude ratio

$$C_F = \frac{R1 + R2}{2\pi \times (R1 * RF + R2 * RF + R2 * R1) \times F_{cross}} \rightarrow \quad \text{(eq. 46)}$$

$$456\ pF = \frac{24.9\ k\Omega + 7.87\ k\Omega}{2\pi \times (24.9\ k\Omega * 1\ k\Omega + 7.87\ k\Omega * 1\ k\Omega + 7.87\ k\Omega * 24.9\ k\Omega) \times 50\ kHz}$$

where:

C_F = Compensation pole capacitor
F_{cross} = Cross over frequency
gm = Transconductance of amplifier
R_1 = Top resistor divider
R_2 = Bottom resistor divider
R_F = Feed through resistor

Calculating Input Inrush Current

The input inrush current has two distinct stages: input charging and output charging. The input charging of a buck stage is usually controlled, but there are times when it is not and is limited only by the input RC network, and the output impedance of the upstream power stage. If the upstream power stage is a perfect voltage source and switches on instantaneously, then the input inrush current can be depicted as shown in Figure 47 and calculated as:

$$R_C = \frac{1}{2\pi \times C_C \times F_P} \rightarrow \quad \text{(eq. 44)}$$

$$2.925\ k\Omega = \frac{1}{2\pi \times 5.70\ nF \times 1.354\ kHz}$$

where:

C_C = Compensation capacitance
C_{OUT} = Output capacitance
F_P = Current mode pole frequency
R_C = Compensation resistor

$$C_P = \frac{1}{2\pi \times R_C \times F_{ESR}} \rightarrow \quad \text{(eq. 45)}$$

$$75.2\ pF = \frac{1}{2\pi \times 2.925\ k\Omega \times 723\ kHz}$$

where:

C_P = Compensation pole capacitor
F_{ESR} = Capacitor ESR zero frequency
R_C = Compensation resistor

If the ESR frequency is greater than the switching frequency, a CF compensation capacitor may be needed for stability as the output LC filter is considered high Q and thus will not give the phase boost at the crossover frequency. Further at low duty cycles due to some blanking and filtering of the current signal the current gain of the converter is not constant and the current gain is small. Thus adding CF and RF can give the needed phase boost.

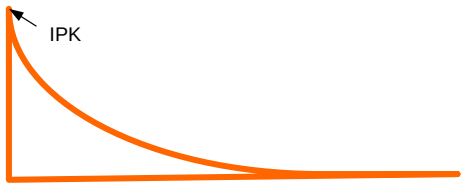


Figure 47. Input Charge Inrush Current

$$I_{ICinrush\_PK}1 = \frac{V_{IN}}{CIN_{ESR}} \quad \text{(eq. 47)}$$

$$1.2\ kA = \frac{12}{0.01}$$

$$I_{ICinrush\_RMS}1 = \frac{V_{IN}}{CIN_{ESR}} \times 0.316 \times \sqrt{\frac{5 \times CIN_{ESR} \times C_{IN}}{t_{DELAY\_TOTAL}}} \quad \text{(eq. 48)}$$

$$12.58\ A = \frac{12\ V}{0.01} \times 0.316 \times \sqrt{\frac{5 \times 0.01\ \Omega \times 22\ \mu F}{1\ ms}}$$

where:

C_{IN} = Output capacitor
CIN_{ESR} = Output capacitor ESR
t_{DELAY_TOTAL} = Total delay interval
V_{IN} = Input Voltage

Once the t_{DELAY_TOTAL} has expired, the buck converter starts to switch and a second inrush current can be calculated:

$$I_{OCinrush\_RMS} = \frac{\left(C_{OUT} + C_{LOAD}\right) \times V_{OUT}}{t_{SS}} \frac{D}{\sqrt{3}} + I_{CL} \times D \quad \text{(eq. 49)}$$

where:

C_{OUT} = Total converter output capacitance
C_{LOAD} = Total load capacitance
D = Duty ratio of the load
I_{CL} = Applied load at the output
$I_{OCinrush\_RMS}$ = RMS inrush current during start-up
t_{SS} = Soft start interval
V_{OUT} = Output voltage

From the above equation, it is clear that the inrush current is dependent on the type of load that is connected to the output. Two types of load are considered in Figure 48: a resistive load and a stepped current load.

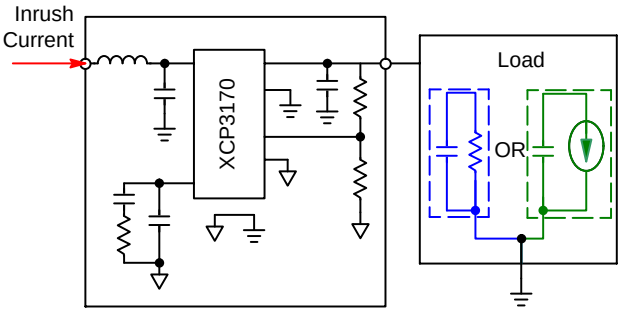


Figure 48. Load Connected to the Output Stage

If the load is resistive in nature, the output current will increase with soft start linearly which can be quantified in Equation 50.

$$I_{CLR\_RMS} = \frac{1}{\sqrt{3}} \times \frac{V_{OUT}}{R_{OUT}} \qquad I_{CR\_PK} = \frac{V_{OUT}}{R_{OUT}} \quad \text{(eq. 50)}$$

$$191\ mA = \frac{1}{\sqrt{3}} \times \frac{3.3\ V}{10\ \Omega} \qquad 300\ mA = \frac{3.3\ V}{10\ \Omega}$$

where:

I_{CLR_RMS} = RMS resistor current
I_{CR_PK} = Peak resistor current
R_{OUT} = Output resistance
V_{OUT} = Output voltage

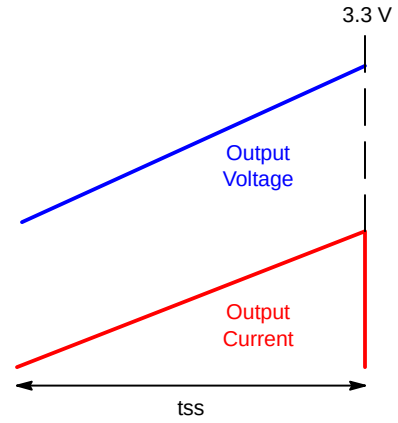


Figure 49. Resistive Load Current

Alternatively, if the output load has an under voltage lockout, turns on at a defined voltage level, and draws a constant current, then the RMS connected load current is:

$$I_{CL1} = \sqrt{\frac{V_{OUT} - V_{OUT\_TO}}{V_{OUT}}} \times I_{OUT} \quad \text{(eq. 51)}$$

$$492\ mA = \sqrt{\frac{3.3\ V - 2.5\ V}{3.3\ V}} \times 1\ A$$

where:

I_{OUT} = Output current
V_{OUT} = Output voltage
V_{OUT_TO} = Output voltage load turn on

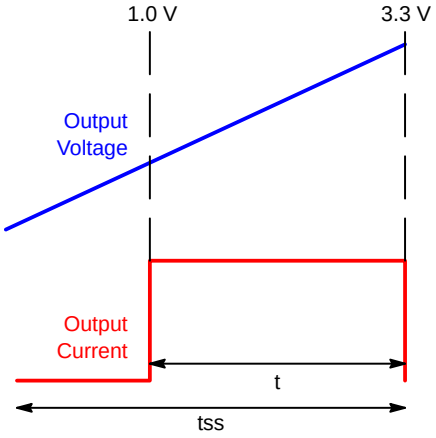


Figure 50. Voltage Enable Load Current

If the inrush current is higher than the steady state input current during max load, then an input fuse should be rated accordingly using I^2t methodology.

THERMAL MANAGEMENT AND LAYOUT

Consideration

In the NCP3170 buck regulator high pulsing current flows through two loops as shown in the figure below.

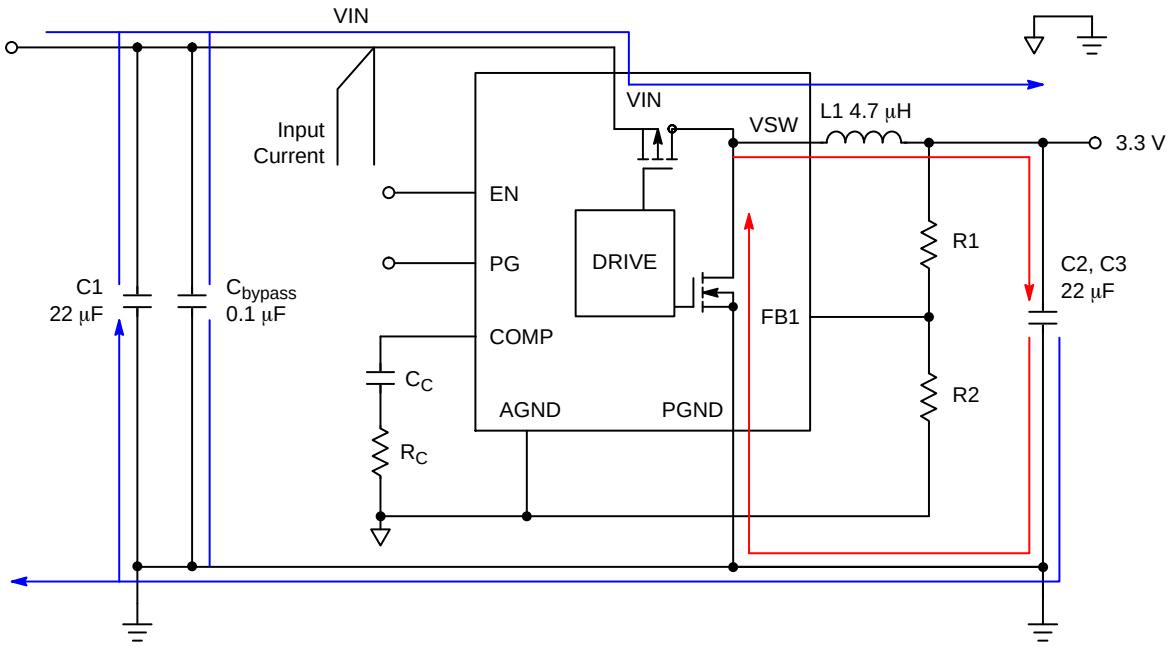


Figure 51. Buck Converter Current Paths

The first loop shown in blue activates when the high side switch turns on. When the switch turns on, the edge of the current waveform is provided by the bypass capacitor. The remainder of the current is provided by the input capacitor. Slower currents are provided by the upstream power supply which fills up the input capacitor when the high side switch is off. The current flows through the high side MOSFET and to the output, charging the output capacitors and providing current to the load. The current returns through a PCB ground trace where the output capacitors are connected, the regulator is grounded, and the input capacitors are grounded. The second loop starts from the inductor to the output capacitors and load, and returns through the low side MOSFET. Current flows in the second loop when the low side NMOSFET is on. The designer should note that there are locations where the red line and the blue line overlap; these areas are considered to have DC current. Areas containing a single blue line indicate that AC currents flow and transition very quickly. The key to power supply layout is to focus on the connections where the AC current flows.

A good rule of thumb is that for every inch of PCB trace, 20 nH of inductance exists. When laying out a PCB, minimizing the AC loop area reduces the noise of the circuit and improves efficiency. A ground plane is strongly recommended to connect the input capacitor, output capacitor, and PGND pin of the NCP3170. Drawing the real high power current flow lines on the recommended layout is important so the designer can see where the currents are flowing.

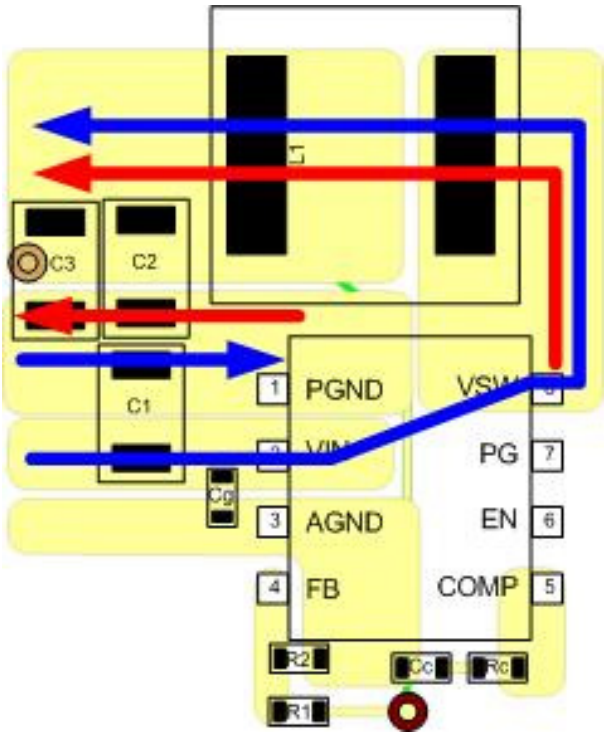


Figure 52. Recommended Signal Layout

The NCP3170 is the major source of power dissipation in the system for which the equations above detailed the loss mechanisms. The control portion of the IC power dissipation is determined by the formula below:

$$P_C = I_C \times V_{IN} \quad \text{(eq. 52)}$$

where:

I_{CC} = Control circuitry current draw
P_C = Control power dissipation
V_{IN} = Input voltage

Once the IC power dissipations are determined, the designer can calculate the required thermal impedance to maintain a specified junction temperature at the worst case ambient temperature. The formula for calculating the junction temperature with the package in free air is:

$$T_J = T_A + P_D \times R_{\theta JA} \quad \text{(eq. 53)}$$

where:

P_D = Power dissipation of the IC
$R_{\theta JA}$ = Thermal resistance junction to ambient of the regulator package
T_A = Ambient temperature
T_J = Junction temperature

The thermal performance of the NCP3170 is strongly affected by the PCB layout. Extra care should be taken by users during the design process to ensure that the IC will operate under the recommended environmental conditions. As with any power design, proper laboratory testing should be performed to ensure the design will dissipate the required power under worst case operating conditions. Variables considered during testing should include maximum ambient temperature, minimum airflow, maximum input voltage, maximum loading, and component variations (i.e., worst case MOSFET $R_{DS(on)}$). Several layout tips are listed below for the best electric and thermal performance. Figure 53 illustrates a PCB layout example of the NCP3170.

1. The VSW pin is connected to the internal PFET and NFET drains, which are a low resistance thermal path. Connect a large copper plane to the VSW pin to help thermal dissipation. If the PG pin is not used in the design, it can be connected to the VSW plane, further reducing the thermal impedance. The designer should ensure that the VSW thermal plane is rounded at the corners to reduce noise.
2. The user should not use thermal relief connections to the VIN and the PGND pins. Construct a large plane around the PGND and VIN pins to help thermal dissipation.
3. The input capacitor should be connected to the VIN and PGND pins as close as possible to the IC.
4. A ground plane on the bottom and top layers of the PBC board is preferred. If a ground plane is not used, separate PGND from AGND and connect them only at one point to avoid the PGND pin noise coupling to the AGND pin.
5. Create copper planes as short as possible from the VSW pin to the output inductor, from the output inductor to the output capacitor, and from the load to PGND.
6. Create a copper plane on all of the unused PCB area and connect it to stable DC nodes such as: V_{IN}, GND, or V_{OUT}.
7. Keep sensitive signal traces far away from the VSW pins or shield them.

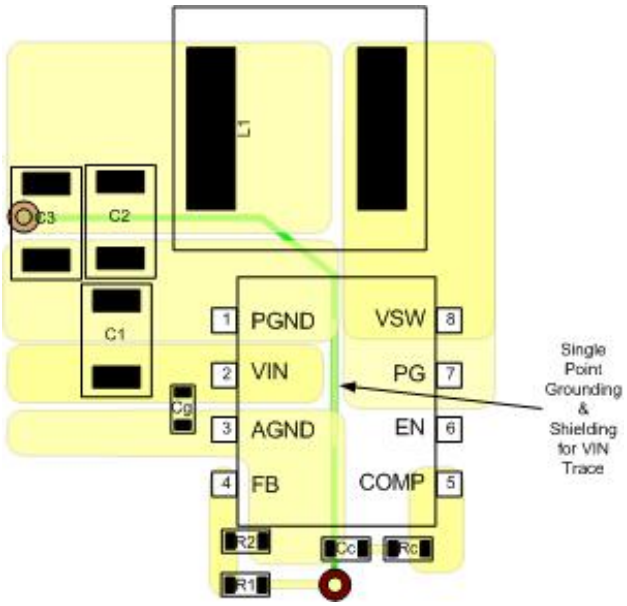


Figure 53. Recommend Thermal Layout

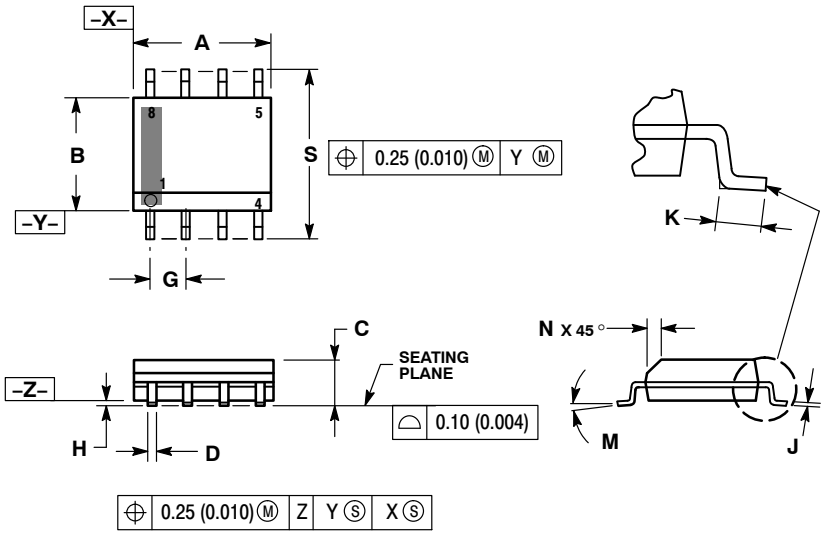
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

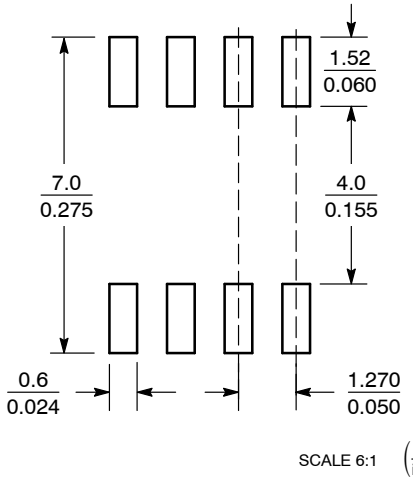
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

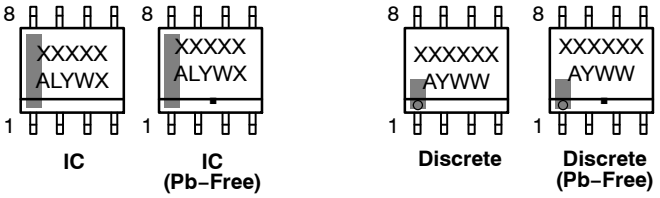
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:

NCP3170ADR2G NCP3170BDR2G