NCP3120

Dual 2.0 A, Step-Down DC/DC Switching Regulator

The NCP3120 is a dual buck converter designed for low voltage applications requiring high efficiency. This device is capable of producing an output voltage as low as 0.8 V. The NCP3120 provides dual 2.0 A switching regulators with an adjustable 200 kHz − 750 kHz switching frequency. The switching frequency is set by an external resistor. The NCP3120 also incorporates an auto−tracking and sequencing feature. Protection features include cycle−by−cycle current limit and undervoltage lockout (UVLO). The NCP3120 comes in a 32−pin QFN package.

Features

- Input Voltage Range from 4.5 V to 13.2 V
- 12 V_{in} to 5.0 V_{out} = 87% Efficiency Min @ 2.0 A
- 200−750 kHz Operation
- Stable with Low ESR Ceramic Output Capacitor
- 0.8 ±1.5% FB Reference Voltage
- External Soft−Start
- Out of Phase Operation of OUT1 & OUT2
- Auto−Tracking and Sequencing
- Enable/Disable Capability
- Hiccup Overload Protection
- Low Shutdown Power (I_q < 100 μA)

Typical Applications

- Set−Top Boxes, Portable Applications, Networking and Telecommunications
- DSP/μP/FPGA Core

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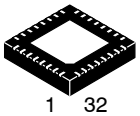


QFN32
CASE 488AM

MARKING DIAGRAM

NCP3120 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 40 of this data sheet.

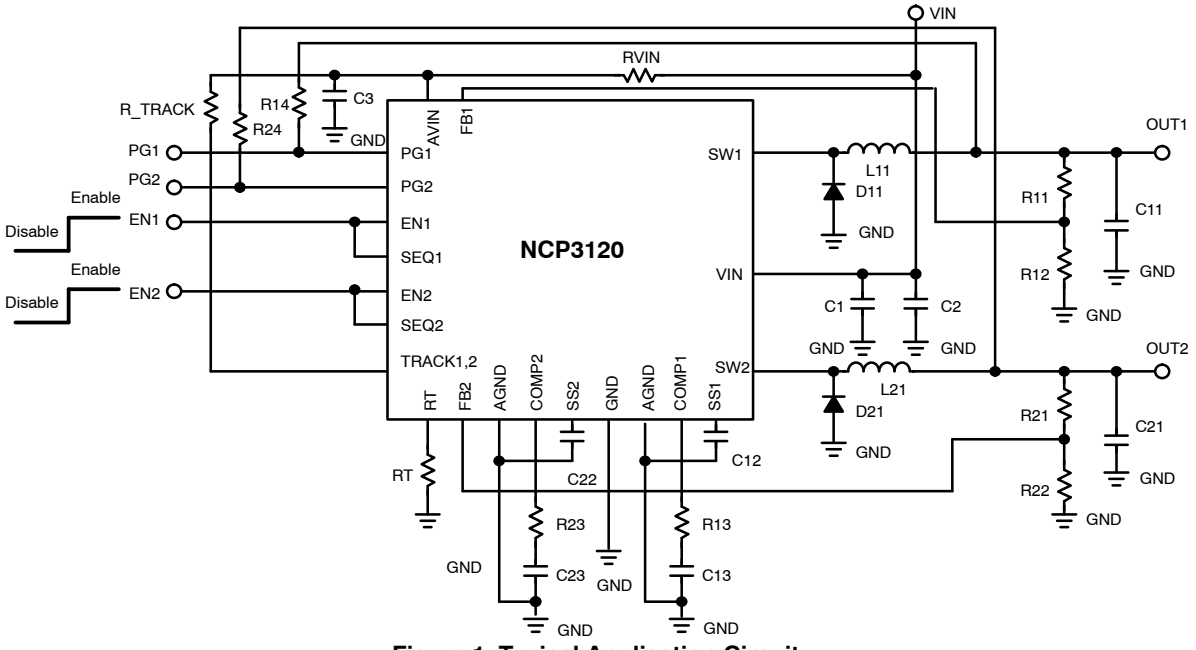


Figure 1. Typical Application Circuit

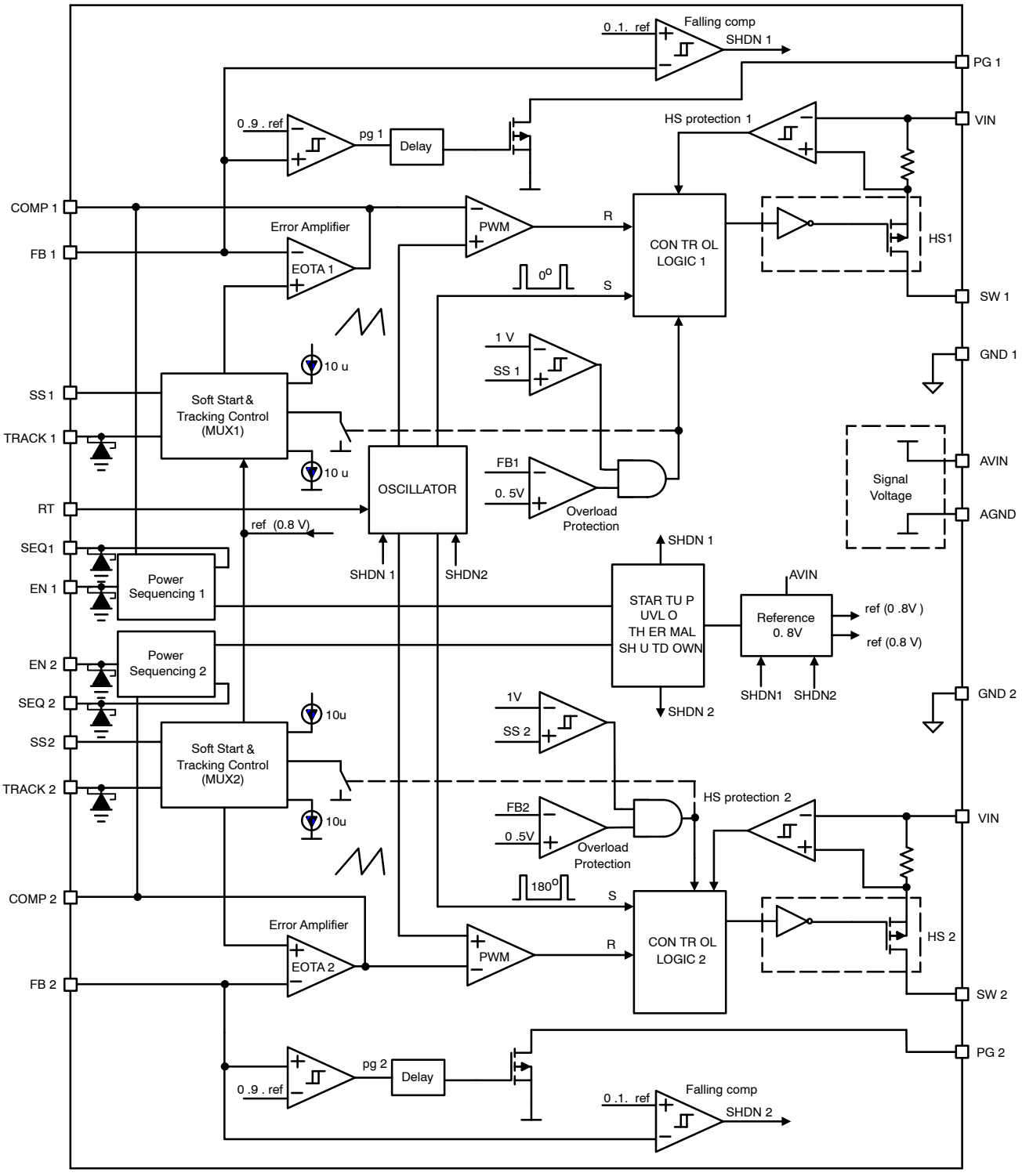


Figure 2. Block Diagram

PIN DESCRIPTION

Pin	Symbol	Description
1, 31, 32	SW1	Switch node of Channel 1. Connect an inductor between SW1 and the regulator output.
2 – 7	V_{IN}	Input power supply voltage pins. These pins should be connected together to the input signal supply voltage pin.
8 – 10	SW2	Switch node of Channel 2. Connect an inductor between SW2 and the regulator output.
11	GND2	Power ground for Channel 2
12	SS2	Soft−start control input for Channel 2. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
13	COMP2	Compensation pin of Channel 2. This is the output of the error amplifier and inverting input of the PWM comparator.
14	AGND	Analog ground; connect to GND1 and GND2.
15	FB2	Feedback Pin. Used to set the output voltage of Channel 2 with a resistive divider from the output.
16	RT	Resistor select for the oscillator frequency. Connect a resistor from the RT pin to AGND to set the frequency of the master oscillator. Leave this pin floating, for 200 kHz operation.
17	TRACK 2	Tracking input for Channel 2. This pin allows the user to control the rise time of the second output. This pin must be tied high in the normal operation (except in the tracking mode).
18	TRACK 1	Tracking input for Channel 1. This pin allows the user to control the rise time of the first output. This pin must be tied high in the normal operation (except in the tracking mode).
19	SEQ2	Sequence pin for Channel 2. I/O used in power sequencing. Connect SEQ to EN for normal operation of a standalone device.
20	EN2	Enable input for Channel 2.
21	SEQ1	Sequence pin for Channel 1. I/O used in power sequencing. Connect SEQ to EN for normal operation of a standalone device.
22	EN1	Enable input for Channel 1.
23	PG2	Power good, open−drain output of Channel 2. Output logic is pulled to ground when the output is less than 90% of the desired output voltage. Tied to an external pull−up resistor. Leave this pin floating, if not used.
24	PG1	Power good, open−drain output of Channel 1. Output logic is pulled to ground when the output is less than 90% of the desired output voltage. Tied to an external pull−up resistor. Leave this pin floating, if not used.
25	AV_{IN}	Input signal supply voltage pin.
26	FB1	Feedback Pin. Used to set the output voltage of Channel 1 with a resistive divider from the output.
27	AGND	Analog ground. Connect to GND1 and GND2.
28	COMP1	Compensation pin of Channel 1. This is the output of the error amplifier and inverting input of the PWM comparator.
29	SS1	Soft−start/stop control input for Channel 1. An internal current source charges an external capacitor connected to this pin to set the soft−start time.
30	GND1	Power ground for Channel 1.
	Exposed Pad (GND)	The exposed pad at the bottom of the package is the electrical ground connection of the NCP3120. This node must be tied to ground.

MAXIMUM RATINGS

Characteristics	Symbol	Min	Max	Unit
Power Supply Voltage Input	V_{VIN}	−0.3	15	V
Signal Supply Voltage Input	V_{AVIN}	−0.3	15	V
SW Pin Voltage	V_{SW}	−0.7 −5V for < 50 ns	V_{VIN}	V
EN Pin Voltage Input	V_{EN}	−0.3	8.0	V
SEQ Pin Voltage Output	V_{SEQ}	−0.3	8.0	
PG Pin Voltage	V_{PG}	−0.3	5.5	V
All Other Pins	–	−0.3	5.5	°V
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	50		°C/W
Storage Temperature Range	T_{STG}	−55 to +150		°C
Junction Operating Temperature (Note 2)	T_J	−40 to +150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $R_{\theta JA}$ on a 100 x 100 mm PCB with two solid 1 oz ground planes.
2. The maximum package power dissipation limit must not be exceeded

$$P_D = \frac{T_{J\ (max)} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 125°C, T_J = 25°C for typical values, V_{AVIN} =12 V, V_{VIN} =12 V, unless otherwise noted. R_T = open kΩ)

Characteristic	Conditions	Min	Typ	Max	Unit
RECOMMENDED OPERATING CONDITIONS					
Input Voltage Range		4.5		13.2	V
SUPPLY CURRENT					
Quiescent Supply Current	V_{EN} = H, V_{FB} = 1.0 V No Switching, PG open		5.0	7.0	mA
Shutdown Supply Current	V_{EN} = 0 V, PG open			100	μA
UNDERVOLTAGE LOCKOUT					
UVLO Threshold	V_{IN} Rising Edge V_{IN} Falling Edge	 3.9	4.3 4.1	4.5	V
UVLO Hysteresis		0.15	0.20	0.25	V
SWITCHING REGULATOR					
Minimum Duty Cycle	Comp = 0.6 V			0	%
Maximum Duty Cycle	Comp = 2.6 V	90			%
High Side MOSFET $R_{DS(on)}$	I_{SW} = 0.5 A, T_J = 25°C		250		mΩ
High Side Leakage Current	V_{EN} = 0V, V_{SW} = 0V			10	μA
High Side Switch Current Limit Set Point	(Note 3)	2.6	3.2	3.8	A
Current Loop Transient Response	(Note 4)		100		nsec
FB					
V_{FB} Feedback Voltage	T_J = 25°C T_J = −40 to 125°C, 4.5 V < V_{IN} < 13.2V	0.788 0.784	0.8 –	0.812 0.816	V
OSC					
Oscillator Frequency	T_J = 25°C, T_J = −40 to 125°C T_J = 25°C, T_J = −40 to 125°C (RT = 52.3 kΩ)	180 170 635	200 200 750	220 230 865	kHz kHz kHz
Standard Oscillator Frequency Range	T_J = 25°C	200		750	kHz
TRANSCONDUCTANCE ERROR AMPLIFIER (GM)					
Transconductance	(Note 4)	0.9	1.0	1.1	mS
DC Gain	(Note 4)	50	55	60	dB
Unity Gain Bandwidth	(Note 4)		4.0		MHz
Output Sink Current	V_{FB} = 1.0 V, Vcomp = 1.5 V	80	100		μA
Output Source Current	V_{FB} = 0.6 V, Vcomp = 1.5 V	80	100		μA
Input Bias Current	V_{FB} = 0.8 V		100	500	nA
Comp Pin Operating Voltage Range	(Note 4)	0.6		2.6	V
SOFT−START					
Soft−Start Period	V_{FB} < 0.8 V, C_S = 0.1 μF		10		ms
Soft−Start Voltage Range		0		V_{FB}	V
Soft−Start Current Source	Charging, V_{SS} = 1 V Discharging, V_{SS} = 1 V	6.0 6.0	8.0 8.0	12 12	μA μA

ELECTRICAL CHARACTERISTICS ($-40°C < T_J < 125°C$, $T_J = 25°C$ for typical values, V_{AVIN} =12 V, V_{VIN} =12 V, unless otherwise noted. R_T = open kΩ)

Characteristic	Conditions	Min	Typ	Max	Unit
TRACK					
Tracking Voltage Range		0		V_{FB}	V
Tracking Voltage Offset	V_{TRACK} = 0.6 V			15	mV
Track Bias Current	V_{TRACK} = 0.6 V		100	500	nA
POWER GOOD					
PG Threshold	Feedback Voltage Rising, EN Tied to SEQ, V_{PG} = 3.3 V	90% V_{FB}			V
PG Shutdown Mode	Feedback Voltage Falling, EN Tied to SEQ, $V_{EN,SEQ}$ = 0V, V_{PG} = 3.3V	10% V_{FB}	15% V_{FB}	20% V_{FB}	V
PG Delay	Rising Edge of V_{out} Falling Edge of V_{out}		50 10		μs μs
PG Low Level Voltage	$I_{(PG)}$ = 1 mA			0.3	V
PG Hysteresis			45		mV
PG Leakage Current	V_{PG} = 5.5 V			1.0	μA
ENABLE/POWER SEQUENCING					
Enable Internal Pullup Current			4.0		μA
Sequence Internal Pulldown Current			16		μA
Enable Threshold High	EN Tied to SEQ	2.0			V
Sequence Threshold Low	EN Tied to SEQ			0.8	V
THERMAL SHUTDOWN					
Overtemperature Trip Point	(Note 4)		160		°C
Hysteresis			15		°C

3. DC value.
4. Guaranteed by design.

TYPICAL OPERATING CHARACTERISTICS

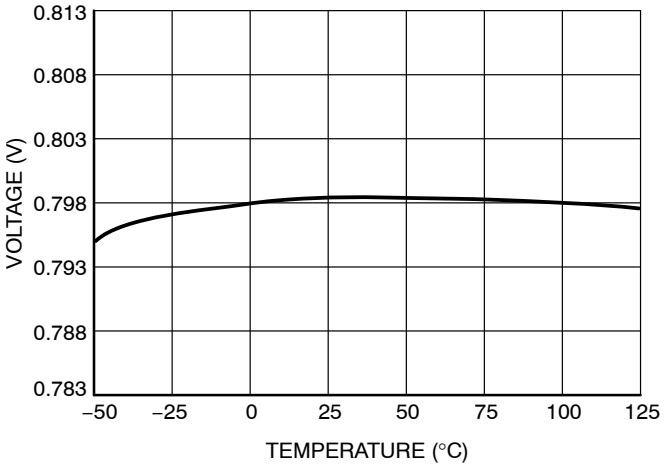


Figure 3. Feedback Voltage vs. Temperature

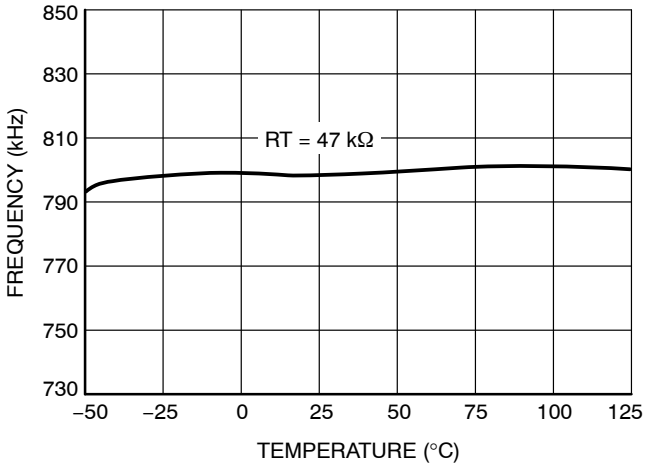


Figure 4. High Switching Frequency vs. Temperature

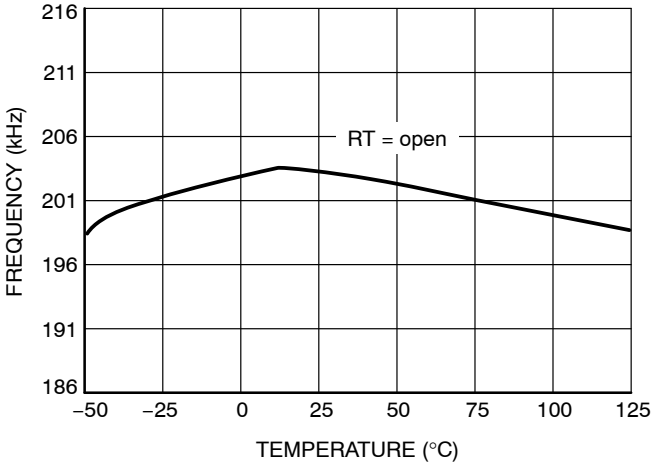


Figure 5. Low Switching Frequency vs. Temperature

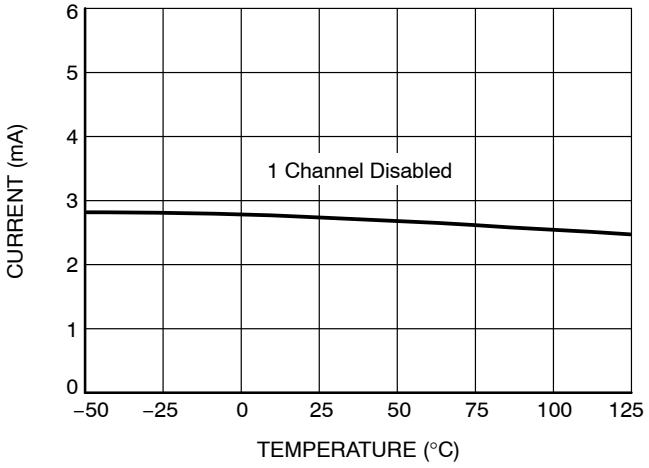


Figure 6. Quiescent Supply Current vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

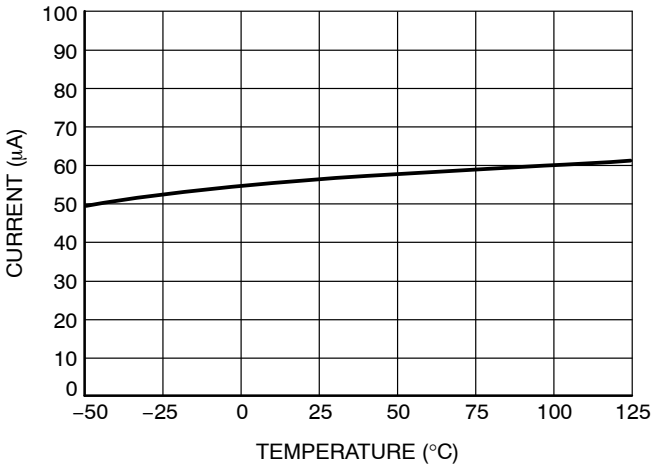


Figure 7. Shutdown Supply Current vs. Temperature

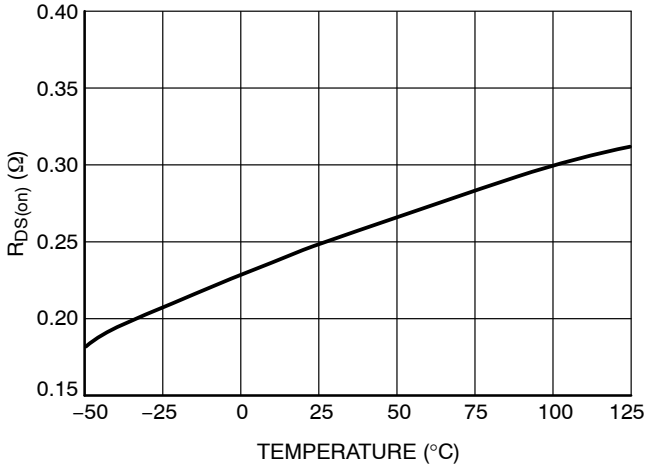


Figure 8. $R_{DS(on)}$ vs. Temperature

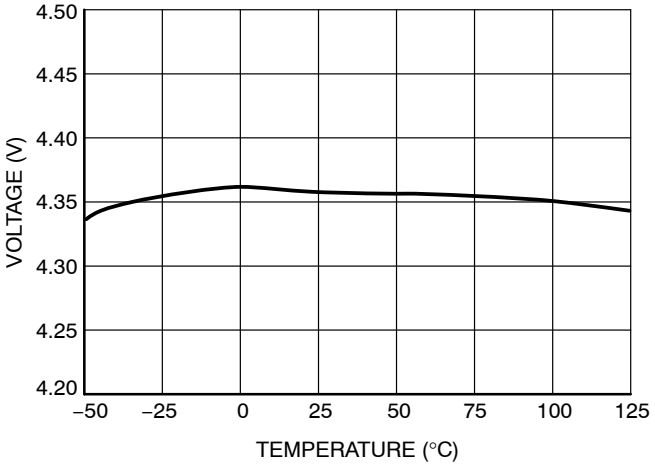


Figure 9. UVLO − Rising Threshold vs. Temperature

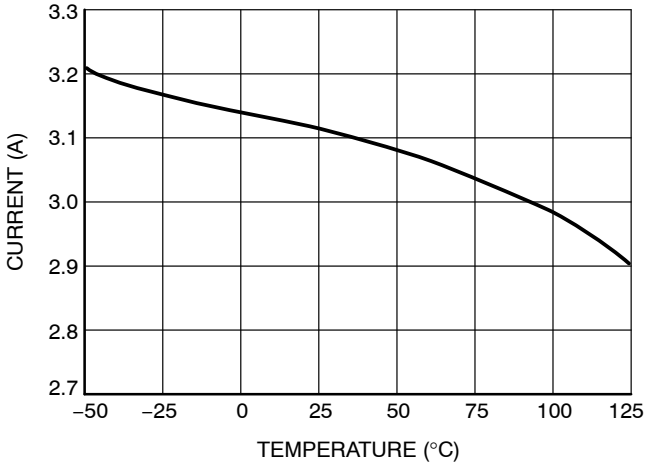


Figure 10. Current Limit vs. Temperature

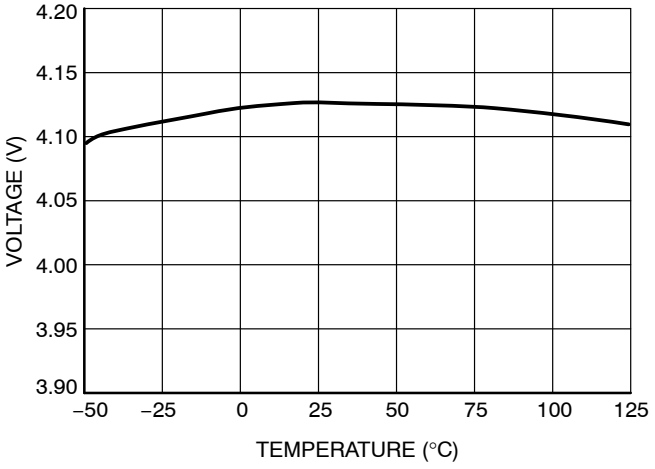


Figure 11. UVLO − Falling Threshold vs. Temperature

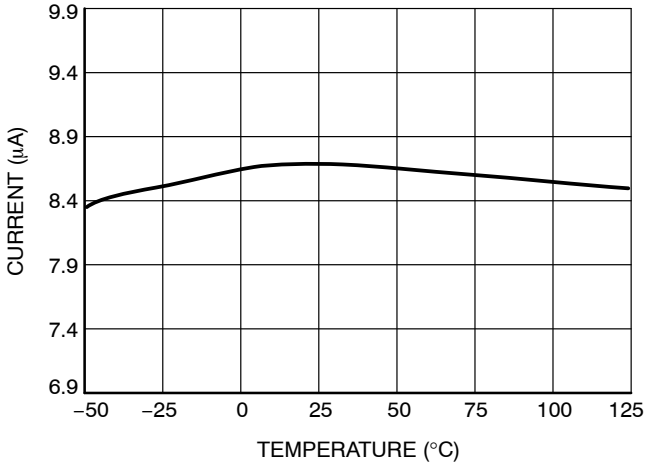


Figure 12. Soft−Start Charge Current vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

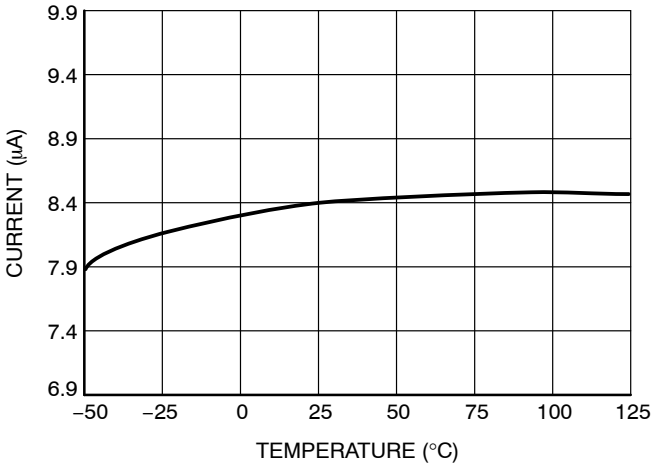


Figure 13. Soft−Start Discharge Current vs. Temperature

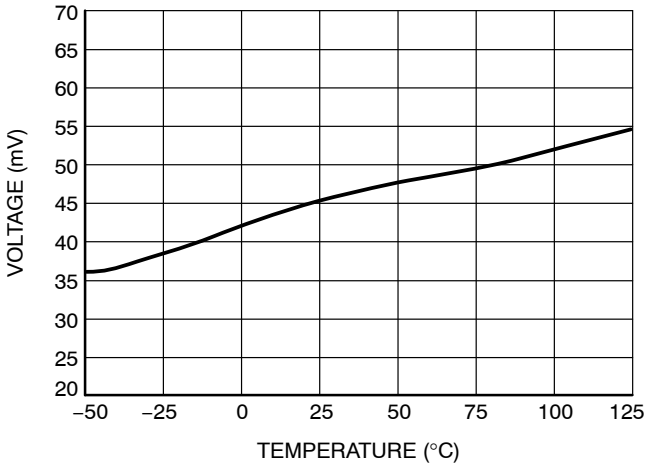


Figure 14. Power Good Hysteresis vs. Temperature

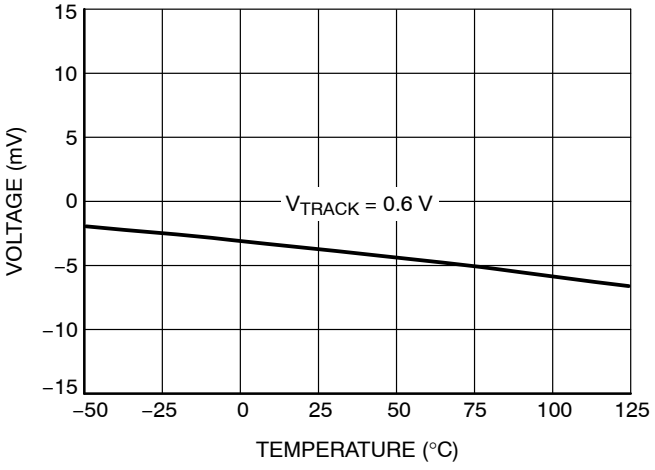


Figure 15. Tracking Voltage Offset vs. Temperature

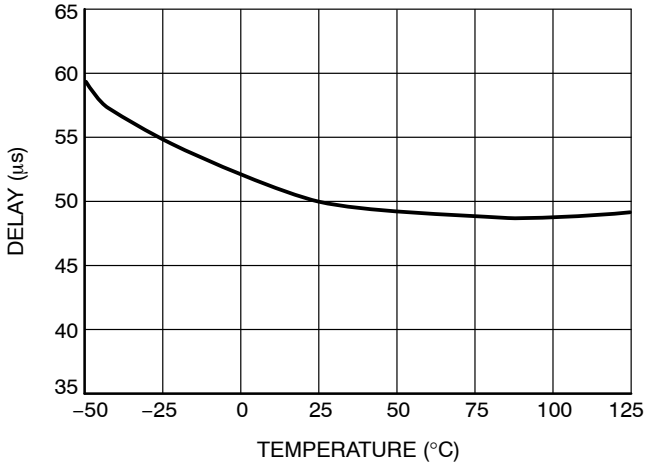


Figure 16. Power Good Rising Delay vs. Temperature

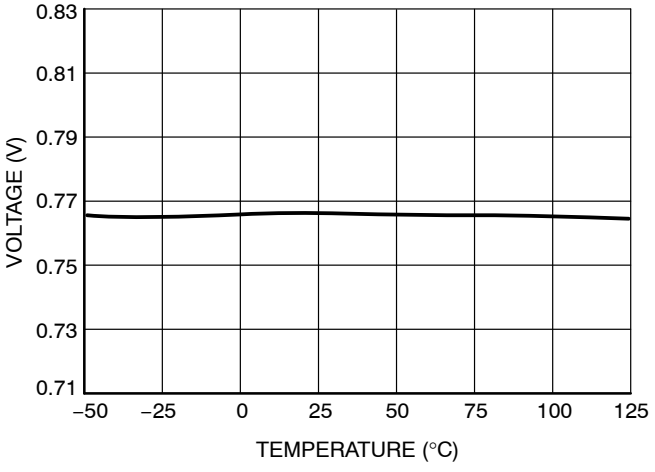


Figure 17. Power Good Feedback Threshold vs. Temperature

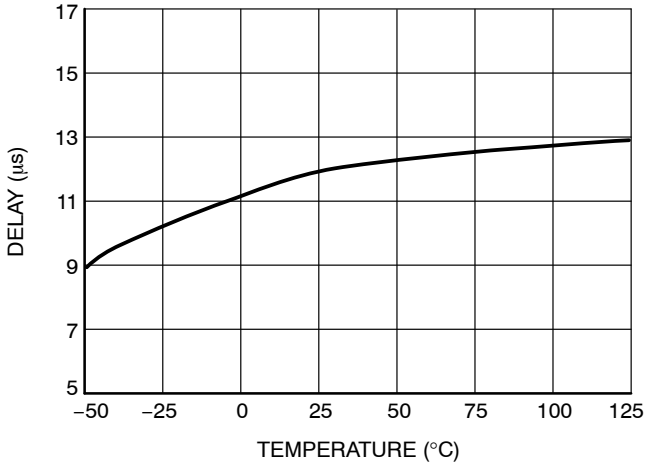


Figure 18. Power Good Falling Delay vs. Temperature

TYPICAL OPERATING CHARACTERISTICS

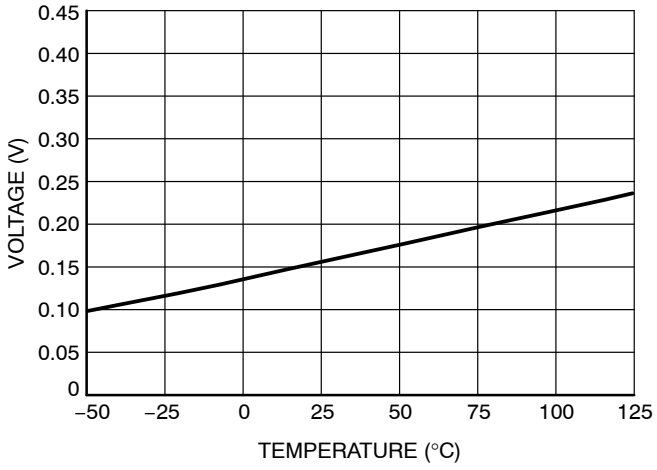


Figure 19. Power Good Saturation Voltage vs. Temperature

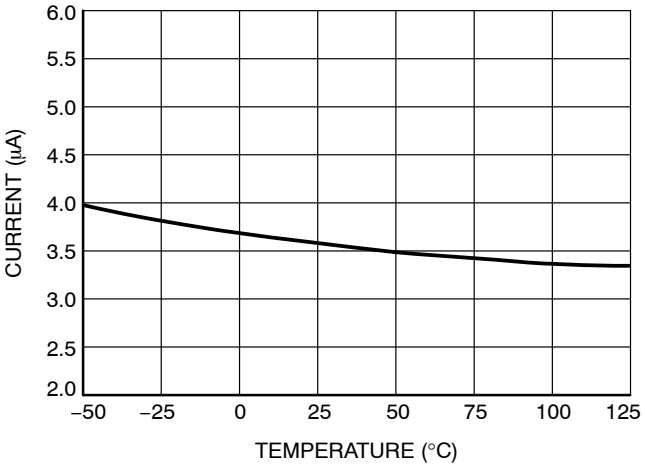


Figure 20. EN Internal Pull−up Current vs. Temperature

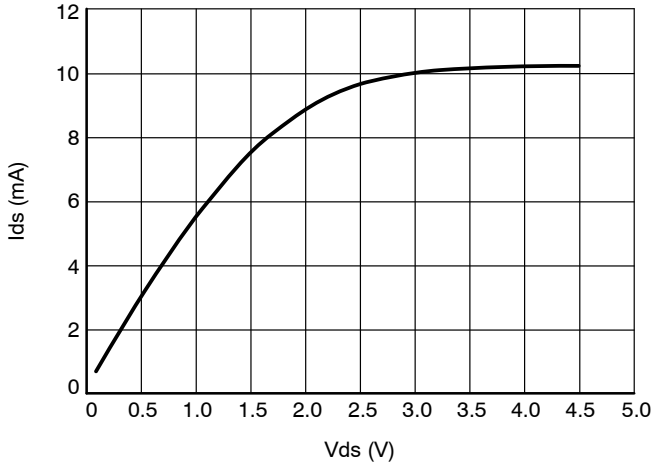


Figure 21. Power Good Current vs. Drain−to−Source Voltage

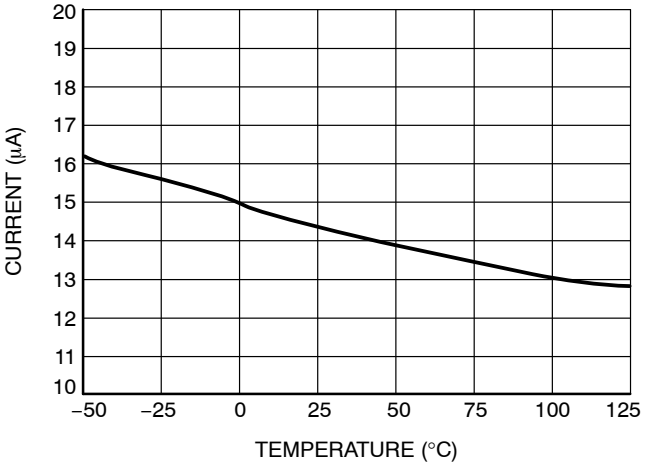


Figure 22. SEQ Internal Pull−down Current vs. Temperature

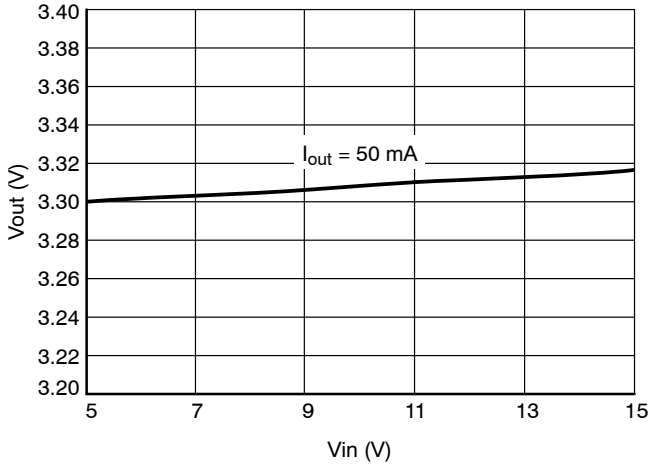


Figure 23. NCP3120 Line Regulation

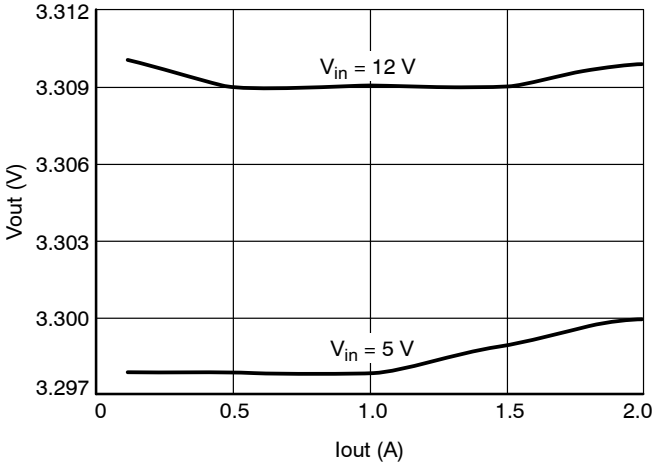


Figure 24. NCP3120 Load Regulation

TYPICAL OPERATING CHARACTERISTICS

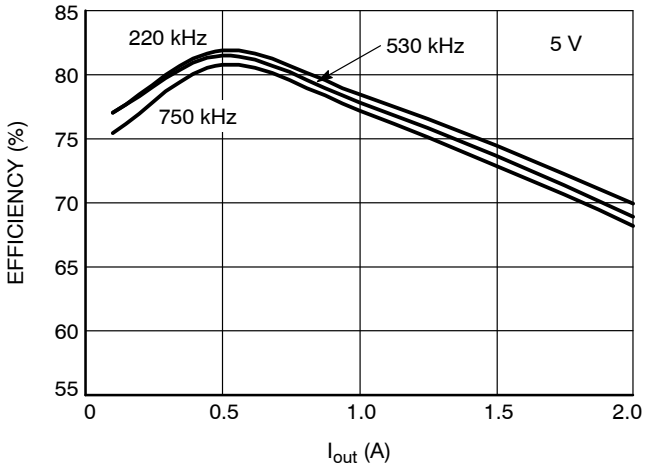


Figure 25. NCP3120 Efficiency, V_{in} = 5 V, V_{out} = 1.8 V, 25°C

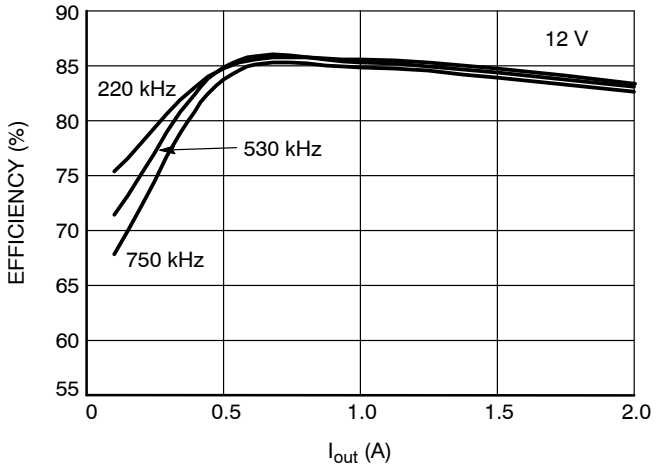


Figure 26. NCP3120 Efficiency, V_{in} = 12 V, V_{out} = 3.3 V, 25°C

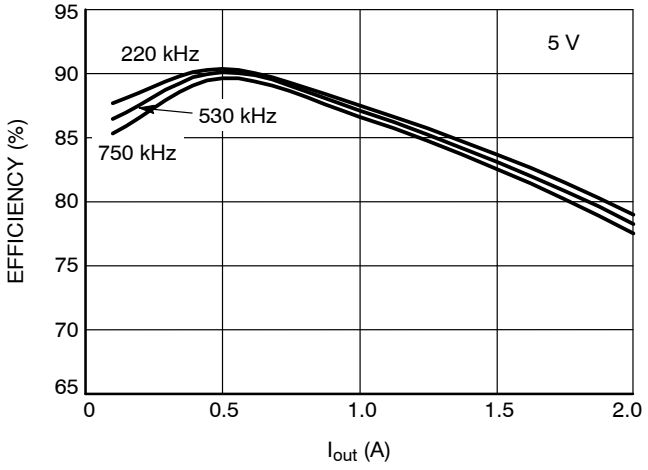


Figure 27. NCP3120 Efficiency, V_{in} = 5 V, V_{out} = 3.3 V, 25°C

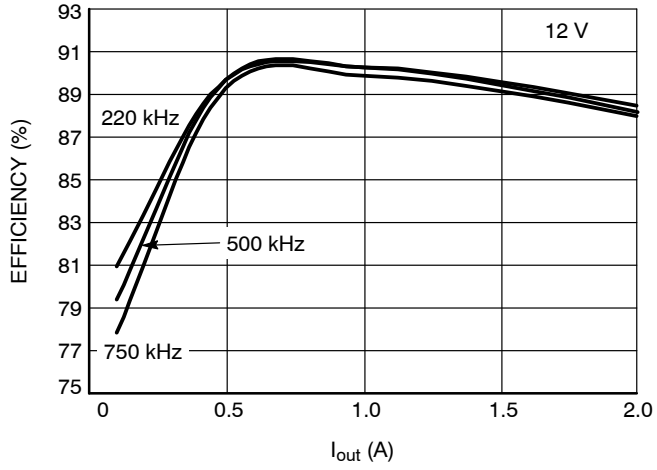


Figure 28. NCP3120 Efficiency, V_{in} = 12 V, V_{out} = 5 V, 25°C

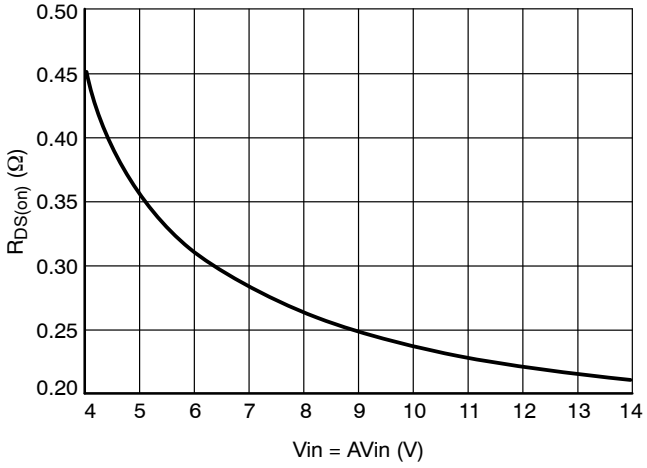


Figure 29. $R_{DS(on)}$ vs. Input Voltage

TYPICAL OPERATING CHARACTERISTICS

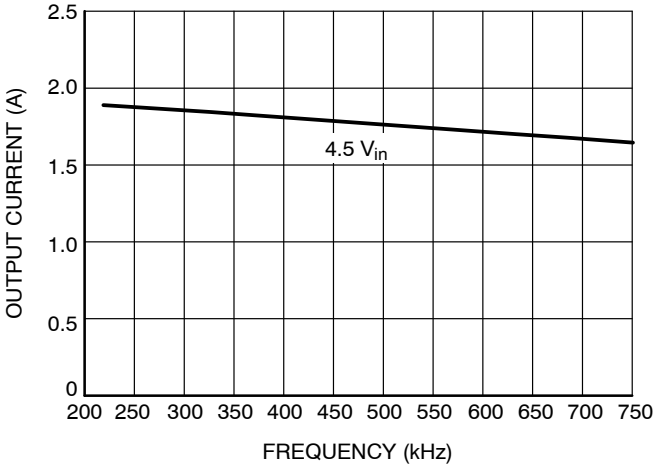


Figure 30. Maximum Currents vs. Operating Frequency due to Toff min limitations 3.3 Vout

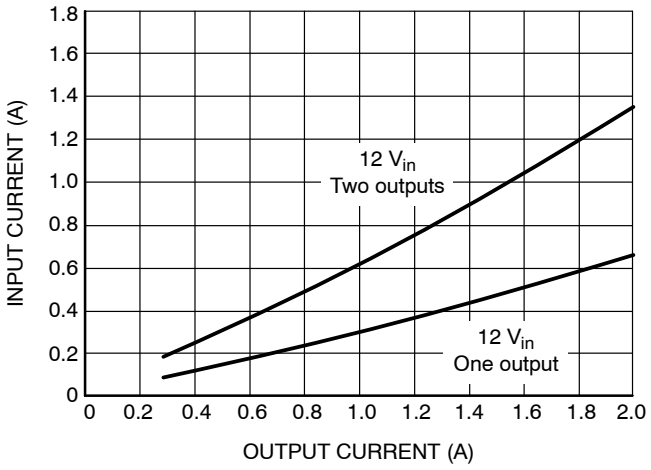


Figure 31. Minimum Input Current 3.3 Vout

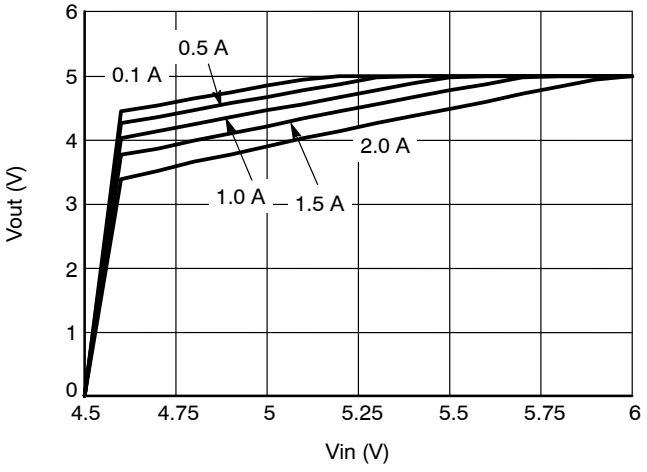


Figure 32. Minimum Input Voltage 5 Vout, 350 kHz

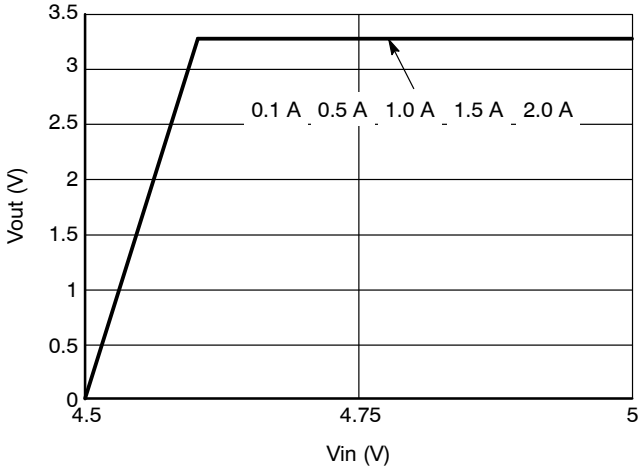


Figure 33. Minimum Input Voltage 3.3 Vout, 350 kHz

DETAILED DESCRIPTION

Introduction

The NCP3120 is a dual channel non−synchronous PWM voltage mode buck regulator. Each channel is identical and has a 2.0 A internal P−FET, compensation, feedback, programmable soft−start, enable and power good pins. These circuits also share the same input voltage, reference voltage, thermal shutdown, undervoltage detect and master oscillator. A simple auto−tracking and sequencing capability can be implemented using the SEQ/TRACK/SS pins.

The fixed−frequency programmable architecture, driven from a common oscillator, ensures a 180° phase differential between channels. This 180° phase shift between the two channels reduces the common input capacitor requirement and improves the noise immunity. The NCP3120 switching frequency is set by an external resistor and is adjustable between 200−750 kHz. This allows application optimization between efficiency and total solution size.

The output voltage is fed back through an external resistor voltage divider to the FB input pin and compared with the reference voltage, then the voltage difference is amplified through the internal transconductance error amplifier. The output current of the transconductance error amplifier (OTA) is presented at the COMP node where an RC network compensates the regulation control system loop.

The NCP3120 features a programmable soft−start function, which is implemented through the error amplifier and the external compensation capacitor. This feature prevents stress to the power components and limits output voltage overshoot during start−up.

Undervoltage Lockout (UVLO)

Undervoltage lockout (UVLO) is provided to ensure that unexpected behavior does not occur when V_{in} is too low to support the internal rails and power the converter. In case the input voltage is higher than the UVLO threshold (4.3 V standard value, rising voltage), the step down converter operation can be started. This circuit has a 0.2 V hysteresis (typical). If the falling trip is activated, switching ceases and eventually the circuit turns off. When the input circuit is in this state, the currrent consumption is equal 5 mA (typical).

Fixed Frequency Operation

The NCP3120 uses a constant frequency architecture for generating a PWM signal. During normal operation, the oscillator generates an accurate pulse at the beginning of each switching cycle to turn on the main switch. The main switch will be turned off when the ramp signal intersects with the output of the error amplifier (COMP pin voltage). Therefore, the switch duty cycle can be modified to regulate the output voltage to the desired value as line and load conditions change.

The major advantage of fixed frequency operation is that the component selections, especially the magnetic component design, become very easy. The oscillator frequency of the NCP3120 is programmable from 200 kHz to 750 kHz using an external resistor connected from the RT pin to ground. The oscillator works on the double frequency internally. Therefore, both channels have a 180° phase shift of the SW pins.

Out−of−Phase Operation

In out−of−phase operation, the turn−on of the second channel is delayed by half the switching cycle. This delay is supervised by the oscillator, which supplies a clock signal to the second channel which is 180° out of phase with the clock signal of the first channel. The advantages of out−of−phase synchronization are many. Since the input current pulses are interleaved with one another, the overlap time is reduced. The effect of this overlap reduction is to attenuate the input filter requirement, allowing the use of smaller components. Additionally, since peak current occurs during a shorter time period, emitted EMI is also reduced, thereby reducing shielding requirements.

Enable Input

Pull the EN enable input high to enable operation. The EN high signal must occur **after VIN has exceeded 2.7 V** to allow internal Power-on Reset (POR) logic to initialize the IC. Logic low on SEQ forces the NCP3120 into shutdown mode. Connect SEQ to EN for normal operation of a standalone device. In shutdown mode, the NCP3120 is turned off and the supply current is reduced to less than 100 μA. When the enable function is not required, float the EN connection. The NCP3120 will turn itself on once Vin crosses the input UVLO threshold. **Do not pull EN to VIN or a separate supply voltage**. For standalone operation, EN should still be connected to SEQ.

Note: For proper operation of the NCP3120 circuit, no voltage may be pulled high on the output pins. The output capacitors should be discharged. If this condition is not observed when NCP3120 is enabled, the regulator does not start switching. This helps to prevent improper operation of the NCP3120 circuit due to the implemented tracking and sequencing features.

Soft−Start/Stop Control

This capacitor limits the maximum demand on the external power supply by controlling the inrush current peaks to charge the output capacitor and DC load and to attain smoothly increasing output voltage at start−up. A soft start circuit forces the error amplifier output to follow a prescribed voltage ramp when turning on and off. The output capacitor is discharged when V_{in} goes under the UVLO as thermal shutdown or overload detection occurs. The circuit input is presented as a voltage ramp generated by internal current sources tied to an external SS capacitor. The external capacitor on the soft−start node is charged/discharged by the 8.75 μA current from the constant current source, and the voltage on the SS node controls the OTA amplifier output

voltage until the SS capacitor is charged/discharged to a voltage higher than 0.8 V.

Power Good

The power good is an open drain and active high output that indicates when the output voltage has reached 90% (min) of the nominal output voltage. This output can be pulled up to the appropriate level with an external resistor.

The power good comparator senses the voltage at the FB pin, which is a function of V_{out}.

The power good output transistor behavior is shown in the "Typical Operating Characteristics" section. The PG pin is held low during a soft−start. Once a soft−start is completed, the PG goes high if there are no faults and no delays associated with it.

Current Limit

The NCP3120 protects a power system if overcurrent occurs. The NCP3120 contains pulse−by−pulse current limiting to protect the power switch and external components. The current through each channel is continuously monitored. The current limit is set to allow peak switch current in excess of 2.6 A (minimum). Current limiting is implemented by monitoring the high−side P−channel switch current during conduction with a current limit comparator. When the peak of the switching current reaches the current limit, the power switch turns off.

Hiccup Overload Protection (OLM – Over Load Mode)

Hiccup mode is a method of protecting the power supply from damage during overload conditions. Within normal operation, the external soft−start capacitor is pulled up by a current source that delivers 8.75 μA to the SS pin capacitor. The soft−start capacitor continues to charge until it reaches the saturation voltage of the current source, typically V_{ss} = 4 V. When the overload condition is detected, the soft−start capacitor is discharged to 0.1 V and is again charged to 1 V. This is periodically repeated until the overload condition is detected. The transconductance error amplifier output is tied to ground when the soft−start capacitor is discharged.

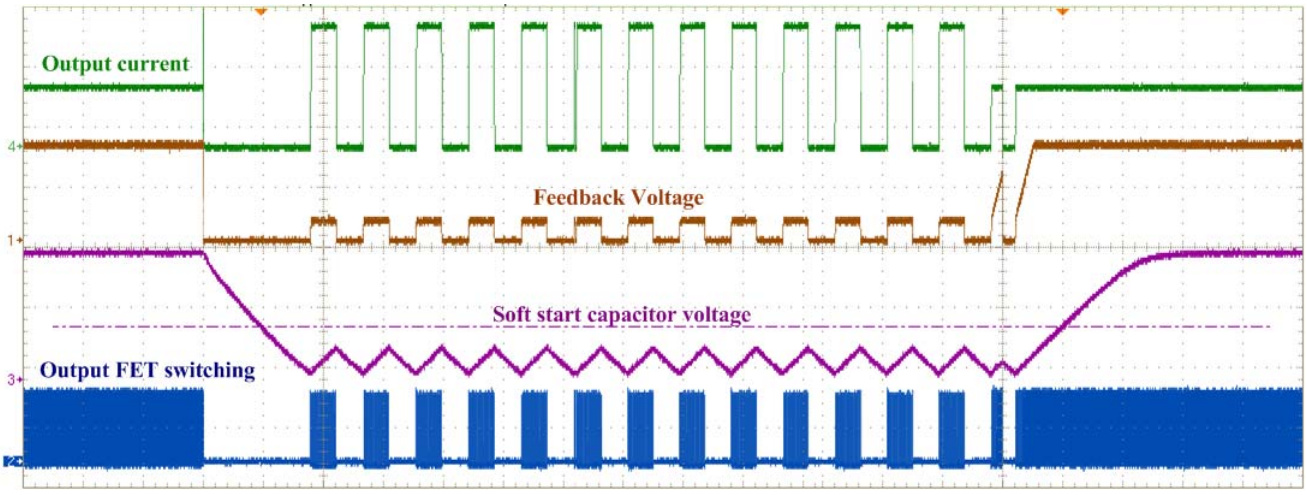


Figure 34. Hiccup Overload Protection

Thermal Shutdown

The NCP3120 has a thermal shutdown feature to protect the device from overheating when the die temperature exceeds 160°C (typically). If the chip temperature exceeds the overtemperature shutdown trip point, the fault signal is activated. This will disable the step down converter operation, and the chip temperature will start to decrease. When the chip temperature drops 15°C below the overtemperature shutdown trip point, the fault signal is deactivated and the step down converter operation starts again with soft−start. The thermal event sends the device immediately into the OFF state. The currrent consumption is equal 5 mA (typical) if the thermal condition is reached.

APPLICATION & DESIGN INFORMATION

Inductor

The output inductor may be the most critical component in the converter because it will directly affect the choice of other components and dictate both the steady state and transient performance of the converter. When choosing inductors, one might have to consider maximum load current, core and copper losses, component height, output ripple, EMI, saturation and cost. Lower inductor values are chosen to reduce the physical size of the inductor. A higher value cuts down the ripple current and core losses and allows more output current. In general, the output inductance value should be as low and the output inductor physically as small as possible to provide the best transient response and minimum cost. If a large inductance value is used, the converter will not respond quickly to rapid changes in the load current. On the other hand, an inductance value that is too low will result in very large ripple currents in the power components, resulting in increased dissipation and lower converter efficiency.

A good standard for determining the inductance to use is to select the inductor peak−to−peak ripple current to be approximately 25% of the maximum switch current. Also, make sure that the inductor peak current is below the maximum switch current limit and the selected inductor type saturation current specification is higher than the peak current through the switch.

The maximum current in the inductor while operating in the continuous current mode is defined as the load current plus one half of the ΔI_L currrent:

$$I_{LP} = I_{LOAD} + \frac{1}{2}\Delta I_L$$

The inductance value can be calculated by:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} \cdot \Delta I_L \cdot f_{OSC}}$$

Therefore, the inductor peak current, I_{LP}, can be calculated by:

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}(V_{IN} - V_{OUT})}{2 \cdot V_{IN} \cdot L \cdot f_{OSC}}$$

where;

I_{LOAD} is the output load current

V_{OUT} is the output voltage

V_{IN} is the input voltage

ΔI_L is the peak−to−peak inductor ripple current

f_{OSC} is the switching frequency of the oscillator

The choice of the appropriate inductor type depends not only on the calculated inductance value, saturation current rating and parasitic serial resistance, but also on the required physical dimensions, EMI requirements (shielded or open inductor) and the price. Examples of suitable inductors from various manufacturers are shown in the table below.

Table 1. Calculated Inductor Values

Calculated coils, I ripple peak−peak 20%					
	f [kHz]	**200**	**350**	**500**	**750**
	I_{out} [A]				
12 V_{in} to 7.5 V_{out}	1 A	70 μH	40 μH	28 μH	18.7 μH
	2 A	36 μH	20 μH	14 μH	10 μH
12 V_{in} to 5 V_{out}	1 A	73 μH	42 μH	29 μH	20 μH
	2 A	36 μH	20 μH	15 μH	10 μH
12 V_{in} to 3.3 V_{out}	1 A	60 μH	34 μH	24 μH	16 μH
	2 A	30 μH	17 μH	12 μH	8 μH
5 V_{in} to 3.3 V_{out}	1 A	28 μH	16 μH	11.2 μH	7.5 μH
	2 A	14 μH	8 μH	5.6 μH	3.7 μH
5 V_{in} to 2.5 V_{out}	1 A	31 μH	18 μH	12.5 μH	8.3 μH
	2 A	16 μH	9 μH	6.3 μH	4 μH
5 V_{in} to 1.8 V_{out}	1 A	29 μH	16.5 μH	11.5 μH	7.7 μH
	2 A	15 μH	8.2 μH	5.8 μH	3.8 μH

Table 2. Inductor Examples

L [μH]	Part Number	Shielded/ Non−shielded	I_{rms} [A]	DCR max [mΩ}	Manufacturer	Web
33	DO3316P−333	N	2.1	100	Coilcraft	www.coilcraft.com
	MSS1038−333	S	2.3	93	Coilcraft	www.coilcraft.com
	PF0698.333NL	N	2.8	65	PULSE	www.pulseeng.com
	PF0560.333NL	S	2.2	93	PULSE	www.pulseeng.com
22	DO3340P−223	N	2.5	66	Coilcraft	www.coilcraft.com
	MSS1038−223	S	2.85	73	Coilcraft	www.coilcraft.com
	PG0015.223NL	N	1.95	100	PULSE	www.pulseeng.com
	PF0560.223NL	S	2.5	73	PULSE	www.pulseeng.com
15	DO3316P−153	N	3.1	46	Coilcraft	www.coilcraft.com
	MSS1246T−153	S	3.4	56	Coilcraft	www.coilcraft.com
	PG0015.153NL	N	2.27	80	PULSE	www.pulseeng.com
10	DS3316P−103	S	2	101	Coilcraft	www.coilcraft.com
	DO3308P−103	N	2.3	85	Coilcraft	www.coilcraft.com
	P0762.103NL	N	2	110	PULSE	www.pulseeng.com
	P1167.103NL	S	2	50	PULSE	www.pulseeng.com
8.2	DS3316P−822	S	2.1	85	Coilcraft	www.coilcraft.com
	MSS6132−822	S	2.65	70	Coilcraft	www.coilcraft.com
5.6	MSS6132−562	S	2.95	60	Coilcraft	www.coilcraft.com
5.4	P1167.542NL	S	2.5	33	PULSE	www.pulseeng.com
5.2	PA0390.472NL	N	2.2	54.4	PULSE	www.pulseeng.com
3.9	DO3316T−392	N	5.3	15	Coilcraft	www.coilcraft.com
3.8	PA0390.332NL	N	2.9	42.8	PULSE	www.pulseeng.com

Output Rectifier Diode

When the high−side switch is on, energy is stored in the magnetic field in the inductor. During off time, the internal MOSFET switch is off. Since the current in the inductor has to discharge, the current flows through the rectifying diode to the output. A Schottky diode is recommended due to low diode forward voltage and very short recovery times, which positively impacts the step down voltage converter's overall efficiency. Another choice could be fast recovery or ultra−fast recovery diodes. It should be noted that some types of these diodes with an abrupt turn−off characteristic may cause instability or EMI troubles.

The peak reverse voltage is equal to the maximum input voltage. The peak conducting current is clamped by the current limit of the NCP3120. Use of Schottky barrier diodes reduces diode reverse recovery input current spikes. For switching regulators operating at low duty cycles, it is beneficial to use rectifying diodes with somewhat higher RMS current ratings (thus lower forward voltages). This is because the diode conduction interval is much longer than that of the transistor. Converter efficiency will be improved if the voltage drop across the diode is lower. The average current can be calculated from:

$$I_{D(AVG)} = \frac{I_{LOAD}(V_{IN} - V_{OUT})}{V_{IN}}$$

Table 3. Schottky Diode Example

Part Number	Description	V_{RRM} min [V]	V_F max [V]	$I_{O(rec)}$ max [A]	Package	Web
MBRS2040LT3G	2 A, 40 V Low V_f Schottky Rectifier	40	0.43	2	SMB	www.onsemi.com
MBRS230LT3G	2 A, 30 V Low V_f Schottky Rectifier	30	0.49	2	SMB	www.onsemi.com
MBRS240LT3G	2 A, 40 V Low V_f Schottky Rectifier	40	0.43	2	SMB	www.onsemi.com
SS24T3G	2 A, 40 V Schottky Rectifier	40	0.5	2	SMB	www.onsemi.com
MBRA340T3G	3 A, 40 V Schottky Rectifier	40	0.45	3	SMA	www.onsemi.com
MBRS330T3G	3 A, 30 V Schottky Rectifier	30	0.5	3	SMC	www.onsemi.com

The worst case of the diode average current occurs during maximum load current and maximum input voltage. The rectifying diodes should be placed close to the SW pin to avoid the possibility of ringing due to trace inductance.

Input Capacitor

The input current to the step down converter is discontinuous. The input capacitor has to maintain the DC input voltage and to sustain the ripple current produced by internal MOSFET switching. For stable operation of the switch mode converter, a low ESR capacitor is needed to prevent large voltage transients from appearing at the input. Therefore, ceramic capacitors are preferred, but the circuit works in a stable manner also with electrolytic capacitors. It must be located near the regulator and use short leads. Also, paralleling ceramic capacitors will increase the regulator stability.

The RMS value of the input capacitor current ripple is:

$$I_{RMS} = I_{LOAD}\sqrt{D(1 - D)}$$

The duty cycle is:

$$D = \frac{V_{OUT} + V_D}{V_{IN} + V_D - V_{DSAT}}$$

where:

V_D is the voltage drop across the rectifying diode and

V_{DSAT} is the switch saturation voltage on the power MOSFET.

The equation reaches its maximum value with duty cycle = 0.5, where:

$$I_{RMS} = \frac{I_{LOAD}}{2}$$

Losses in the input capacitor can be calculated using the following equation:

$$P_{CIN} = I_{RMS}^2 \cdot ESR_{CIN}$$

where:

ESR_{CIN} is the effective series resistance of the input capacitance.

The input capacitor voltage ripple depends on the C_{IN} capacitor value. Therefore, the input capacitor can be estimated by:

$$C_{IN} = \frac{I_{LOAD}}{f_{SW} \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Output Capacitor

The output capacitor filters output inductor ripple current and provides low impedance for load current changes. The principle consideration for the output capacitor is the ripple current induced by the switches through the inductor. It supplies the current to the load in DCM or during load transient and filters the output voltage ripple. For low output ripple voltage and good stability, low ESR output capacitors are recommended. The inductor ripple current acting against the ESR of the output capacitor is the major contributor to the output ripple voltage.

An output capacitor has two main functions: it filters the output and provides regulator loop stability.

The ESR of the output capacitor and the peak−to−peak value of the inductor ripple current are the main factors contributing to the output ripple voltage value.

The output voltage ripple is given by the following equation:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(ESR + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right)$$

where:

ESR is the equivalent series resistance of the output capacitor.

The output capacitor value can by expressed by:

$$C_{OUT} = \frac{\Delta I_L}{8 \cdot f_{SW} \cdot (\Delta V_{OUT} - \Delta I_L \cdot ESR)}$$

These components must be selected and placed carefully to yield optimal results. Key specifications for output capacitors are their ESR (equivalent series resistance) and ESL (equivalent series inductance) values. For best transient response, a combination of low value/high frequency and bulk capacitors placed close to the load will be required.

For most applications, a 22 μF ceramic capacitor should be sufficient. X5R or X7R dielectrics ceramic capacitors are recommended.

Soft−Start Capacitor Selection

The soft−start time is programmed by an external capacitor connected from the SS pin to AGND, which can be calculated by:

$$C_{SS} \approx \frac{t_{SS} \cdot 8.75\ \mu A}{0.8\ V}$$

where:

− t_{SS} is the soft−start/stop interval.

Note: See the “Sequencing and Tracking” section on how to use this capacitor.

Output Voltage Programming

The controller will maintain 0.8 V at the feedback pin. Thus, if a resistor divider circuit is placed across the feedback pin to V_{OUT}, the controller will regulate the output voltage in proportion to the resistor divider network in order to maintain 0.8 V at the FB pin.

Table 4. Output Voltage Setting

V_{OUT} [V]	8	7.5	6	5	4	3.3	2.5	1.8	1.2
R_1 [kΩ]	180	360	130	68	300	47	51	20	10
R_2 [kΩ]	20	43	20	13	75	15	24	16	20

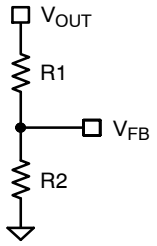


Figure 35. Feedback divider

The relationship between the resistor divider network and the output voltage is shown in the following equation:

$$R_2 = R_1\left(\frac{V_{REF}}{V_{OUT} - V_{REF}}\right)$$

where:

V_{REF} is the circuit's internal voltage reference, which equals 0.8 V.

Resistor R1 is selected based on a design trade−off between efficiency and output voltage accuracy. For high values of R1, there is less current consumption in the feedback network. However, the trade−off is output voltage accuracy due to the bias current in the error amplifier. Once R1 has been determined, R2 can be calculated.

Selecting the Switching Frequency

Selecting the switching frequency is a trade−off between component size and power losses. Operation at higher switching frequencies allows the use of smaller inductor and capacitor values. Nevertheless, it is common to select lower frequency operation because a higher frequency results in lower efficiency due to MOSFET gate charge losses. Additionally, the use of smaller inductors at higher frequencies results in higher ripple current, higher output voltage ripple, and lower efficiency at light load currents. The value of the oscillator resistor is designed to be linearly related to the switching period. There are two ways to determine the RT resistor value: by using the standard curve shown in Figure 36 or by using Table 5. The frequency on the RT pin will set the master oscillator. The actual operating frequency on each channel will be one−half the master oscillator.

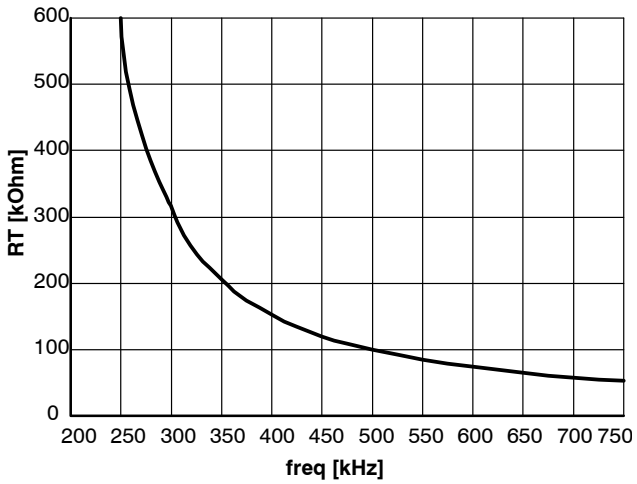


Figure 36. Switching Frequency Selection

Table 5. Switching Frequency Selection

Freq. [kHz]	200	250	300	350	400	450	500	550	600	650	700	750
RT [kΩ]	open	649	316	205	154	121	100	84.5	73.2	64.9	57.6	52.3

Sequencing of Output Voltages

Some microprocessors and DSP chips need two power supplies with different voltage levels. These systems often require voltage sequencing between the core power supply and the I/O power supply. Without proper sequencing, latch−up failure or excessive current draw may occur that could result in damage to the processor's I/O ports or the I/O ports of a supporting system device such as memory, an FPGA or a data converter. To ensure that the I/O loads are not driven until the core voltage is properly biased, tracking of the core supply and the I/O supply voltage is necessary.

Designing a system without proper power supply sequencing for signal processing devices like DSPs, FPGAs, and PLDs may create risks as to reliability or proper functionality. The risk comes when there are active and inactive power supply rails on the device for a long time. During this time, the ESD structures, internal circuits and components are stressed from interference between different voltages (from the two separate power supply rails). When these conditions persist on multi−supply devices for long time periods (this is a cumulative phenomenon), the life of the products (DSP, FPGA, and PLD devices) is drastically reduced. The failure is often a result of high currents flowing to the pins or the high voltage difference between pins.

In that case, the signal processors require multiple power supplies generating different voltage levels for core and I/O peripherals over time. NCP3120 offers ratiometric sequencing, sequential sequencing and tracking sections to manage the output voltages behavior during start−up and power−down. Basically, the DSP, FPGA, and PLD manufacturers do not specify the method of power sequencing, but they do specify restrictions on the time or voltage differences during power−up and power−down. The power−up sequence for microprocessors should be finished approximately within a few seconds to prevent the risks mentioned above. For more information, see the microprocessor manufacturers' datasheets.

Ratiometric Sequencing

In the ratiometric sequencing mode, multiple outputs start ramping at the same time and also reach the regulation level at the same time. When common EN is pulled down, the output voltages are going down at the same time. See Figure 37. This functionality is created by using the same capacitor values as the soft−start capacitors for all outputs and by connecting all EN + SEQ pins together. To ensure this behavior, the soft start capacitors should have values greater than the time constant of the output inductor and output capacitor.

For proper operation in this mode, using a common soft−start capacitor for both channels is not recommended.

Note: If enable control is not required, float the EN/SEQ connections rather than pulling them to VIN or a separate supply voltage. The NCP3120 will enable itself once VIN crosses the input UVLO threshold.

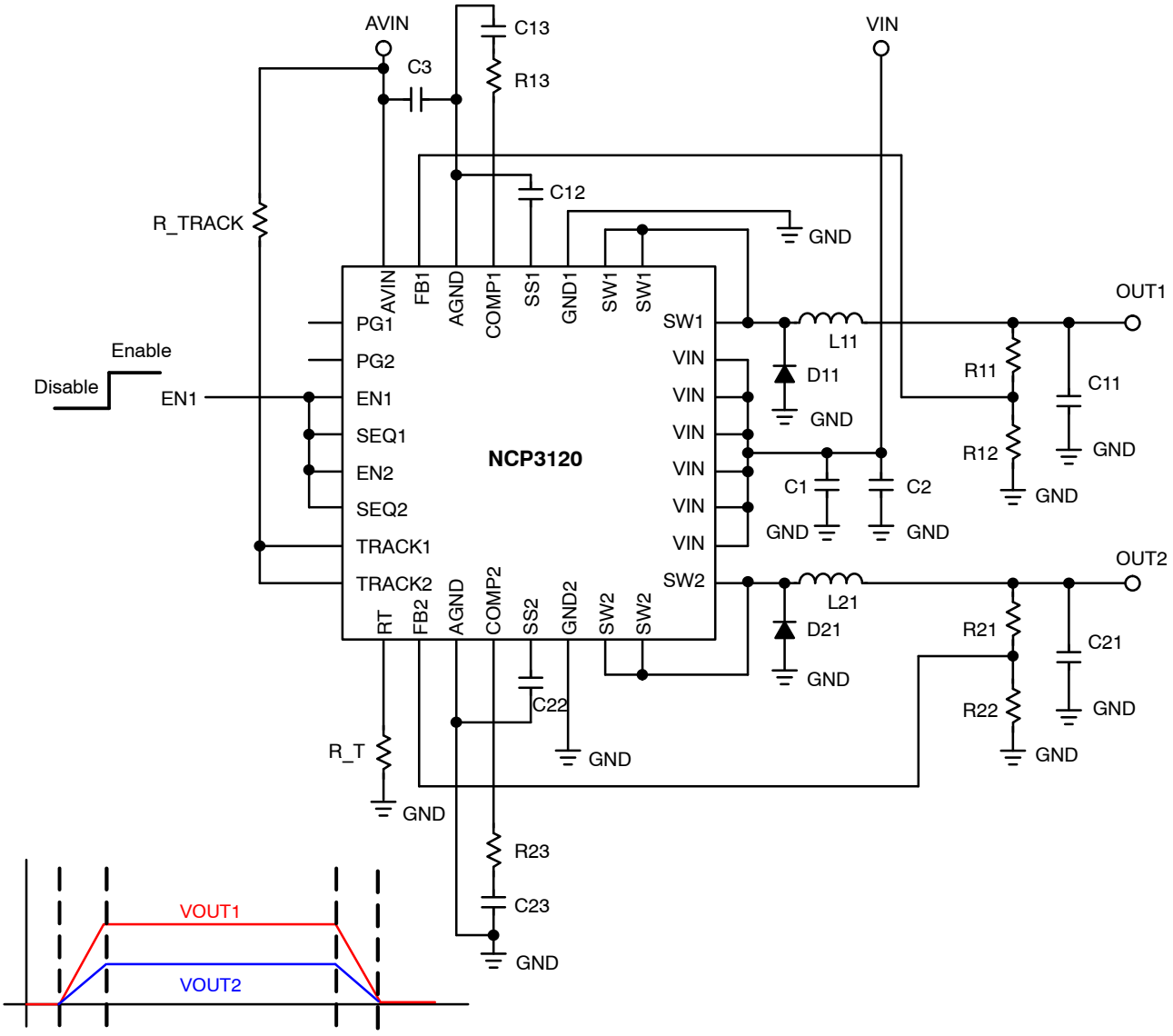


Figure 37. Ratiometric Sequencing Configuration

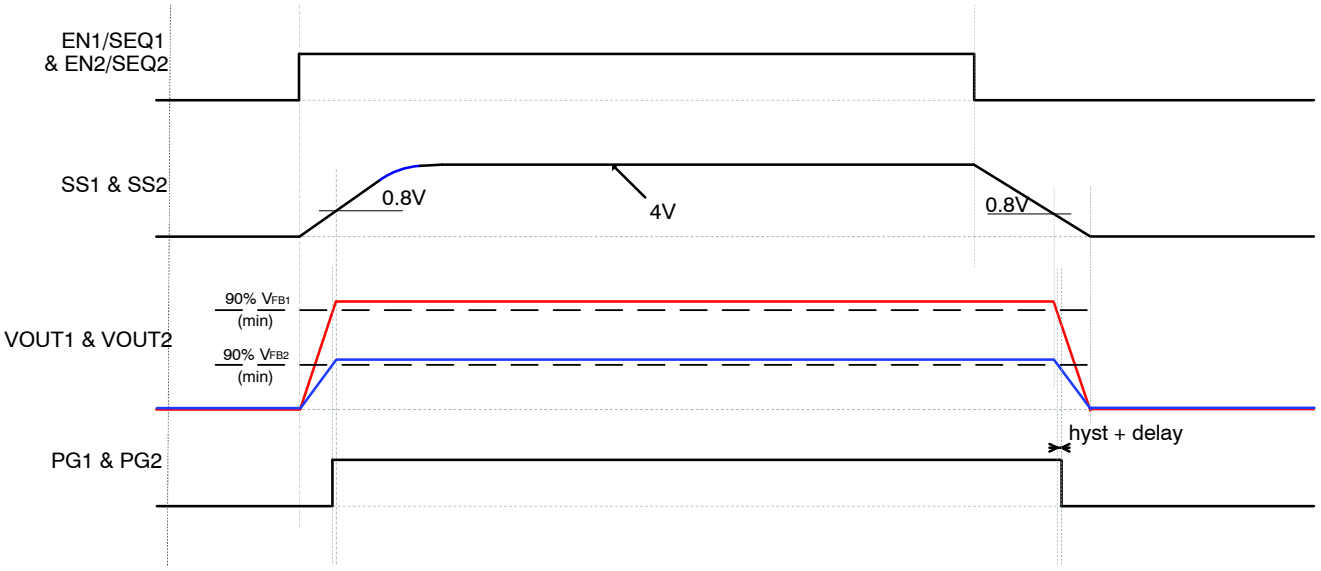


Figure 38. Typical Behavior of Ratiometric Sequencing Mode

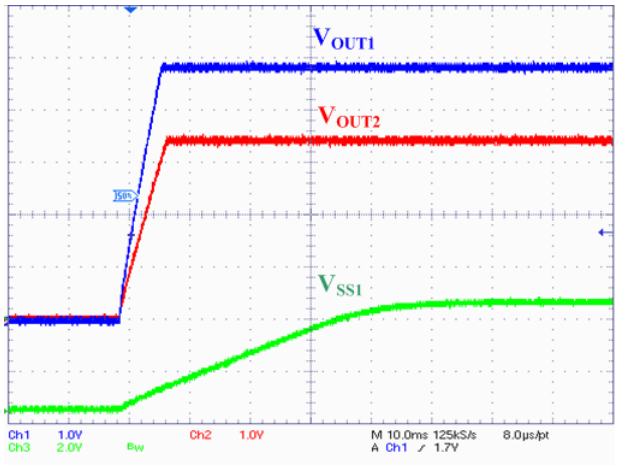


Figure 39. Ratiometric Mode − Power−up

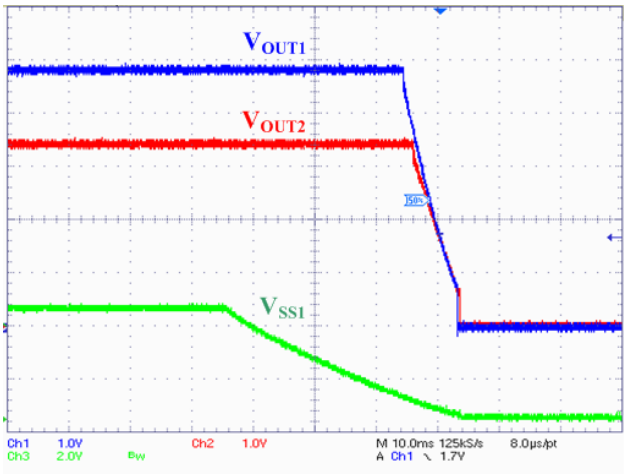


Figure 40. Ratiometric Mode − Power−down

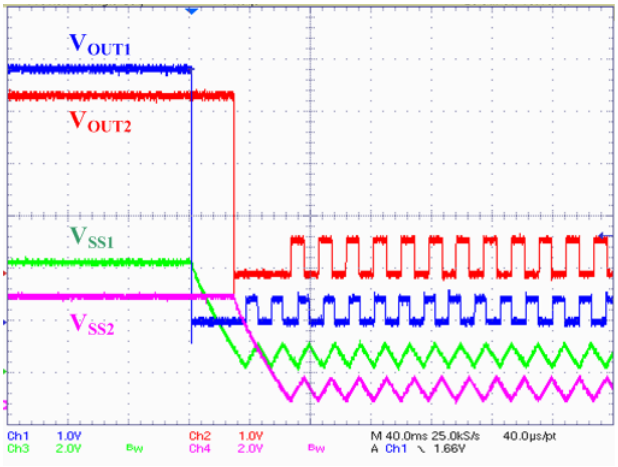


Figure 41. Ratiometric Mode − Start of OLM

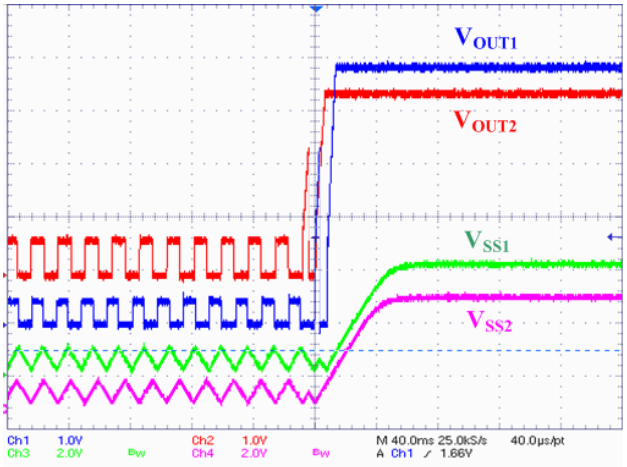


Figure 42. Ratiometric Mode − End of OLM

Sequential Sequencing (First−Up/Last−Down Sequence Configuration)

In sequential sequencing mode, the second output voltage starts ramping when the first output voltage is already settled and its power good signal is set. Figure 43 shows the NCP3120's configuration and standard waveforms. The rising slope of both voltages can be selected independently by the soft−start capacitors' values (C12, C22). When the enable pin is deactivated, the second output voltage decreases first, followed by the first output voltage. The control logic is based on the internal power good signal; no delay is added. The signal has the same threshold values as the power good signal shown in the electrical table. The sequential sequencing mode is also called first−up/last−down and is ideal for DSPs with separate power supplies for the core and the I/O ports.

Note: If enable control is not required, float the EN(first)/SEQ(last) connection rather than pulling it to VIN or a separate supply voltage. For Figure 43 this is EN1/SEQ1. For Figure 44, this is EN1/SEQ4. The NCP3120 will enable itself once VIN crosses the input UVLO threshold.

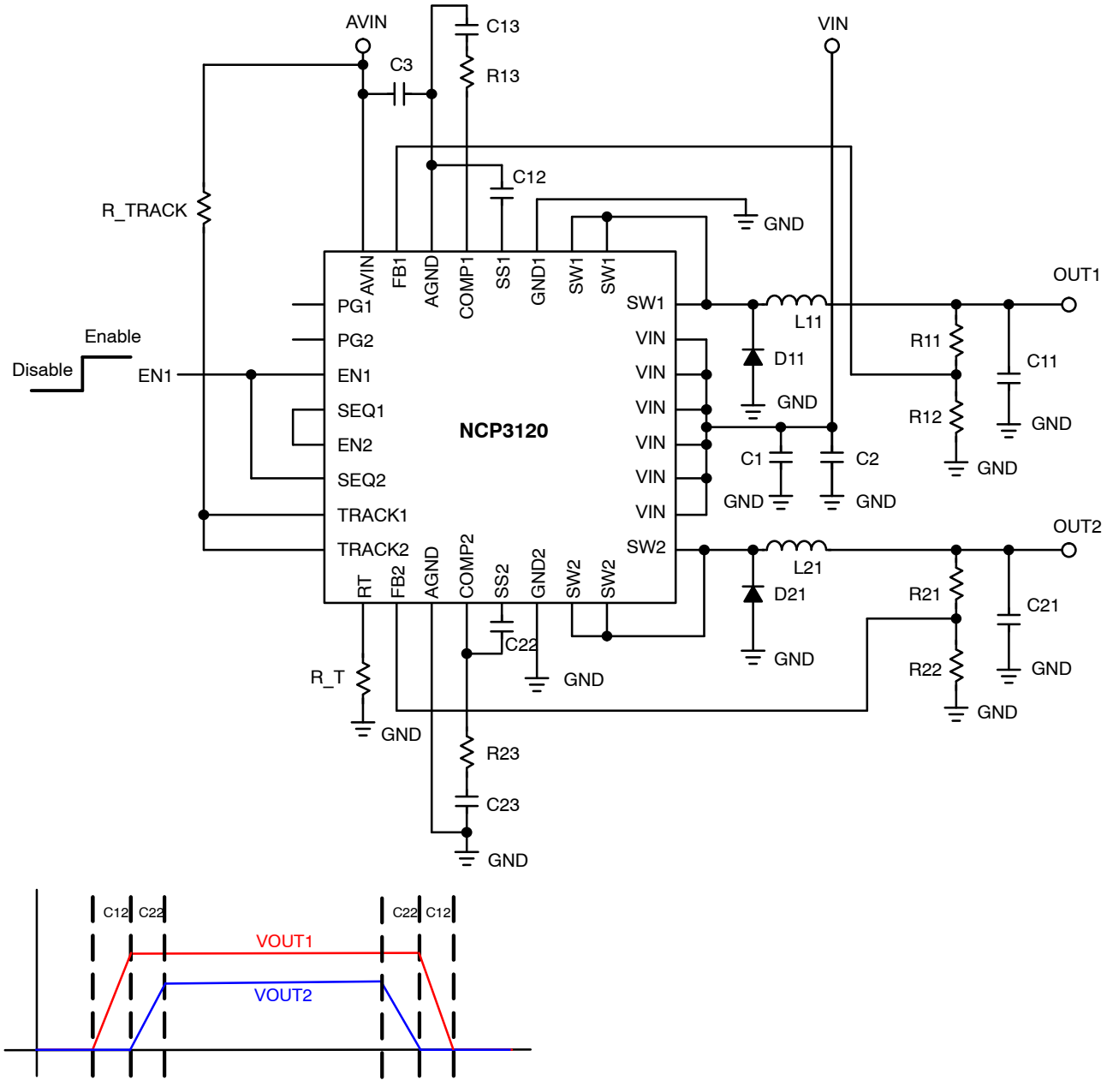


Figure 43. Sequential Configuration

Daisy Chain Operation

The last−up/first−down power output has its SEQ pin tied to the EN of the first−up/last−down power output. Each output in the chain has its power−up delay set by the soft−start ramp−up of the supply. This feeds its EN and its power−down delay set by the soft−start ramp−down of the supply that feeds its SEQ pin.

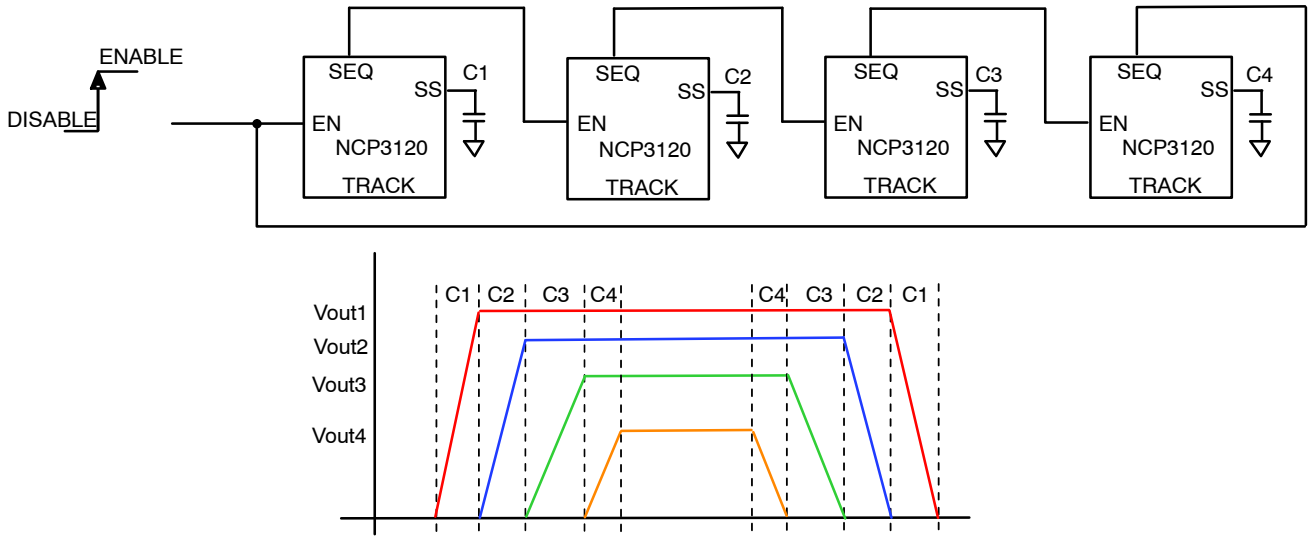


Figure 44. Simplified Drawing of Daisy−chained NCP3120's

When the first voltage rail has reached a specific voltage level, the next voltage rail is enabled and its rise is monitored until it has reached the power good trip point. At this point, the next voltage rail is enabled. This continues until all voltage rails have been enabled (see Figure 45). Power−down sequencing is just the opposite of the power−up sequence.

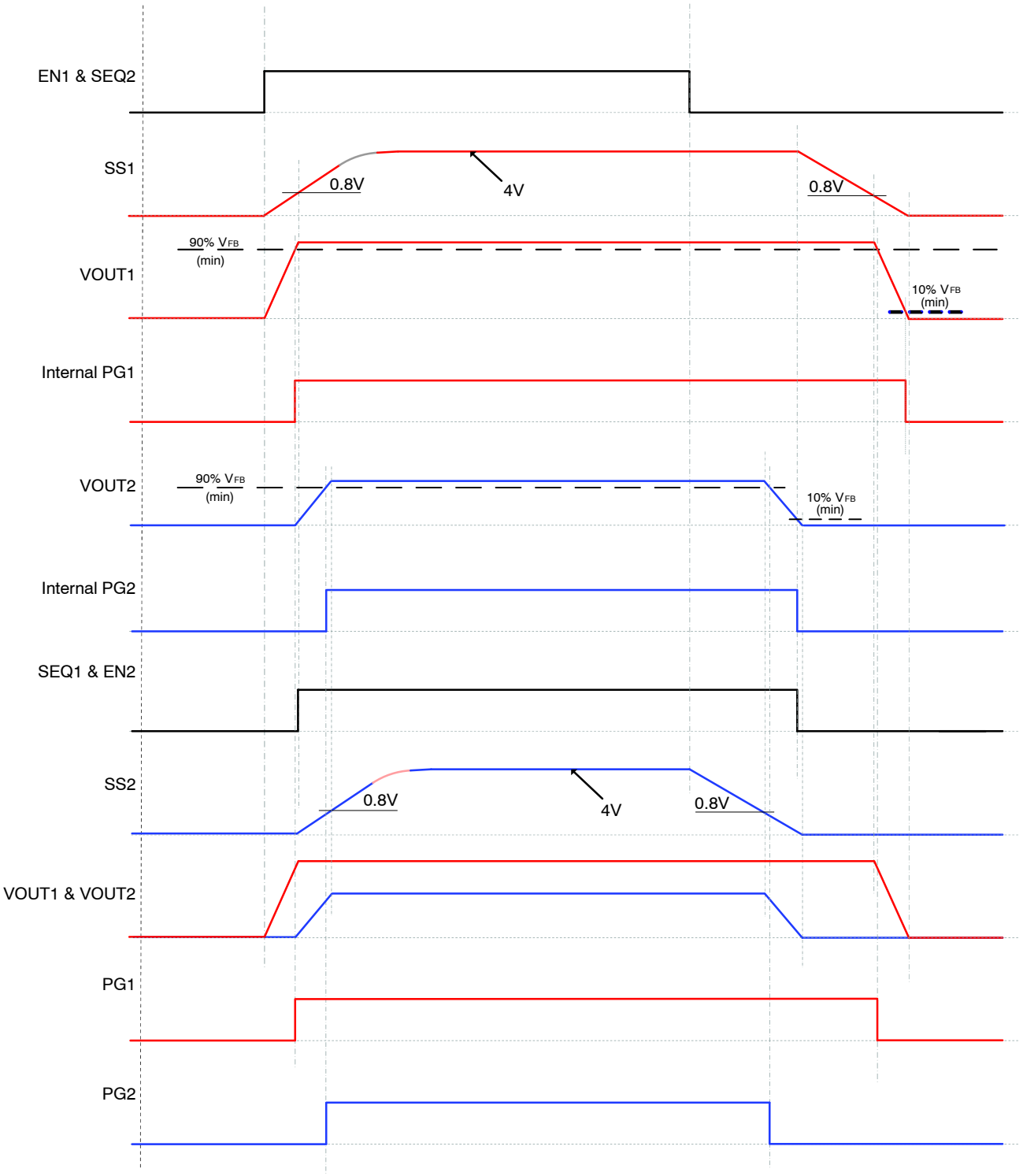


Figure 45. Typical Behavior of Sequential Mode

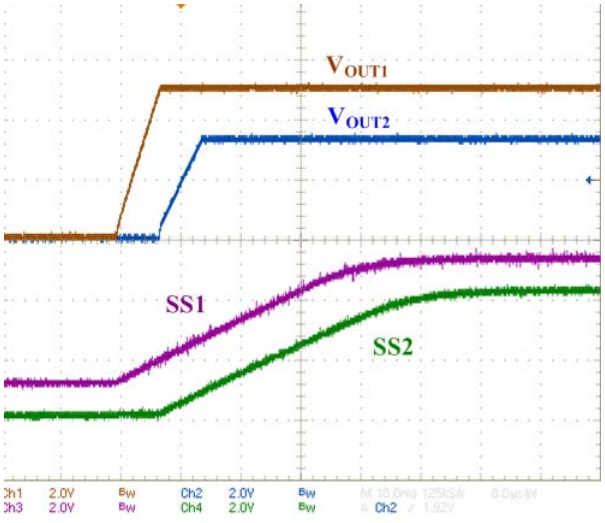


Figure 46. Sequential Mode − Power−up

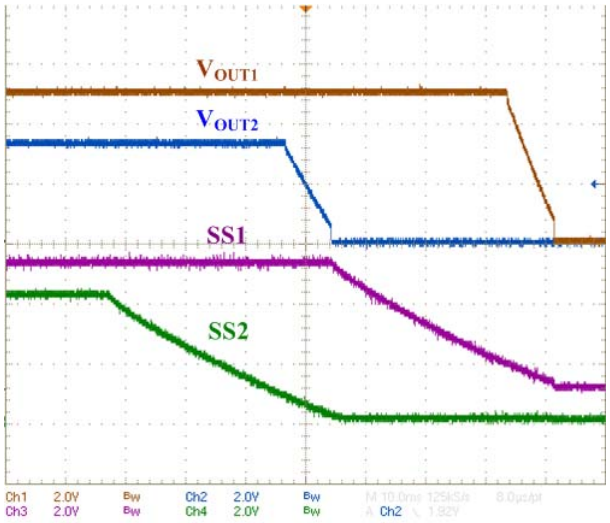


Figure 47. Sequential Mode − Power−down

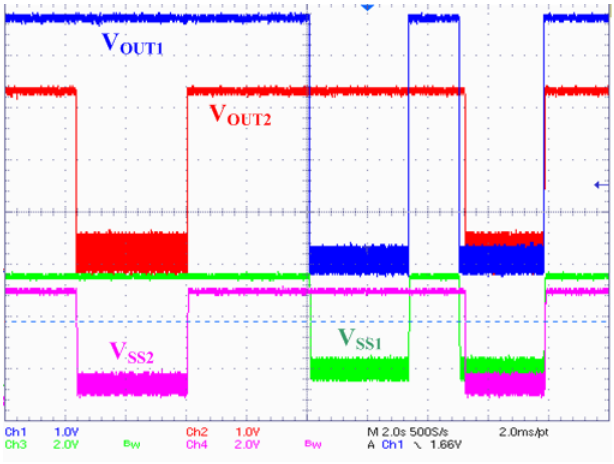


Figure 48. Sequential Mode − Power−down

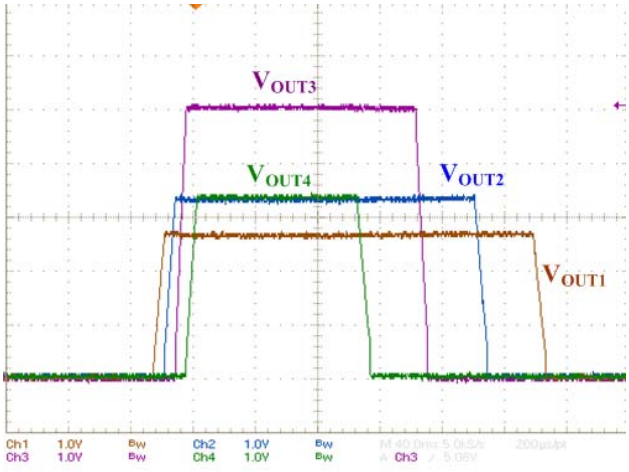


Figure 49. Daisy Chain of Four Outputs

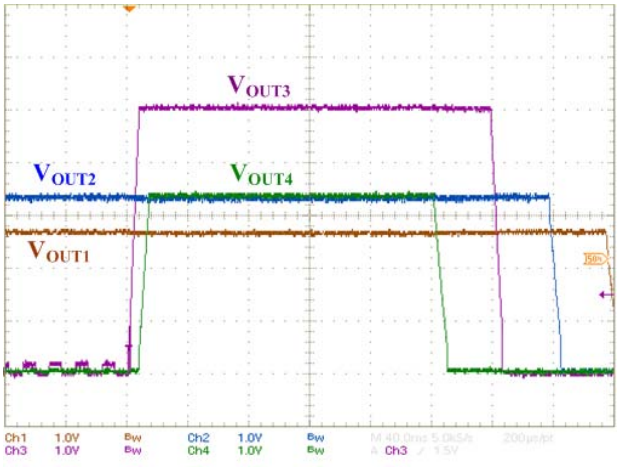


Figure 50. OLM of the 3rd Output in Daisy Chain

Tracking

Voltage tracking is enabled by applying a ramp voltage to the TRACK pin. When the voltage on the TRACK pin is below 0.8 V, the feedback voltage will regulate to this tracking voltage. When the tracking voltage exceeds 0.8 V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage.

In this start−up sequence, the tracking pin is used to match the output voltage ramps exactly. Higher output voltage will continue to rise past the lower regulated point. This is achieved by dividing the higher output voltage by the same ratio as the lower voltage feedback components and connecting the divided voltage into the TRACK pin of the lower voltage. Track pins must be tied high in the normal operation (except in the tracking mode).

The output voltage during tracking can be calculated with the following equation:

$$V_{OUT} = V_{TRACK}\left(1 + \frac{R5}{R6}\right) \qquad V_{TRACK} < 0.8\ V$$

Note: If enable control is not required, float the EN/SEQ connections rather than pulling them to VIN or a separate supply voltage. The NCP3120 will enable itself once VIN crosses the input UVLO threshold.

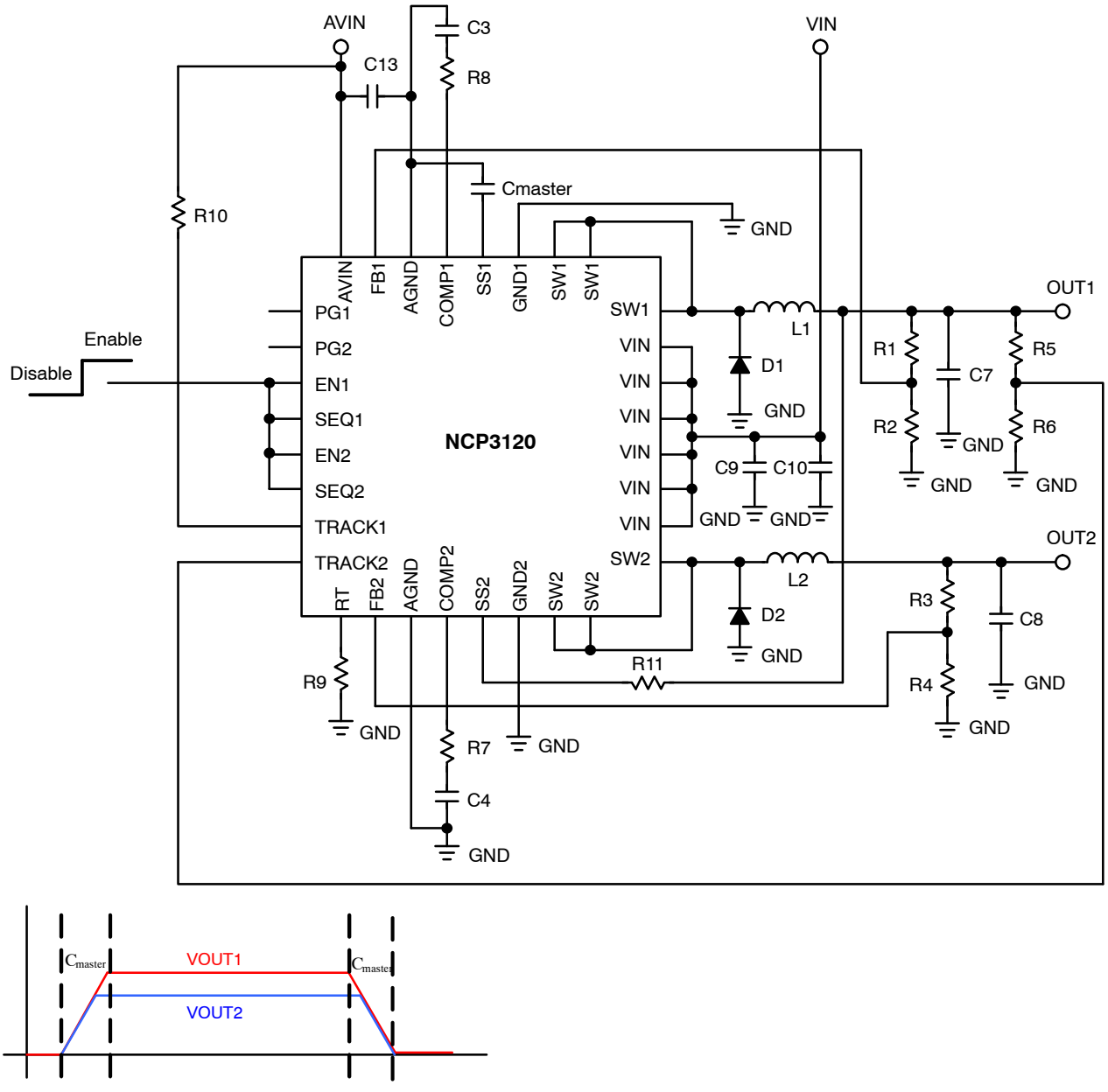


Figure 51. Tracking Configuration

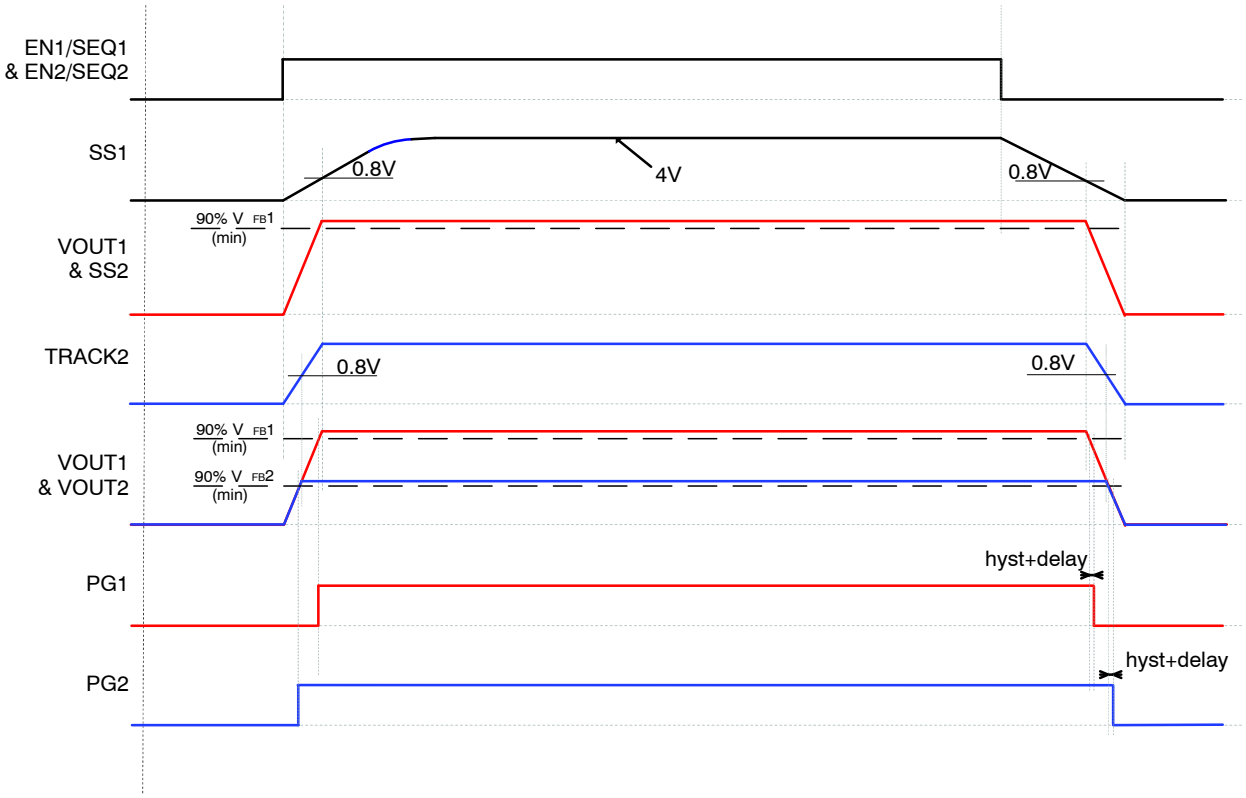


Figure 52. Typical Behavior of Tracking Configuration

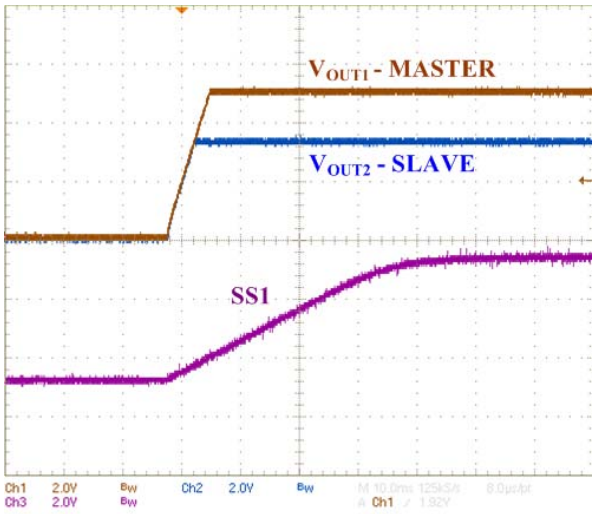


Figure 53. Tracking Mode – Power−up

Figure 54. Tracking Mode – Power−down

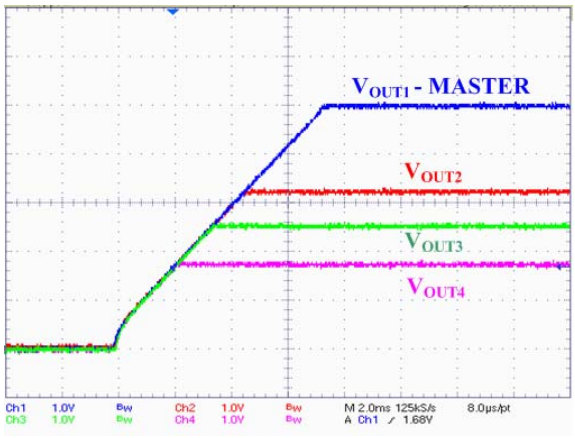


Figure 55. Tracking Mode of Four Outputs – Power−up

Figure 56. Tracking Mode of Four Outputs – Power−down

When hiccup overload mode is detected on the slave channel only, the output voltage of the 2nd channel (slave) decreases. After the overload condition ends, the slave channel voltage remains low. If the slave channel should rise when the OLM disappears, the configuration of the enable and soft−start pins shown in Figure 57 must be used.

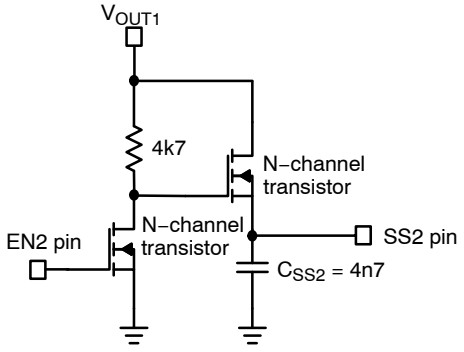


Figure 57. Augmented OLM in Tracking Mode

For proper operation of the modified tracking mode, use an SS1 capacitor with a value at least 10 times higher than that of the SS2 capacitor.

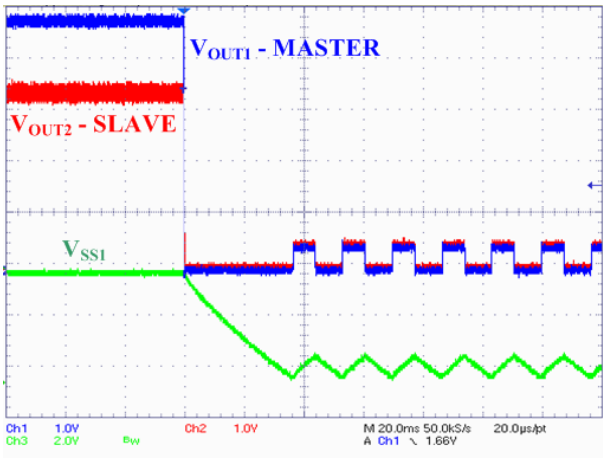


Figure 58. Master Voltage – Start of OLM

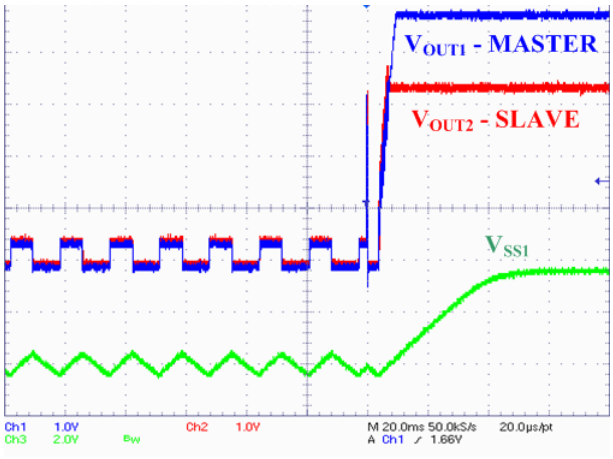


Figure 59. Master Voltage – End of OLM

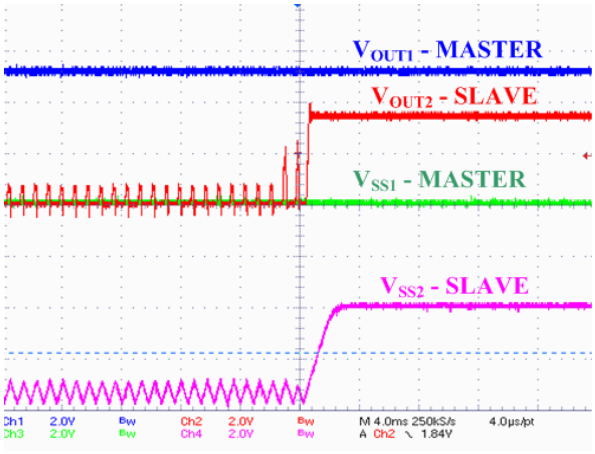


Figure 60. Master Voltage – Start of Augmented OLM

Figure 61. Master Voltage – End of Augmented OLM

Note: If the overload conditions are detected on the master channel only or on both channels together (master + slave), both output voltages increase when the overload conditions are released.

Mixed Mode A (Sequencing and Tracking)

The different modes can also be used together to achieve various combinations of power sequencing. Mixed mode A demonstrates the configuration of tracking and sequencing for four outputs. The schematic and typical output behavior is shown in Figure 62. Mixed mode B shows the combination of tracking, sequencing and normal mode.

Note: As in the previous, and all subsequent examples, if enable control is not required, float the EN/SEQ control connection rather than pulling it to VIN or a separate supply voltage. The NCP3120 will enable itself once VIN crosses the input UVLO threshold.

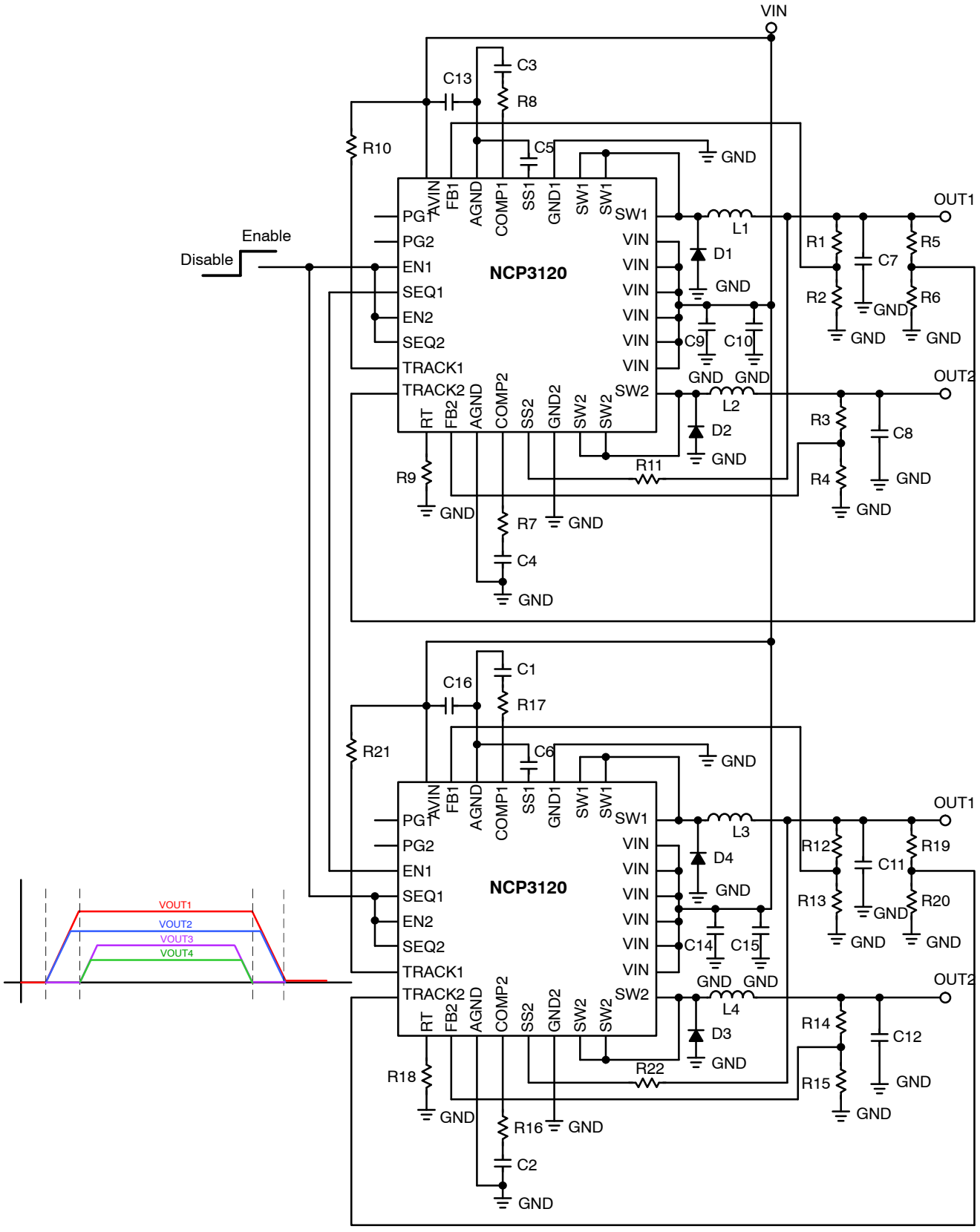


Figure 62. Mixed Mode, Configuration A

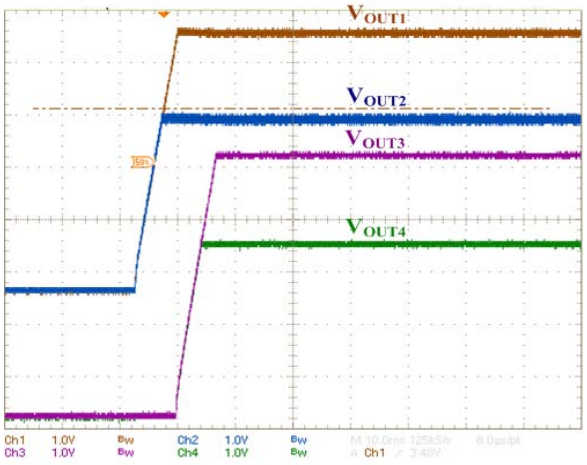


Figure 63. Mixed Mode of Four Outputs – Power−up

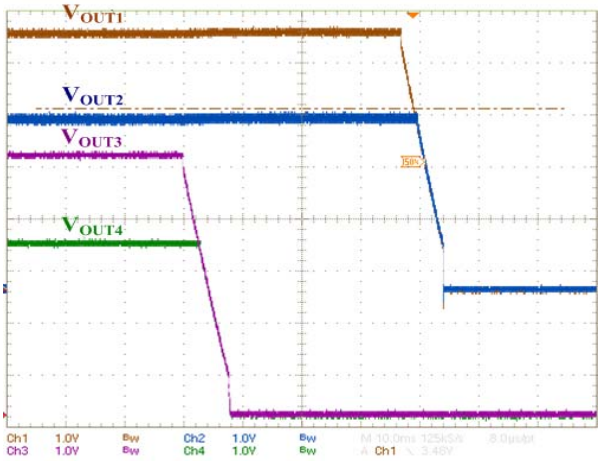


Figure 64. Mixed Mode of Four Outputs – Power−down

Mixed Mode B (Normal & Sequencing & Tracking)

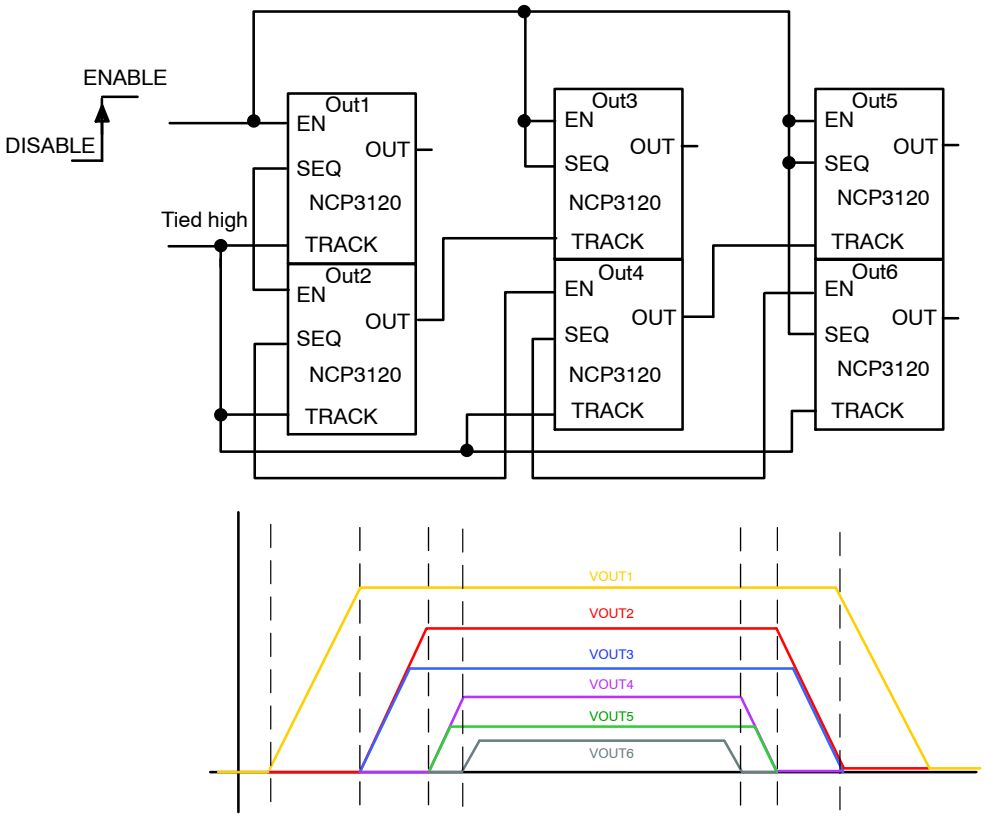


Figure 65. Mixed Mode, Configuration B

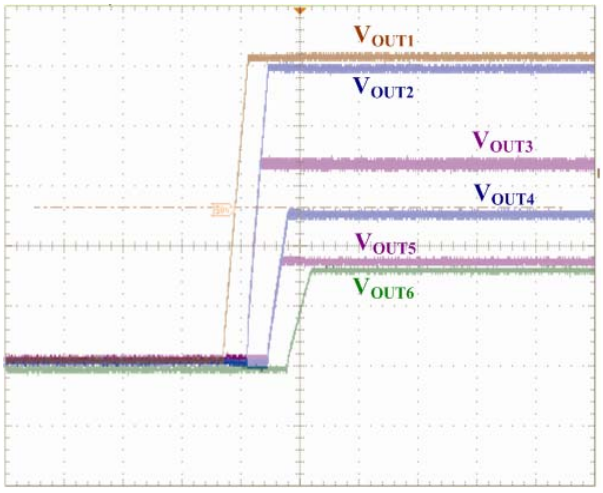


Figure 66. Mixed Mode of Six Outputs – Power−up

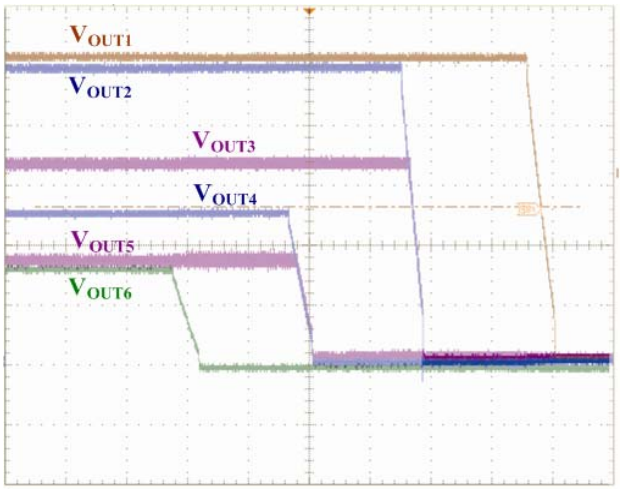


Figure 67. Mixed Mode of Six Outputs – Power−down

Normal Operation (No Tracking, No Sequencing)

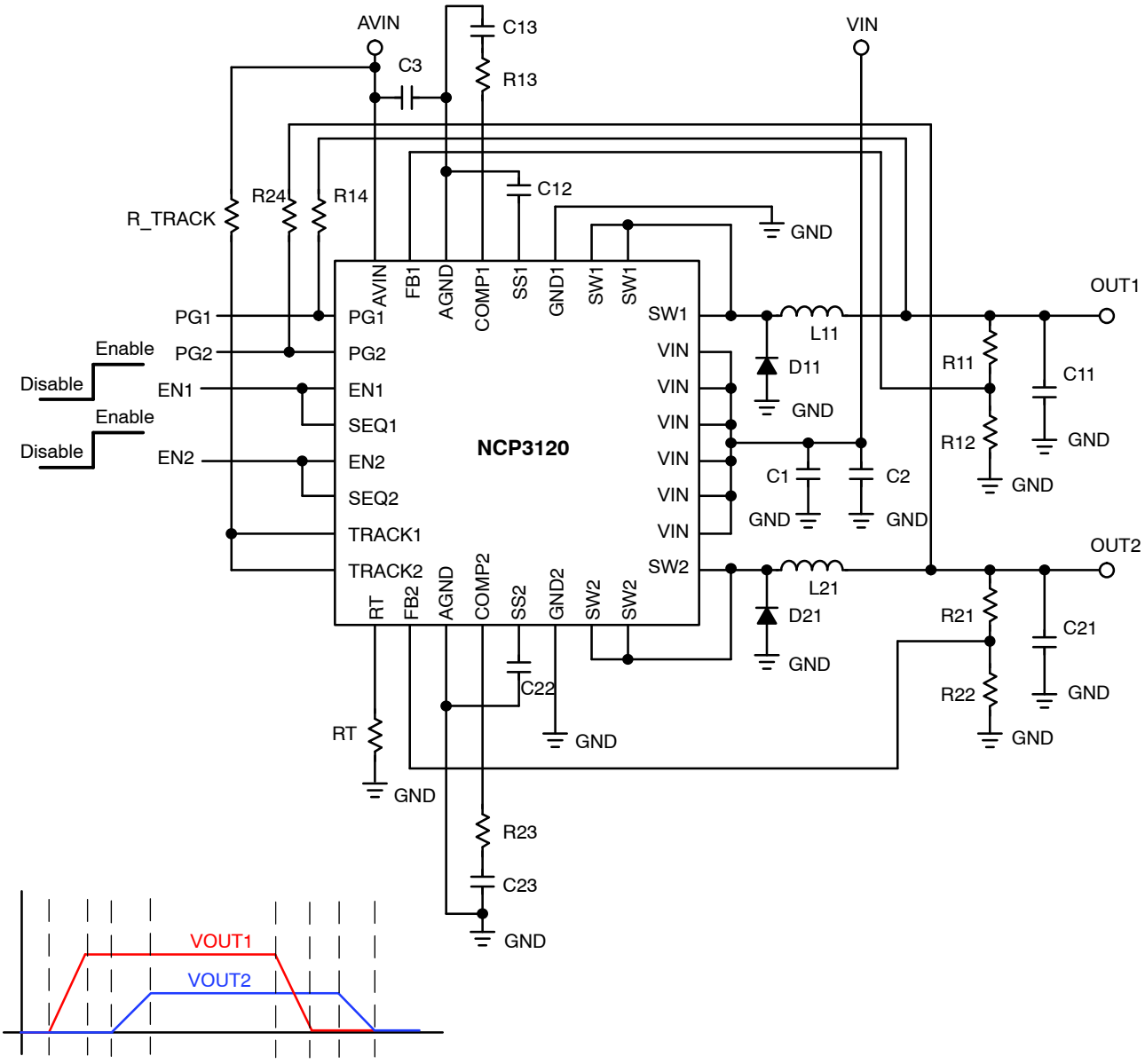


Figure 68. Normal Operation Configuration

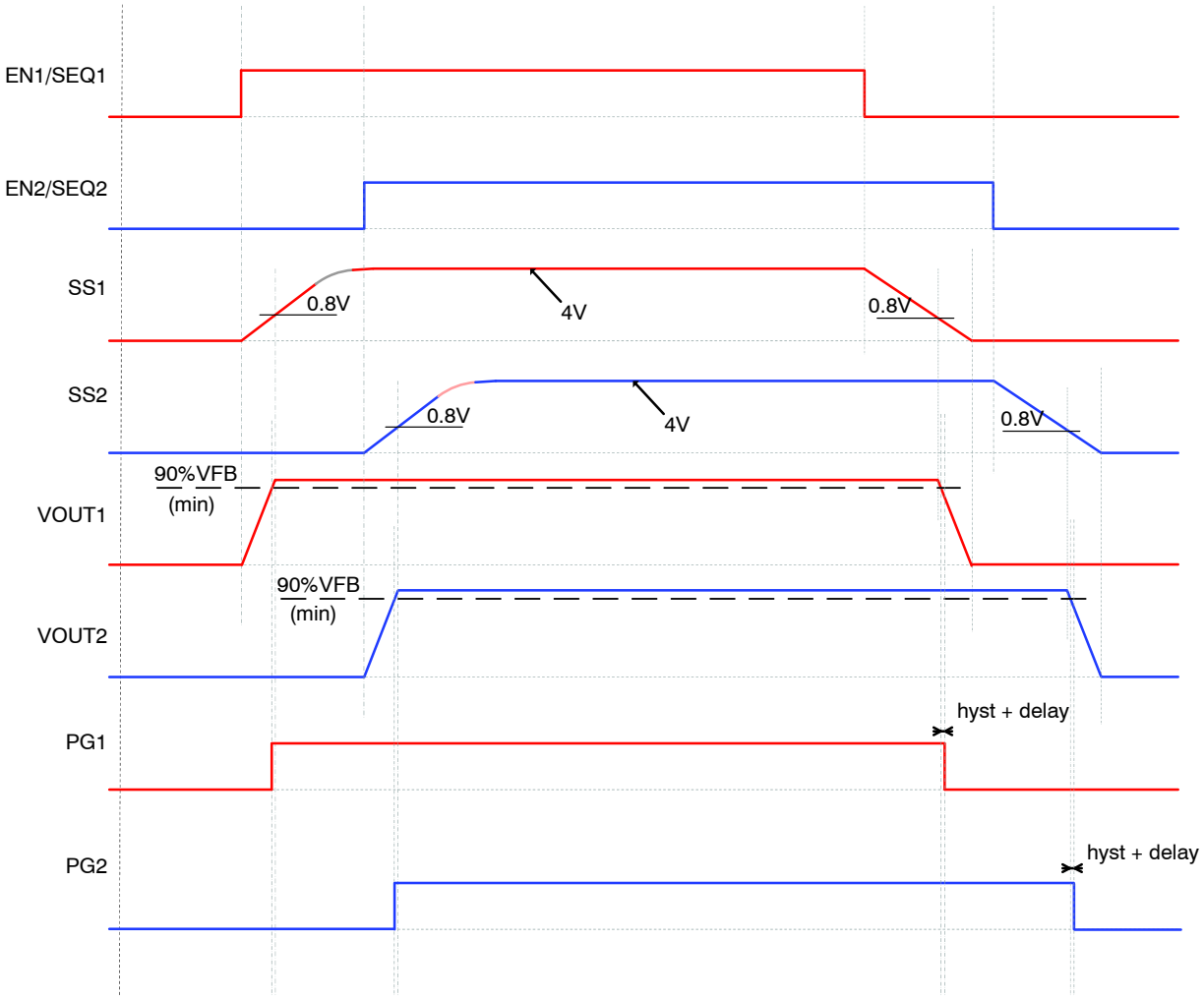


Figure 69. Typical Application Behavior

Parallel Operation

Parallel operation of NCP3120 circuit(s) has several advantages. One of the most important aspects is the capability to deliver a double output current. The major advantage is a reduced output voltage ripple in case of out−of−phase synchronization. The standard configuration is shown in Figure 70.

OLM in Parallel Operation

When OLM is detected (e.g., a jump from 4 A on the output to 6 A), the output voltage decreases. When OLM wears off, the output current must be decreased below 3 A. Then, the output voltage is released and current can be increased again − up to 4 A.

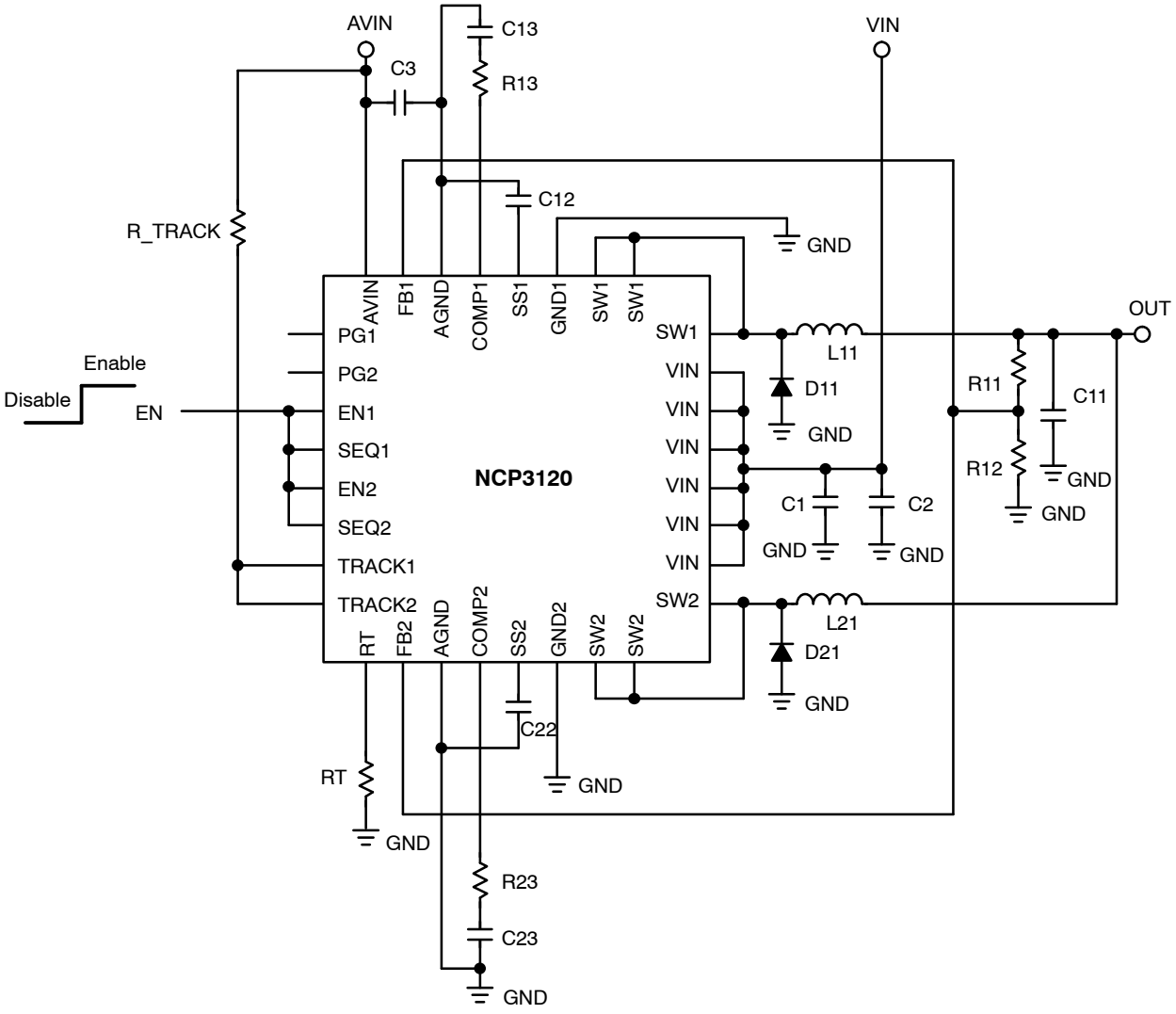


Figure 70. Parallel Operation Configuration.

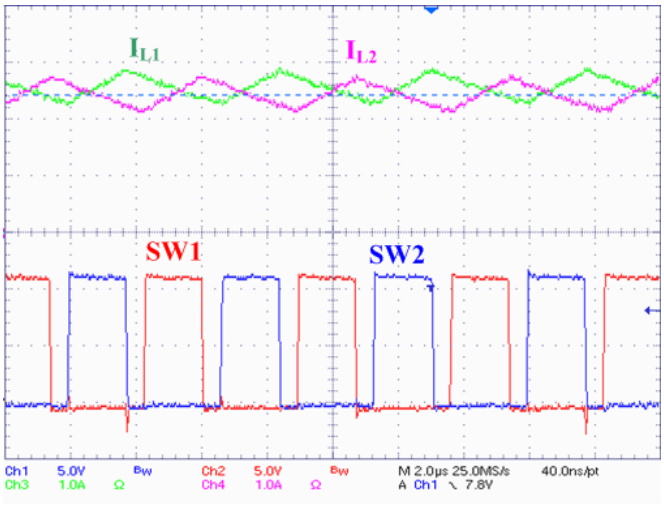


Figure 71. Parallel Operation of Both Outputs

Loop Compensation

A COMP pin of the transconductance error amplifier is used to compensate the regulation control system. Standard COMP pin values are shown in the BOM at the end of the datasheet. (See the COMPCALC program to determine customer preferred values.)

To design the compensation components for conditions not described in Table 6 and/or for tuning the compensation for specific requirements, the COMPCALC design tool is available from ON Semiconductor at no charge. Visit http://www.onsemi.com/pub/Collateral/COMPCALC.ZIP to download the self−extracting program for NCP3120 loop compensation design assistance. There is an Excel design tool for component selection. This design tool is available at http://www.onsemi.com/pub/Collateral/NCP312X%20DWS.XLS.

Table 6. Compensation Values Example for Typical Output Voltages

Vin [V]	Vout [V]	Freq [kHz]	Iout [A]	L11 [µH]	C11 − ceramic [µF]	C13 [nF]	R13 [kΩ]	C14 [pF]	R14 [Ω]	C15 [nF]
12	3.3	200	2	22	22	22	4.7	220	100	none
12	5	200	2	33	22	18	4.7	270	100	none
5	1.8	200	2	15	22	27	2.7	270	100	none

Thermal Considerations

The NCP3120 has thermal shutdown protection to safeguard the device from overheating when the die temperature exceeds 160°C. For the best thermal performance, wide copper traces and a generous amount of PCB printed circuit board copper should be used in the board layout. One exception to this is at the SW switching node, which should not have a large area in order to minimize the EMI radiation and other parasitic effects. Large areas of copper provide the best transfer of heat from the IC into the ambient air.

PCB Layout Guidelines

As in any switching regulator, the layout of the printed circuit board is very important. Rapidly switching currents associated with wiring inductance, stray capacitance and parasitic inductance of the printed circuit board traces can generate voltage transients that can generate electromagnetic interferences (EMI) and affect the desired operation. To minimize inductance and ground loops, the lengths of the leads indicated by heavy lines should be kept as short as possible. For best results, single−point grounding or ground plane construction should be used. On the other hand, the PCB area connected to the SW pin (drain of the internal switch) of the circuit should be kept to a minimum in order to minimize coupling to sensitive circuitry. Another sensitive part of the circuit is the feedback. It is important to keep the sensitive feedback wiring short. To ensure this, physically locate the programming resistors near the regulator.

There should be a ground area on the top layer directly under the IC with an exposed area for connecting the IC exposed pad. Any internal ground planes should be connected by vias to this ground area. Additional vias must be used at the ground side of the input and output capacitors. The GND pin also should be tied to the PCB ground in the area under the IC.

When laying out the buck regulator on a printed circuit board, the following checklist should be used to ensure proper operation of the circuit:

1. Rapid changes in voltage across parasitic capacitors and abrupt changes in current in parasitic inductors are major concerns for a good layout.
2. Keep high currents out of sensitive ground connections.
3. Avoid ground loops, as they pick up noise. Use star or single−point grounding.
4. For high power buck regulators on double−sided PCBs, a single ground plane (usually the bottom) is recommended.
5. Even though double−sided PCBs are usually sufficient for a good layout, four layer PCBs represent the optimum approach to reducing susceptibility to noise. Use the two internal layers as the power and GND planes, the top layer for power connections and component vias, and the bottom layer for noise sensitive traces.
6. Keep the inductor switching node small by placing the output inductor as close as possible to the chip.
7. Use fewer, but larger, output capacitors; keep the capacitors clustered; and use multiple layer traces with heavy copper to keep the parasitic resistance low.
8. Place the output capacitors as close to the output coil as possible.
9. Place the COMP capacitor as close as possible to the COMP pin.
10. Place the V_{IN} bypass capacitors as close as possible to the IC.
11. Place the RT resistor as close as possible to the RT pin.
12. The exposed pad must be connected to a ground plane with a large copper surface area to dissipate heat.

Layout Diagram

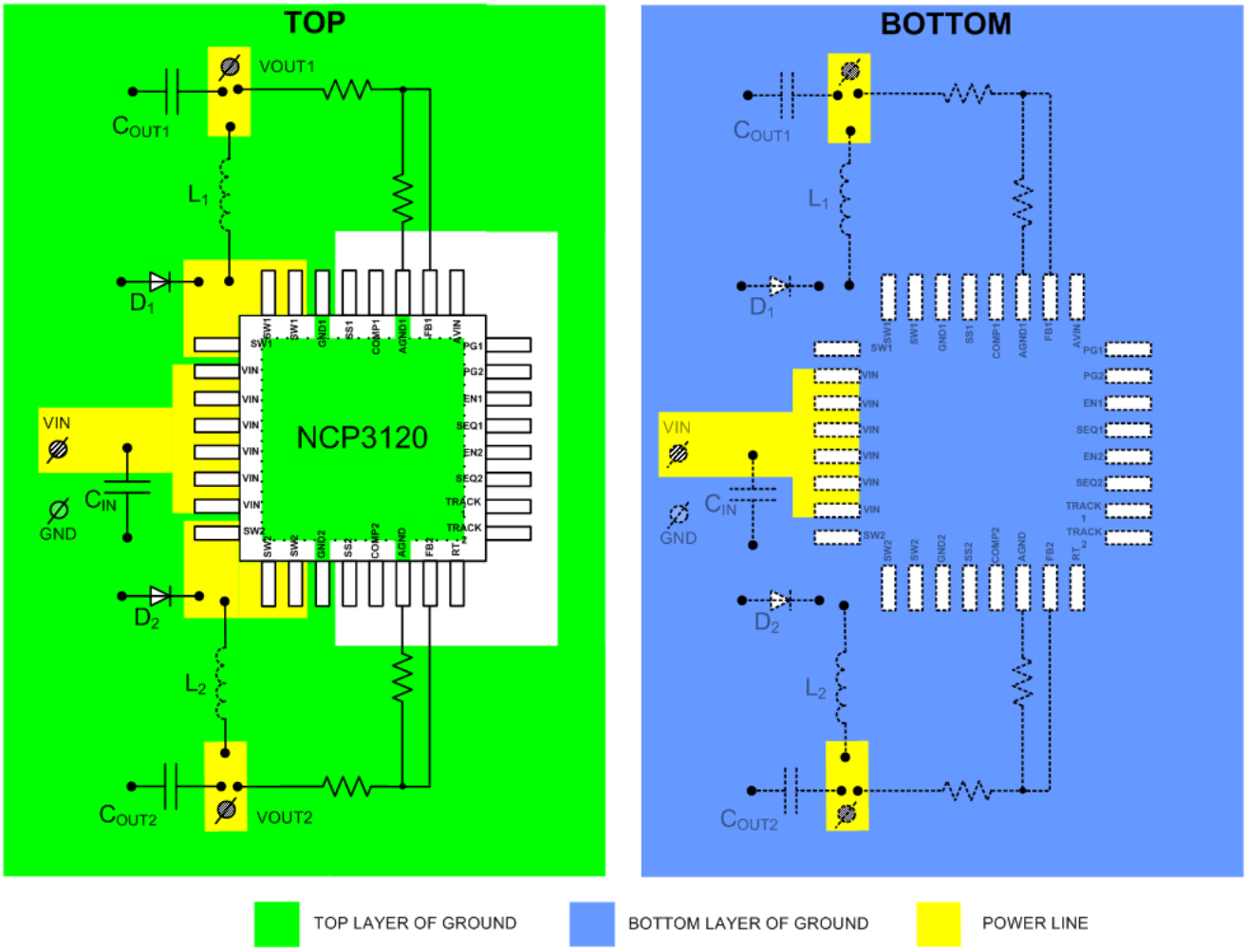


Figure 72. Typical Layout Diagram

Typical Application Circuit

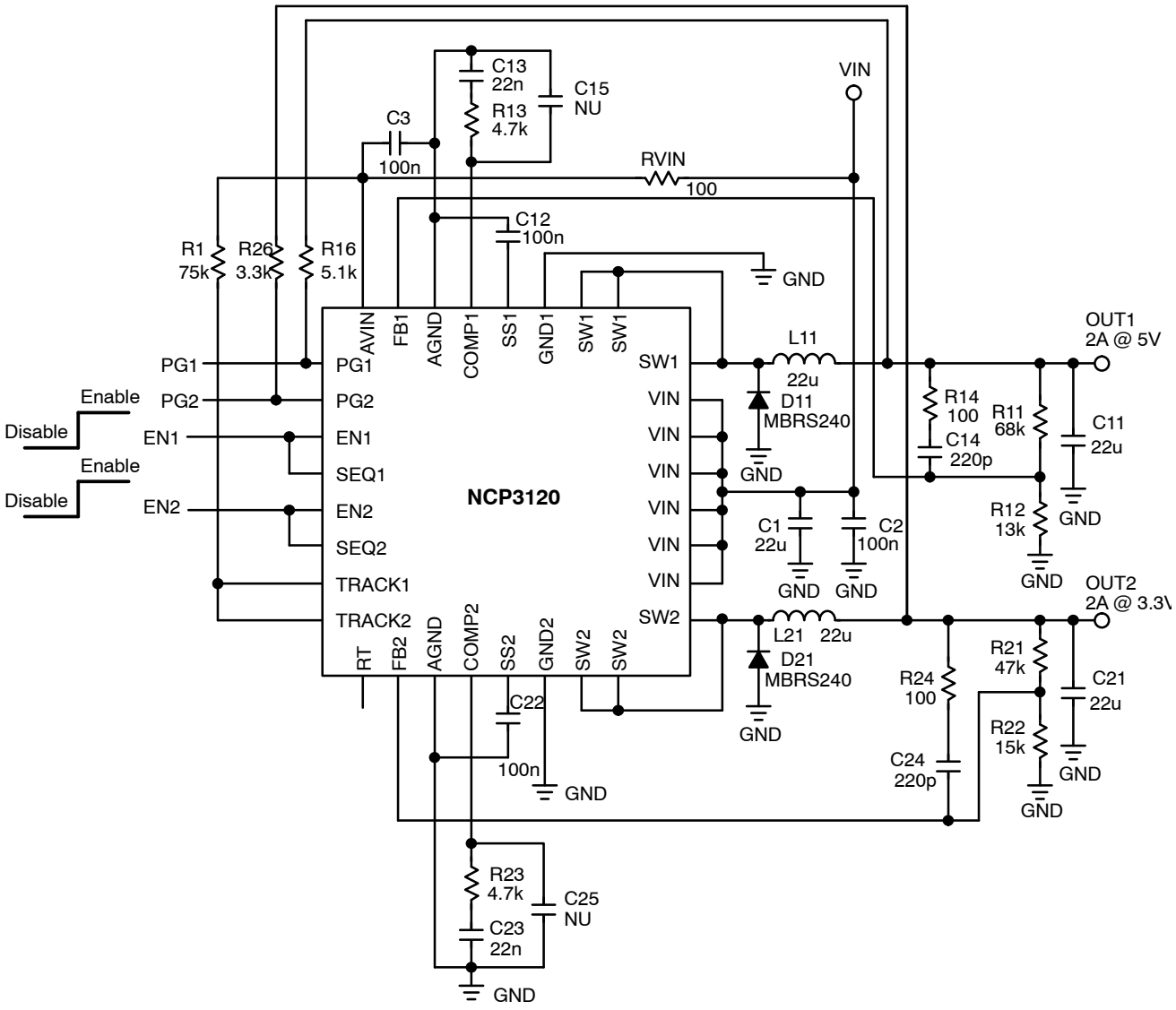
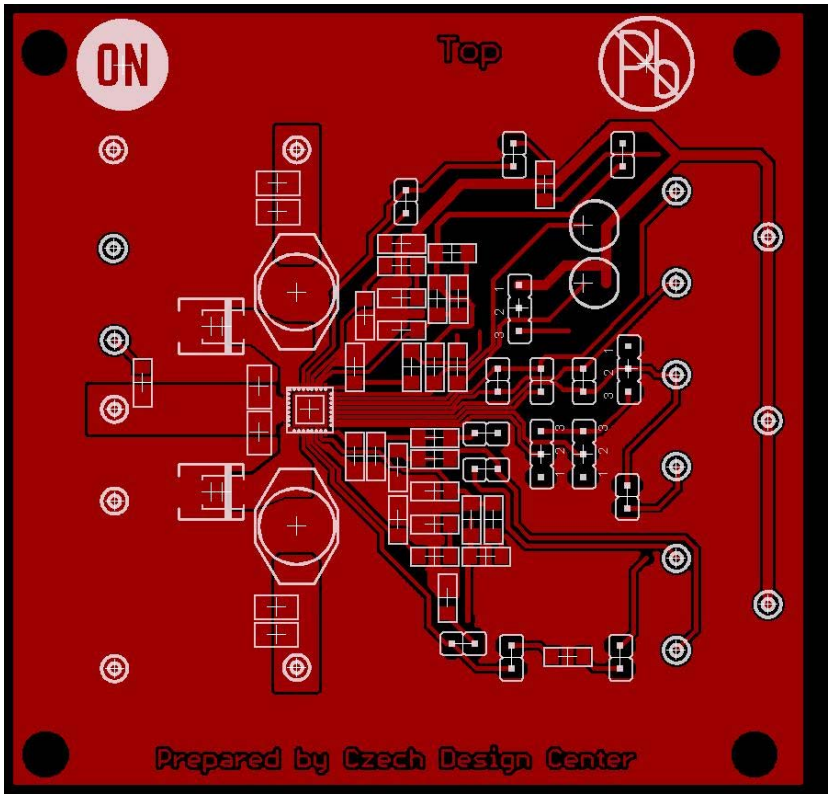


Figure 73. Typical Circuit Diagram

TOP



BOTTOM

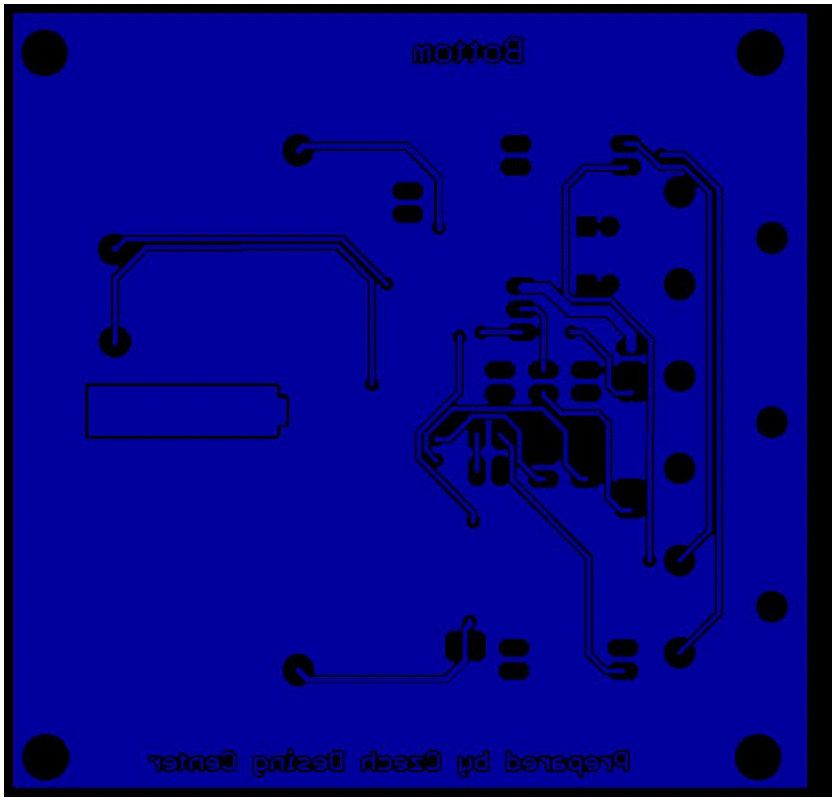


Figure 74. PCB Board Example – Evaluation Board v2.11

Components:

Table 7. Bill of Materials for the Typical Application Circuit

BOM of the NCP3120 – Evaluation Board v2.11						
Qty	**Value**		**Scale**	**Ref. Designator**	**Vendor**	**Part number**
Chip						
1			QFN32, 5x5 mm	NCP3120	ON Semiconductor	
Resistors						
3	100	Ω	1206	RV_{IN}, R14, R24	Vishay	RCA1206100R0FKEA
1	75	kΩ	1206	R1	Vishay	RCA120675KFKEA
1	68	kΩ	1206	R11	Vishay	RCA120668K0FKEA
1	13	kΩ	1206	R12	Vishay	RCA120613K0FKEA
2	4.7	kΩ	1206	R13, R23	Vishay	RCA12064K70FKEA
1	47	kΩ	1206	R21	Vishay	RCA120647K0FKEA
1	15	kΩ	1206	R22	Vishay	RCA120615K0FKEA
1	5.1	kΩ	1206	R16	Vishay	RCA12065K10FKEA
1	3.3	kΩ	1206	R26	Vishay	RCA12063K30FKEA
Capacitors						
3	22	μF	1210	C1, C11, C21	Kemet	C1210C226K4PAC
4	100	nF	1206	C2, C3, C12, C22	Epcos	B37872A5104K060
2	22	nF	1206	C13, C23	Epcos	B37872A5223K060
2	220	pF	1206	C14, C24	Epcos	B37871K5221J060
Inductors						
2	22	μH		L11, L21	Coilcraft	DO3340P−223
Diodes						
2	MBRS240LT3			D11, D21		ON Semiconductor

ORDERING INFORMATION

Device	Package	Shipping†
NCP3120MNTXG	QFN32 (Pb−Free)	4000 / Tape & Reel

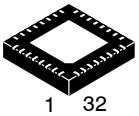
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

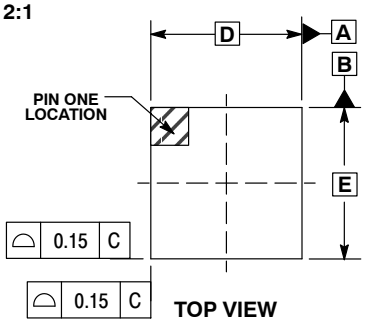
ON Semiconductor®

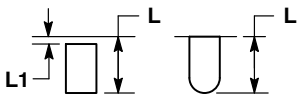
QFN32 5x5, 0.5P
CASE 488AM
ISSUE A

DATE 23 OCT 2013

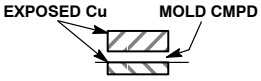


SCALE 2:1

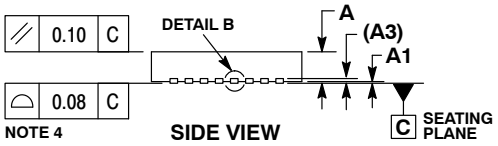


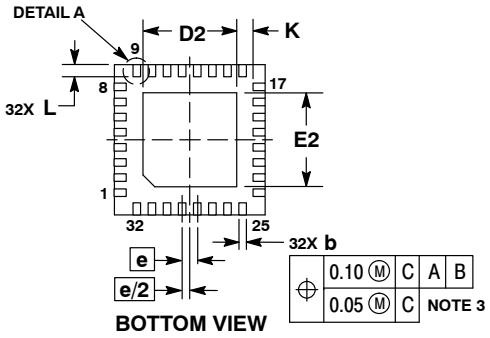


DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTION

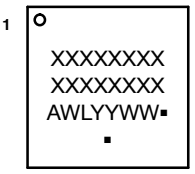




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	---	0.05
A3	0.20 REF	
b	0.18	0.30
D	5.00 BSC	
D2	2.95	3.25
E	5.00 BSC	
E2	2.95	3.25
e	0.50 BSC	
K	0.20	---
L	0.30	0.50
L1	---	0.15

GENERIC MARKING DIAGRAM*

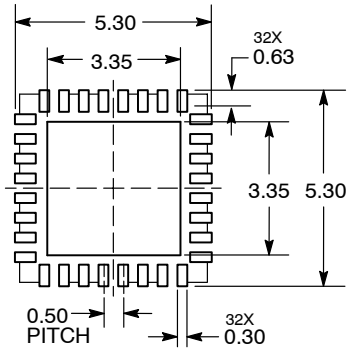


XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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