Enhanced, High-Efficiency Power Factor Controller

NCP1623

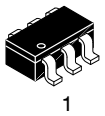
Features

- Valley Synchronized Frequency Fold−back (VSFF):
  - CrM at Heavy Load
  - DCM at Light Load by Dead Time Control
  - Valley Switching in Both CrM and DCM
- On−time Modulation for High PFC in Both CrM and DCM
- Follower Boost Capability (NCP1623A Only)
  - Lowered Output Voltage Regulation at Low Line
  - High−Efficient Boost Stage and Downsized Inductor Design
- Skip Mode for Light Load Regulation
- Sleep Mode with Low Current Consumption (SOIC8 Only)
- Fast Line / Load Transient Control
  - Dynamic Response Enhancer at Output Undershoot
  - Soft OVP and Fast OVP at Output Overshoot
- Excessive Current Protection
  - Over Current Protection (OCP)
  - Over Stress Protection (OVS)
- Brown Out Protection
- Second Over Voltage Protection (OVP2)
- These are Pb−Free Devices

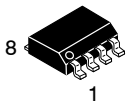
Typical Applications

- USB−PD
- Flat TV
- Industrial Power Supplies
- All Off−line Appliances Requiring Power Factor Correction

PACKAGE PICTURES

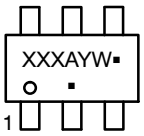


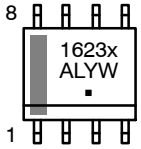
TSOP−6
(SOT23−6)
SN SUFFIX
CASE 318G−02



SOIC−8
D SUFFIX
CASE 751−07

MARKING DIAGRAMS



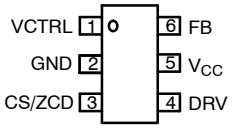


XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

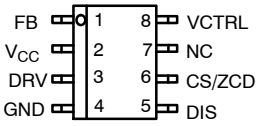
x = A
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)
TSOP−6



(Top View)
SOIC−8

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 16 of this data sheet.

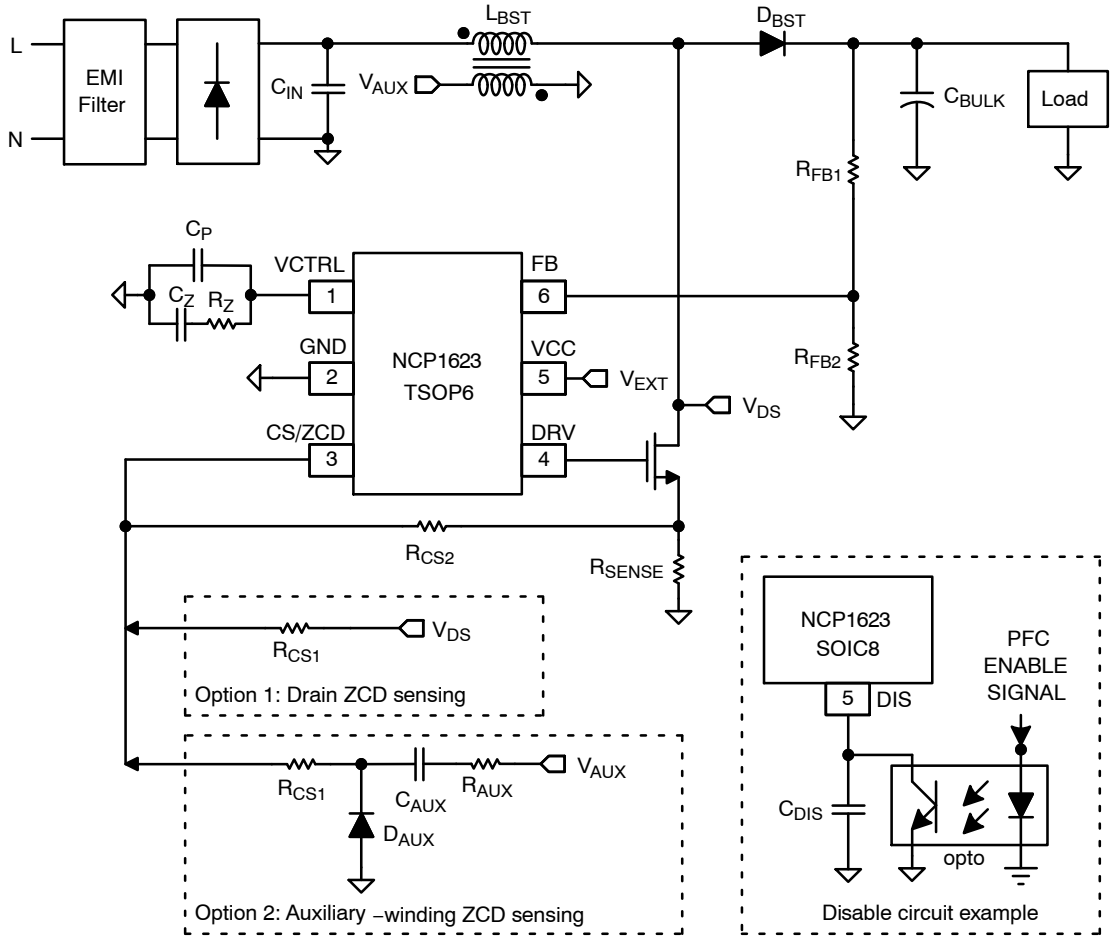


Figure 1. Application Schematic

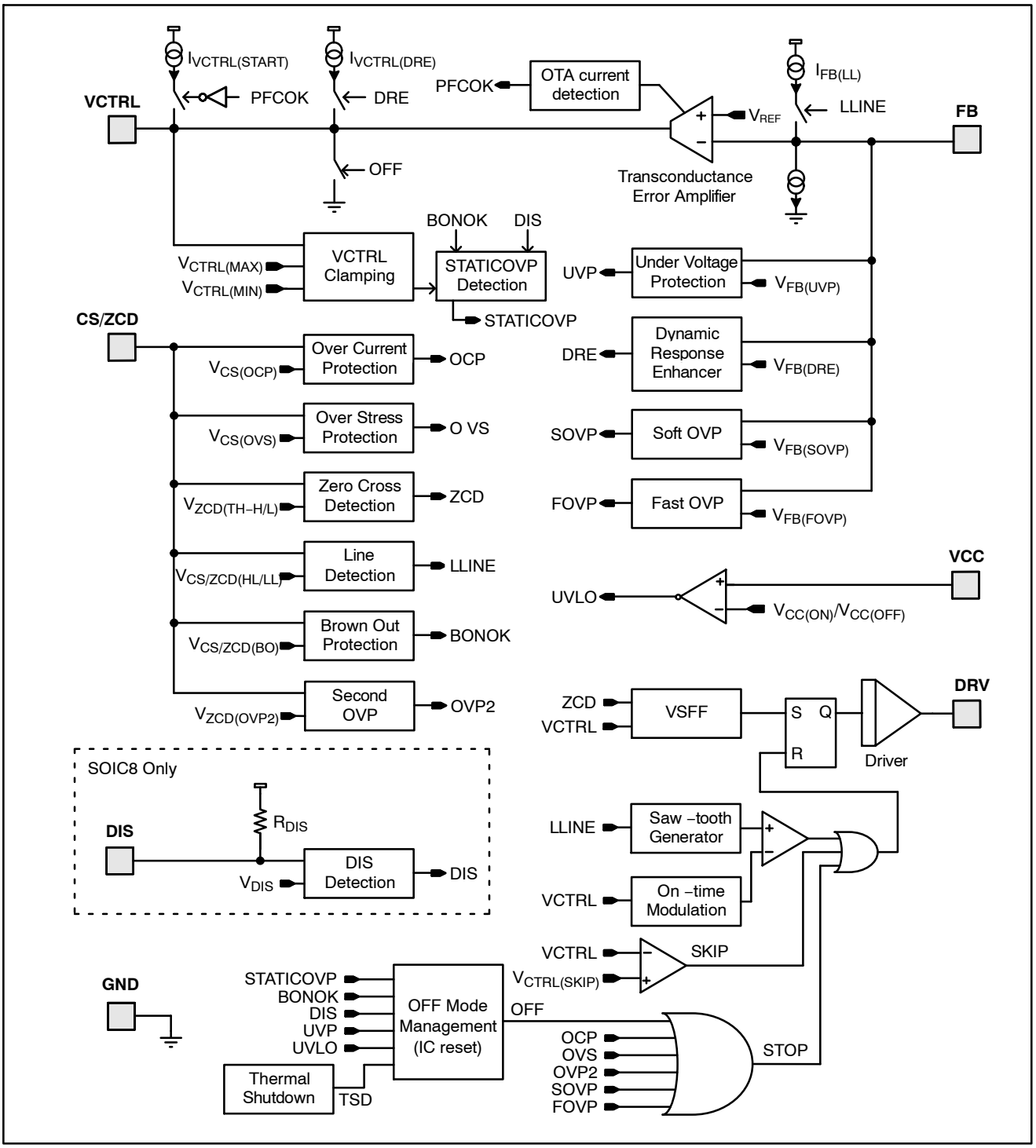
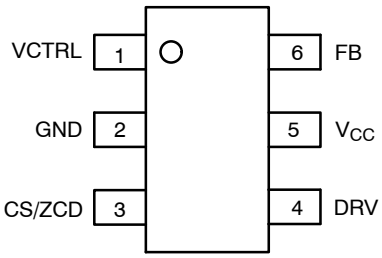
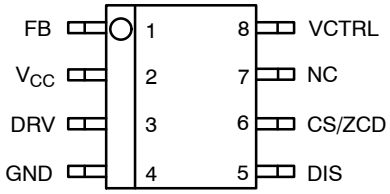


Figure 2. Simplified Block Diagram

PIN CONNECTIONS



(Top View)
TSOP−6



(Top View)
SOIC−8

Table 1. PIN DESCRIPTION

Pin Number TSOP−6	Pin Number SOIC−8	Pin Name	Description
1	8	VCTRL	The error amplifier output is connected to this pin. The regulation loop bandwidth is adjusted by the feedback compensation network connected between this pin and ground. When IC is reset at off mode, the NCP1623 grounds the VCTRL pin to provide a soft−start function at a subsequent startup.
2	4	GND	Power Supply Ground
3	6	CS/ZCD	Based on a novel technique, this multi−functional pin is designed to monitor inductor current, ZCD signal and input/output voltage.
4	3	DRV	The high−current capability of the totem pole gate drive makes it suitable to drive high gate charge power FETs.
5	2	V_{CC}	IC operating current is supplied to this pin.
6	1	FB	The feedback pin is connected to the input of the error amplifier to monitor the PFC output voltage for regulation. Also, this pin detects the PFC output transient condition to enable DRE, SOVP and FOVP for overshoot−less and undershoot−less output regulation. A 250 nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently open. NCP1623A FB pin further sources a current ($I_{FB(LL)}$ of 25 μA typically) to adjust a lower output regulation level in low−line conditions for higher efficiency and downsized boost inductor design.
	5	DIS	A high level or open circuit on this pin disables the controller and reduces I_{CC} bias current for low standby power.
	7	NC	No Connect (Note 1)

1. True no connect. Printed circuit board traces are allowable.

Table 2. MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Power Supply Input	V_{CC}	−0.3 to 30	V
CS/ZCD Pin with 5 mA of Clamp Current	CS/ZCD	−0.3 to 11.5	V
Feedback Pin	FB	−0.3 to 9	V
V_{CTRL} Pin	V_{CTRL}	−0.3 to 9	V
Disable Pin, SOIC−8 Version	DIS	−0.3 to 9	V
Driver Voltage	DRV	−0.3 to $V_{DRV(HIGH)}$ (Note 2)	V
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 3)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Note 4)	ESD_{HBM}	2	kV
ESD Capability, Charge Device Model (Note 4)	ESD_{CDM}	1	kV
Moisture Sensitivity Level	MSL	1	−

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. $V_{DRV(HIGH)}$ is the DRV high clamp voltage if V_{CC} is higher than $V_{DRV(HIGH)}$ V_{DRV} is V_{CC} otherwise.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78

THERMAL CHARACTERISTICS (Note 5)

Parameter	Symbol	Value	Unit
Thermal Characteristics, TSOP−6 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	230	°C/W
Thermal Characteristics, SOIC−8 Thermal Resistance, Junction−to−Air	$R_{\theta JA}$	153	°C/W

5. Mounted on a JEDEC standard 51−3 (1s0p) test board, 100 mm^2 copper area, 1 oz copper thickness.

RECOMMENDED OPERATING RANGES

Parameter	Symbol	Min	Max	Unit
Operating Junction Temperature Range	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 3. ELECTRICAL CHARACTERISTICS

(V_{CC} = 18.5 V and T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SUPPLY CIRCUIT						
V_{CC} Turn−On Voltage	$V_{CC(ON)}$	V_{CC} rising	9.75	10.50	11.25	V
V_{CC} Turn−Off Voltage	$V_{CC(OFF)}$	V_{CC} falling	8.5	9.0	9.5	V
V_{CC} Turn−On/Off Hysteresis	$V_{CC(HYS)}$	$V_{CC(ON)} - V_{CC(OFF)}$	1.0	1.5	2.0	V
V_{CC} Reset Voltage, I_{CC} Drops to $I_{CC(START)}$	$V_{CC(RST)}$	V_{CC} falling	6	7	8	V
IC Start−Up Current	$I_{CC(START)}$	V_{CC} = 7 V	–	20	50	μA
IC Operating Current without Switching	I_{CC1}	No switching	–	0.5	1.0	mA
IC Operating Current when Switching	I_{CC2}	f_{SW} = 50 kHz, No C_L load	–	2	3	mA
IC Sleep Mode Current, SOIC−8	$I_{CC(DIS)}$	DIS pin high	–	–	100	μA
GATE DRIVE						
DRV Rising Time	t_R	C_L = 1 nF	15	30	90	ns
DRV Falling Time	t_F	C_L = 1 nF	10	20	50	ns
DRV Source Resistance	R_{OH}		–	10	20	Ω
DRV Sink Resistance	R_{OL}		–	7	15	Ω
DRV High Clamp Voltage	$V_{DRV(HIGH)}$	V_{CC} = 30 V, R_L = 33 kΩ	10	12	14	V
ON−TIME CONTROL						
Maximum On−Time at Low Line Ver. A Ver. C	$t_{ON(MAX-LL)}$		 10.8 13.5	 12.5 16.5	 14.2 19.5	μs
Maximum On−Time at High Line Ver. A Ver. C	$t_{ON(MAX-HL)}$		 4.2 5.6	 5.0 6.6	 5.8 7.6	μs
On−Time Ratio of Low and High Line	$K_{TON(LL-HL)}$	$t_{ON(LL)}/t_{ON(HL)}$	2.0	2.5	3.0	–
Minimum On Time at Low−Line	$t_{ON(MIN-LL)}$		100	180	250	ns
Minimum On Time at High−Line	$t_{ON(MIN-HL)}$		50	100	150	ns
FREQUENCY FOLDBACK AND SKIP						
Dead−Time 1	t_{DT1}	V_{CTRL} = 0.63 V	13	18	23	μs
Dead−Time 2	t_{DT2}	V_{CTRL} = 0.75 V	5.5	8.5	11.5	μs
VCTRL Frequency Foldback Enter Voltage	$V_{CTRL(FF-EN)}$	V_{CTRL} falling	1.87	2.08	2.29	V
VCTRL Frequency Foldback Exit Voltage	$V_{CTRL(FF-EX)}$	V_{CTRL} rising	1.96	2.18	2.40	V
VCTRL Frequency Foldback Hysteresis	$V_{CTRL(FF-HYS)}$		75	100	120	mV
Minimum Frequency	f_{MIN}		24	28	32	kHz
VCTRL Skip Enter Voltage	$V_{CTRL(SKIP-EN)}$	V_{CTRL} falling	0.50	0.56	0.62	V
VCTRL Skip Exit Voltage	$V_{CTRL(SKIP-EX)}$	V_{CTRL} rising	0.55	0.62	0.68	V
VCTRL Skip Hysteresis	$V_{CTRL(SKIP-HYS)}$		40	70	100	mV
FEEDBACK REGULATION						
FB Regulation Reference Voltage	V_{REF}		2.44	2.50	2.56	V
FB Source Current at Low Line, Ver. A	$I_{FB(LL)}$		23.75	25.00	26.25	μA
Error Amplifier Source Current	$I_{EA(SOURCE)}$	V_{FB} = 2.4 V	15	20	25	μA
Error Amplifier Sink Current	$I_{EA(SINK)}$	V_{FB} = 2.6 V	−25	−20	−15	μA
Error Amplifier Gain	G_{EA}		110	200	290	μS
VCTRL Maximum Clamping Voltage	$V_{CTRL(MAX)}$	V_{FB} = 2 V	4.0	4.5	5.0	V
VCTRL Minimum Clamping Voltage	$V_{CTRL(MIN)}$	V_{FB} = 3 V	0.3	0.5	0.8	V
VCTRL Startup Source Current	$I_{VCTRL(START)}$		90	120	150	μA

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 18.5 V and T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
FEEDBACK DYNAMIC RESPONSE ENHANCER (DRE)						
FB DRE Enter Voltage Ratio	$K_{FB(DRE-EN)}$	$V_{FB(DRE-EN)}$ / V_{REF}	94.5	95.5	96.5	%
FB DRE Exit Voltage Ratio	$K_{FB(DRE-EX)}$	$V_{FB(DRE-EX)}$ / V_{REF}	96.5	97.5	98.5	%
FB DRE Hysteresis Ratio	$K_{FB(DRE-HYS)}$		1	2	3	%
VCTRL DRE Source Current	$I_{VCTRL(DRE)}$		180	215	250	μA
FEEDBACK SOFT AND FAST OVER VOLTAGE PROTECTION (SOVP AND FOVP)						
FB SOVP Enter Voltage Ratio	$K_{FB(SOVP-EN)}$	$V_{FB(SOVP-EN)}$ / V_{REF}	103.5	105.0	106.5	%
FB SOVP Exit Voltage Ratio	$K_{FB(SOVP-EX)}$	$V_{FB(SOVP-EX)}$ / V_{REF}	101.5	103.0	104.5	%
FB SOVP Hysteresis Ratio	$K_{FB(SOVP-HYS)}$		1	2	3	%
FB SOVP Enter Voltage Ratio at Low Line, Ver. A	$K_{FB(SOVP-EN-LL)}$	$V_{FB(SOVP-EN-LL)}$ / V_{REF}	108.5	110.0	111.5	%
FB SOVP Exit Voltage Ratio at Low Line, Ver. A	$K_{FB(SOVP-EX-LL)}$	$V_{FB(SOVP-EX-LL)}$ / V_{REF}	106.5	108.0	109.5	%
FB SOVP Hysteresis Ratio at Low Line, Ver. A	$K_{FB(SOVP-HYS-LL)}$		1	2	3	%
FB FOVP Enter Voltage Ratio	$K_{FB(FOVP-EN)}$	$V_{FB(FOVP-EN)}$ / V_{REF}	105.5	107.0	108.5	%
FB FOVP Exit Voltage Ratio	$K_{FB(FOVP-EX)}$	$V_{FB(FOVP-EX)}$ / V_{REF}	103.5	105.0	106.5	%
FB FOVP Hysteresis Ratio	$K_{FB(FOVP-HYS)}$		1	2	3	%
FB FOVP Enter Voltage Ratio at Low Line, Ver. A	$K_{FB(FOVP-EN-LL)}$	$V_{FB(FOVP-EN-LL)}$ / V_{REF}	112.5	114.0	115.5	%
FB FOVP Exit Voltage Ratio at Low Line, Ver. A	$K_{FB(FOVP-EX-LL)}$	$V_{FB(SOVP-EX-LL)}$ / V_{REF}	110.5	112.0	113.5	%
FB FOVP Hysteresis Ratio at Low Line, Ver. A	$K_{FB(FOVP-HYS-LL)}$		1	2	3	%
FEEDBACK UNDER VOLTAGE PROTECTION (UVP)						
FB UVP Enter Voltage	$V_{FB(UVP-EN)}$	V_{FB} falling	240	300	360	mV
FB UVP Exit Voltage	$V_{FB(UVP-EX)}$	V_{FB} rising	470	530	590	mV
FB UVP Enter Voltage at Low Line, Ver. A	$V_{FB(UVP-EN-LL)}$	V_{FB} falling	1.1	1.2	1.3	V
FB UVP Exit Voltage at Low Line, Ver. A	$V_{FB(UVP-EX-LL)}$	V_{FB} rising	1.2	1.3	1.4	V
FB UVP Sink Current	$I_{FB(UVP)}$		50	250	450	nA
CURRENT SENSE AND ZERO CURRENT DETECTION						
CS Over−Current Protection (OCP) Voltage	$V_{CS(OCP)}$		450	500	550	mV
CS OCP Leading Edge Blanking Time	$t_{OCP(LEB)}$		320	400	460	ns
CS OCP to DRV Off Delay Time	$t_{OCP(DLY)}$	$dV_{CS/ZCD}$ / dt = 10 V/μs	–	40	200	ns
CS Over−Stress Protection (OVS) Voltage	$V_{CS(OVS)}$		675	750	825	mV
CS OVS Leading Edge Blanking Time	$t_{OVS(LEB)}$		50	200	350	ns
CS OVS Watch Dog Timer	$t_{OVS(WDG)}$		700	800	900	μs
ZCD High Threshold Voltage	$V_{ZCD(TH-H)}$	$V_{CS/ZCD}$ rising	5	40	75	mV
ZCD Low Threshold Voltage	$V_{ZCD(TH-L)}$	$V_{CS/ZCD}$ falling	−75	−40	−5	mV
ZCD Low Threshold Hysteresis	$V_{ZCD(TH-HYS)}$		50	80	110	mV
ZCD Blanking Time	$t_{ZCD(BLANK)}$		500	600	700	ns
ZCD to DRV On Delay Time Ver. A Ver. C	$t_{ZCD(DLY)}$		 170 250	 220 310	 270 370	ns
ZCD Watch Dog Timer	$t_{ZCD(WDG)}$		80	200	320	μs
CS/ZCD Source Current for Short−to−Ground Pin Detection	$I_{ZCD(GND)}$		40	50	60	μA
CS/ZCD Threshold Voltage for Short−to−Ground Pin Detection	$V_{ZCD(GND)}$		200	240	280	mV
CS/ZCD Clamp Voltage	$V_{CS/ZCD(CL)}$	$I_{CS/ZCD}$ = 5 mA	8.0	9.5	11.5	V

Table 3. ELECTRICAL CHARACTERISTICS (continued)
(V_{CC} = 18.5 V and T_J = −40°C to 125°C, unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LINE RANGE DETECTION						
CS/ZCD High Line Detection Voltage	$V_{CS/ZCD(HL)}$	$V_{CS/ZCD}$ rising	1.65	1.80	1.95	V
ZCD Low Line Detection Voltage	$V_{CS/ZCD(LL)}$	$V_{CS/ZCD}$ falling	1.45	1.55	1.65	V
ZCD Line Detection Hysteresis	$V_{CS/ZCD(LD-HYS)}$		200	300	400	mV
CS/ZCD Line Detection Blanking Time	$t_{LD(BLANK)}$	$V_{CS/ZCD}$ falling	20	25	30	ms
CS/ZCD Line Detection Watch Dog Timer, Ver. A	$t_{LD(WDG)}$		430	500	560	ms
BROWN–OUT (BO) – DISABLED IN A AND C VERSION						
CS/ZCD BO Enter Voltage	$V_{CS/ZCD(BO-EN)}$	$V_{CS/ZCD}$ falling	730	790	850	mV
CS/ZCD BO Exit Voltage	$V_{CS/ZCD(BO-EX)}$	$V_{CS/ZCD}$ rising	860	940	1020	mV
CS/ZCD BO Hysteresis	$V_{CS/ZCD(BO-HYS)}$		130	145	160	mV
CS/ZCD BO Blanking Time	$t_{BO(BLANK)}$		35	50	65	ms
VCTRL BO Sink Current	$I_{VCTRL(BO)}$		20	30	40	μA
SECOND OVER VOLTAGE PROTECTION (OVP2) – C VERSION ONLY						
ZCD OVP2 Enter Voltage	$V_{ZCD(OVP2-EN)}$	$V_{CS/ZCD}$ rising	3.61	3.77	3.93	V
ZCD OVP2 Blanking Time	$t_{OVP2(BLANK)}$		0.8	1.0	1.2	μs
ZCD OVP2 Reset Time to Disable DRV	$t_{OVP2(RST)}$		55	75	95	ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold (Note 6)	T_{LIMT}		150	–	–	°C
Thermal Shutdown Hysteresis (Note 6)	H_{TEMP}		–	50	–	°C
DISABLE MODE – SOIC8 ONLY						
DIS Sleep Mode Enter Voltage	$V_{DIS(EN)}$	V_{DIS} rising	1.5	1.8	2.1	V
DIS Sleep Mode Exit Voltage	$V_{DIS(EX)}$	V_{DIS} falling	0.8	1.1	1.4	V
DIS Sleep Mode Hysteresis	$V_{DIS(HYS)}$		0.5	0.7	0.9	V
DIS Sleep Mode Detection Blanking Time Ver. A Ver. C	$t_{DIS(BLANK)}$		 16 16	 25 25	 34 34	 ms μs
DIS Pull – Up Resistance	R_{DIS}		370	530	690	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Values based on design and/or characterization.

DEFINITIONS

General

Extremely compact, the NCP1623 is designed to optimize the efficiency of your PFC stage throughout the load range. It also incorporates protection features for a rugged operation. More generally, NCP1623 is ideal in systems where cost−effectiveness, reliability, high power factor and efficiency ratios are key requirements:

Low Start−Up Current and Large V_{CC} Range

The A and C versions ($V_{CC(ON)}$ of 10.5 V typically) are preferred in applications where the controller is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start−up level (11.25 V, $V_{CC(ON)}$) eases circuit powering from traditional 12−V rails. After start−up, the high V_{CC} maximum rating allows a large V_{CC} operation range from 9.5 V up to 30 V, thus easing the circuit feeding.

Output Stage Totem Pole

NCP1623 incorporates a −0.5 A / +0.8 A gate driver to efficiently drive most power FETs typically used in 70 to 300 W power supplies. As V_{CC} can be as high as 30 V, an internal clamp limits the DRV pin to 14 V max to be compatible with typical gate−source max ratings of industry MOSFETs.

Valley Synchronized Frequency Fold−Back

NCP1623 classically operates in critical conduction mode (CrM) until the power drops below a threshold level where the PFC stage enters the discontinuous conduction mode (DCM) with a dead time prolonged as the load further decays (frequency foldback). This novel technique also provides stable valley turn−on in both CrM and DCM for a maximized efficiency. In addition, the minimum frequency clamp (33 kHz typically) prevents audible frequencies and the on−time is modulated to ensure near−unity power factor in both CrM and DCM operations.

Compactness

The NCP1623 features the CS/ZCD multifunctional pin based on a novel technique for an enhanced control and a large bunch of protections in a small TSOP6 (or SOIC8) package with few external components. In addition, the NCP1623A forces a lower output regulation level in low−line condition to raise the PFC stage efficiency and reduce its size. This 2−level Follower Boost technique best fits for applications where the downstream converter (like a flyback power supply) can withstand input voltage variations in a cost−effective and efficient manner.

Feedback Transient Control (SOVP, FOVP and DRE)

Since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start−up) may cause excessive over or under voltages. Firstly, the soft and fast over voltage protections (SOVP and FOVP) interrupt the power delivery when the output voltage is excessive. At output voltage undershoot, the circuit dramatically speeds up the regulation loop when the output voltage goes below the low detect threshold (dynamic response enhancer − DRE).

Over Current and Over Stress Protection (OCP, OVS)

The circuit senses the FET current and turns it off if the sensed current exceeds the OCP limit. In addition, the circuit pauses FET switching for 800 μs when the current reaches OVS threshold as result of an inductor saturation or a short of the bypass diode.

Brown−Out Protection (BO, Disabled in A and C Version)

The circuit detects too low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.

Second Over−Voltage Protection (OVP2, C Version Only)

CS/ZCD multi−functional pin is used to detect excessive output voltage levels and prevent a destructive output voltage runaway if the feedback network happens to be wrong. (incorrect resistors value, aging effects...)

Under−Voltage Protection (UVP)

This circuit turns off FET switching when the FB pin voltage drops close to 0 V at low ac line or a failure in the feedback network (e.g., accidental short to ground / open failure of the FB pin).

Thermal Shutdown (TSD)

An internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C. The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).

Disable Function (SOIC8 Package Only)

In case of SOIC8 package option, DIS pin is provided to disable most of the internal blocks in NCP1623 to minimize V_{CC} supply current.

APPLICATIONS INFORMATION

FREQUENCY CONTROL

Valley Synchronized Frequency Foldback (VSFF)

The NCP1623 implements the Valley Synchronized Frequency Fold−back (VSFF) which consists of operating the PFC stage in critical conduction mode (CrM) until the power drops below a threshold level. As the power is further reduced under the threshold, the PFC stage enters the discontinuous conduction mode (DCM) with a dead time which gets longer.

Practically, the output of the regulation error amplifier (V_{CTRL}) is used to select the operation mode and to adjust the dead−time duration. More specifically, the circuit enters the DCM mode when V_{CTRL} drops below a frequency foldback enter voltage, $V_{CTRL(FF-EN)}$ and remains in this mode until V_{CTRL} exceeds a frequency foldback exit voltage, $V_{CTRL(FF-EX)}$ with 100 mV hysteresis, $V_{CTRL(FF-HYS)}$. Figure 3 summarizes this functioning.

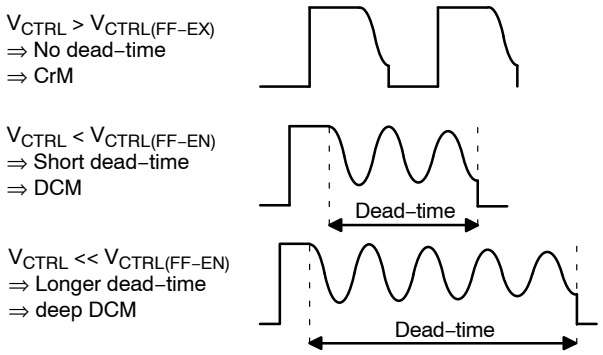


Figure 3. Drain Voltage in VSFF

V_{CTRL} determines the turn−on time (t_{ON}) in the voltage mode where $V_{CTRL} - V_{CTRL(MIN)}$ (0.5 V) sets t_{ON} proportionally and V_{CTRL} control range is up to $V_{CTRL(MAX)}$ (4.5 V). Therefore, the input power is determined by:

$$P_{IN} = \frac{V^2_{IN.RMS}}{2L} \cdot \frac{t_{ON(MAX)} \cdot \left(V_{CTRL} - V_{CTRL(MIN)}\right)}{V_{CTRL(MAX)} - V_{CTRL(MIN)}} \quad \text{(eq. 1)}$$

$V_{CTRL(FF-EN)}$ is typically 2.08 V for the A and C version so that the input power level entering frequency foldback is:

$$P_{IN} = \frac{V^2_{IN.RMS}}{2L} \cdot t_{ON(MAX)} \cdot 0.395 \quad \text{(eq. 2)}$$

To further improve efficiency, the MOSFET turn on is delayed until its drain−source voltage is at its valley. Practically, the circuit forces the dead−time dictated by the V_{CTRL} level. However, the NCP1623 does not immediately generate a DRV pulse if it detects that the FET drain−source voltage is not minimum. In other words, the dead−time is extended until the next valley is detected.

Whether the frequency is reduced by VSFF, an on−time modulation in NCP1623 adjusts the DRV turn−on time to compensate the dead−times in DCM for unity power factor. Also, the minimum frequency clamp prevents the system from operating at audible frequencies.

Minimum Switching Frequency

The DCM dead−time is an increasing function of $V_{CTRL(FF-EN)} - V_{CTRL}$. This frequency foldback function reduces the light−load switching frequency to optimize the efficiency. However, an internal minimum frequency logic limits the switching frequency above the audible frequency.

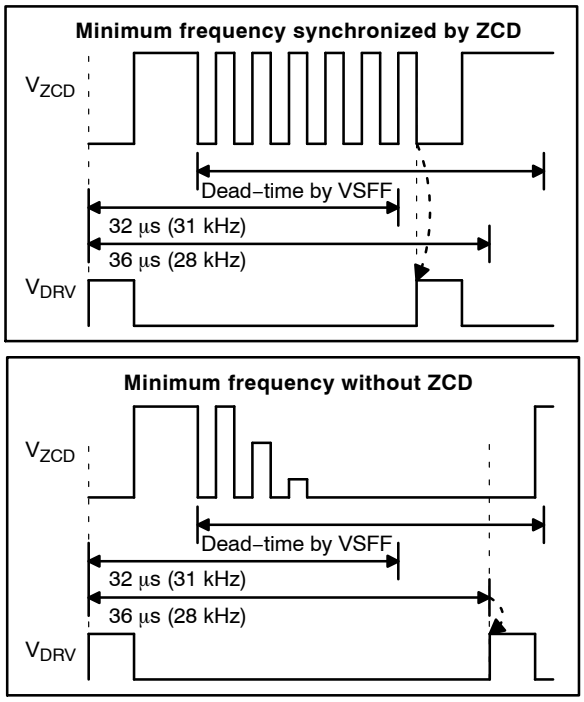


Figure 4. Minimum Switching Frequency

As shown by Figure 4, 32 μs switching period is counted and the DRV output will then turn on when the circuit detects the next valley. However, if no valley can be detected, DRV is forced high in 36 μs switching period whatever the drain−source voltage is. As a result, the minimum frequency is typically between 31 kHz (32 μs switching period) if a valley is immediately detected and 28 kHz (36 μs switching period) if no valley can be detected.

Note that if the circuit cannot detect ZCD signal at all during DRV turn−off time, the circuit does not generate any DRV pulses until the 200 μs ZCD watchdog time has elapsed.

ON−TIME MODULATION

When the FET is on, the inductor current of a CrM/DCM PFC boost stage starts from zero and ramps up with the slope of V_{IN}/L where L is the inductor value as shown in Figure 5. At the end of the on time (t_1 or t_{ON}), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is t_2. At that moment, a new switching cycle starts if the circuit operates in CrM. When in DCM, there is a dead time t_3 that lasts until the next clock is generated.

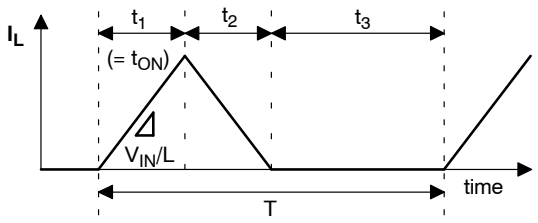


Figure 5. Inductor Current in DCM

One can show that in both CrM and DCM, the input current is given by:

$$I_{IN} = V_{IN}\frac{t_1 \cdot (t_1 + t_2)}{2 \cdot L \cdot T} = V_{IN}\frac{t_{ON} \cdot (t_1 + t_2)}{2 \cdot L \cdot T} \quad \text{(eq. 3)}$$

where $T = t_1 + t_2 + t_3$, switching period (t_3 being 0 in CrM).

In the light of the eq. 3, we note that I_{IN} is proportional to V_{IN} if $t_1 \cdot (t_1 + t_2)/T$ is a constant. In the voltage mode without On−time Modulation, DRV turn−on time (t_{ON} or t_1 in eq. 3) is set by:

$$t_{ON} = t_{ON(MAX)} \cdot \frac{V_{CTRL} - V_{CTRL(MIN)}}{V_{CTRL(MAX)} - V_{CTRL(MIN)}} \quad \text{(eq. 4)}$$

where $t_{ON(MAX)}$ is maximum turn−on time and $t_{ON(MAX)}$ at low−line is 2.5 times longer than high−line condition by 2−level line feedforward.

In order to keep $t_1 \cdot (t_1 + t_2)/T$ constant, NCP1623 further modulate t_{ON} by the factor of $T/(t_1 + t_2)$ information detected from previous switching:

$$t_{ON} = t_{ON(MAX)} \cdot \frac{V_{CTRL} - V_{CTRL(MIN)}}{V_{CTRL(MAX)} - V_{CTRL(MIN)}} \cdot \frac{T}{t_1 + t_2} \quad \text{(eq. 5)}$$

$(t_1 + t_2)/T$ in eq. 3 is removed by $T/(t_1 + t_2)$ in the modulated t_{ON} eq. 5 so that the input current is finally given by:

$$I_{IN} = V_{IN}\frac{t_{ON(MAX)}}{2 \cdot L} \cdot \frac{V_{CTRL} - V_{CTRL(MIN)}}{V_{CTRL(MAX)} - V_{CTRL(MIN)}} \quad \text{(eq. 6)}$$

Therefore, NCP1623 controls both CrM and DCM with no degradation in power factor and no discontinuity in the power delivery.

FEEDBACK REGULATION

OTA and VCTRL Function

A trans−conductance error amplifier (OTA) with access to the inverting input and output is provided as shown in Figure 6. It features a FB reference voltage for output voltage regulation of 2.5 V, a typical trans−conductance gain of 200 μS and a maximum capability of about ±20 μA OTA output current. The VCTRL pin is the output of the error amplifier for external loop compensation. Typically, a type−2 network is applied between the VCTRL pin and ground to set the regulation bandwidth below about 20 Hz. VCTRL basically controls turn−on time, dead time in VSFF, skip mode and STATICOVP:

- Turn−on time is proportional to $V_{CTRL} - V_{CTRL(MIN)}$ as in eq. 5.
- Dead time (ZCD to DRV turn−on delay time) is lengthened as V_{CTRL} is lowered from $V_{CTRL(FF-EN)}$.
- V_{CTRL} is pulled down by 30 μA $I_{VCTRL(BO)}$ when brown−out or DIS sleep mode entering process starts. If V_{CTRL} is lower than 0.5 V $V_{CTRL(MIN)}$ in the 30 μA current enable condition, STATICOVP is triggered and NCP1623 enters OFF mode.

Follower Boost − A version only

At low−line, a Follower Boost reduces the output voltage to optimize the PFC stage efficiency and significantly shrink its size and cost. In particular, the boost inductance and the MOSFET losses can be dramatically reduced. Since, the output voltage must remain higher than the line voltage, the output voltage is lowered in low line only while it remains regulated to the default nominal level generally set to 400 V in high−line conditions. Practically, the NCP1623A controls this 2−level follower boost operation through the feedback pin which sources the current $I_{FB(LL)}$ (25 μA typically) in low line detection condition. $I_{FB(LL)}$ offsets the feedback voltage as follows:

$$V_{FB} = \frac{R_{FB2}}{R_{FB1} + R_{FB2}} \cdot V_{OUT} + R_{FB1} \parallel R_{FB2} \cdot I_{FB(LL)} \quad \text{(eq. 7)}$$

where R_{FB1} and R_{FB2} are the upper and the lower resistors of the feedback bridge as shown in Figure 1.

Finally, the output regulation voltage level is:

$$V_{OUT} = \frac{R_{FB1} + R_{FB2}}{R_{FB2}} \cdot V_{REF} - R_{FB1} \cdot I_{FB(LL)} \quad \text{(eq. 8)}$$

Thus, the low−line regulation level depends on the feedback upper resistance, R_{FB1}. As an example, if R_{FB1} is 6 MΩ and R_{FB2} is 37.7 kΩ:

$$V_{OUT(HL)} = \frac{6\ M + 37.7\ k}{37.7\ k} \cdot 2.5 = 400\ V$$

$$V_{OUT(LL)} = 400\ V - 6\ M \cdot 25\ \mu = 250\ V$$

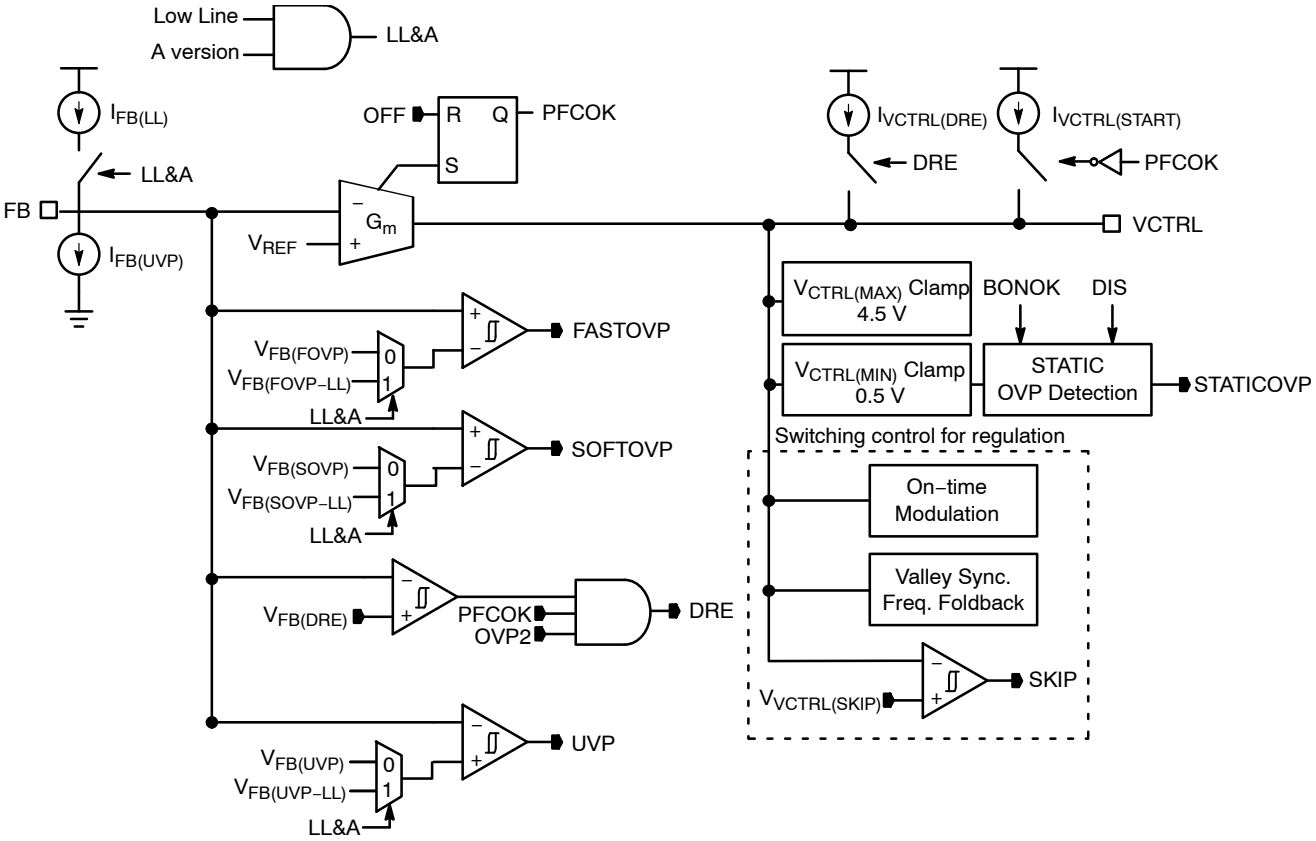


Figure 6. Feedback Regulation and Transient Control

FEEDBACK TRANSIENT CONTROL

Soft Start

At startup, $I_{VCTRL(START)}$ sources an external compensation capacitor properly for soft start. When FB voltage reaches close to V_{REF}, the sourcing current of the OTA is reduced to 0 A where PFCOK signal is set to high level and $I_{VCTRL(START)}$ is turned off.

Dynamic Response Enhancer (DRE)

The NCP1623 embeds a "Dynamic Response Enhancer" (DRE) that deals with the under−shoots of the output voltage at abrupt increases of the load current. An internal comparator monitors the FB pin and when this voltage is lower than 95.5% V_{REF}, a 200 μA $I_{VCTRL(DRE)}$ is sourced to speed up the charge of the compensation network as shown in Figure 6. Effectively this appears as a 10x increase in the loop gain. DRE is disabled during the start−up sequence until the PFC stage has stabilized and PFCOK is high. DRE is also disabled when the OVP2 (Second Over Voltage Protection) is triggered.

Soft / Fast Over Voltage Protection (SOVP, FOVP)

In case of output over−shoots, soft OVP is firstly triggered by comparing FB voltage and a soft OVP threshold, $V_{FB(SOVP)}$ as in Figure 6. Once the soft OVP is triggered, the turn−on time is gradually decreased in 4 to 5 switching periods to smoothly reduce powering. If FB voltage is even higher than a fast OVP threshold, $V_{FB(FOVP)}$, switching is immediately disabled. At low−line condition with A version enabling follower boost, soft and fast OVP thresholds, $V_{FB(SOVP−LL)}$ and $V_{FB(FOVP−LL)}$, are increased.

Based on these control methods at output voltage transient condition, NCP1623 triggers DRE, soft OVP and fast OVP at below levels:

- DRE:
  - $V_{FB(DRE)}$ = 95.5%/97.5% x V_{REF}
- Soft OVP:
  - $V_{FB(SOVP)}$ = 105%/103% x V_{REF}
  - $V_{FB(SOVP−LL)}$ = 110%/108% x V_{REF}
- Fast OVP:
  - $V_{FB(FOVP)}$ = 107%/105% x V_{REF}
  - $V_{FB(FOVP−LL)}$ = 114%/112% x V_{REF}

where $V_{FB(SOVP−LL)}$ and $V_{FB(FOVP−LL)}$ are set at low−line with Follower Boost enabled in A version.

Under Voltage Protection (UVP)

If the FB pin is open, V_{FB} is pulled down lower than an UVP threshold voltage ($V_{FB(UVP)}$) and DRV switching stops. The output voltage of the PFC stage is scaled down by a resistor divider and monitored by the OTA inverting input (FB pin voltage). FB sink current, $I_{FB(UVP)}$ for UVP, is minimized less than 450 nA to allow the use of a high impedance feedback resistor network.

CURRENT SENSE AND ZERO CROSS DETECTION

The NCP1623 uses CS/ZCD pin to detect a switching FET conduction current and drain voltage. The FET current is detected by a current sense resistor (R_{SENSE}) inserted between the FET source and ground. The drain voltage is monitored by directly sensing V_{DS} using a resistive bridge or by monitoring a reflected V_{DS}, typically obtained from an auxiliary winding as shown in Figure 1. The direct V_{DS} sensing is a simple solution with no auxiliary winding and the auxiliary winding based ZCD sensing is generally preferred to improve CS/ZCD noise immunity with lower standby power.

As illustrated in Figure 7, the CS/ZCD pin provides the input signal for the following functions:

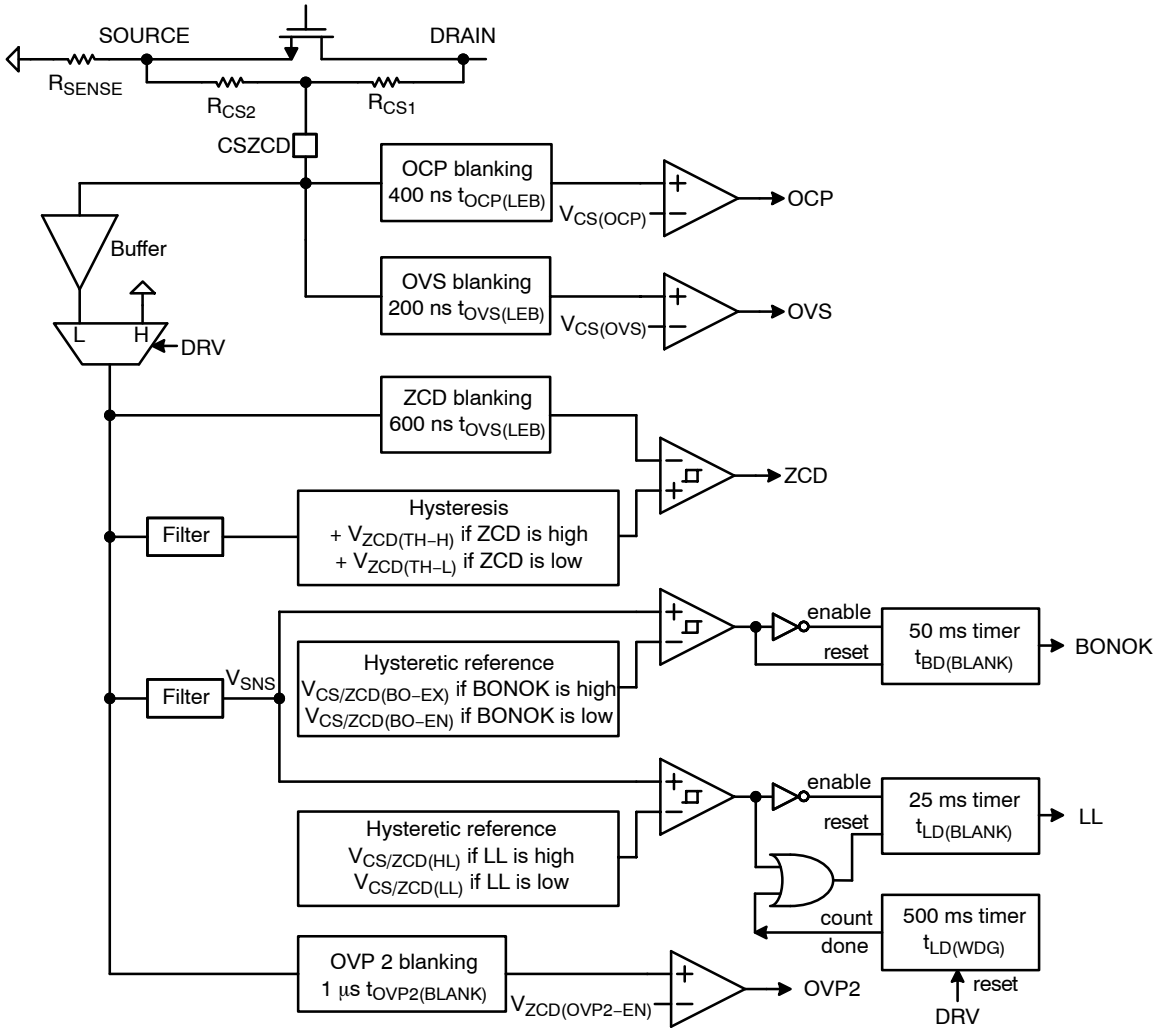


Figure 7. CS/ZCD Internal Circuit Block

Excessive Current Protection (OCP and OVS)

The NCP1623 turns off the FET when $V_{CS/ZCD}$ reaches the over−current threshold (500 mV $V_{CS(OCP)}$) after OCP blanking time (400 ns $t_{OCP(LEB)}$) from DRV on. In addition, if $V_{CS/ZCD}$ further exceeds the overstress level (750 mV $V_{CS(OVS)}$) after OVS blanking time (200 ns $t_{OVS(LEB)}$) from DRV on, FET is turned off for OVS watch dog time (800 μs $t_{OVS(WDG)}$).

Zero Current Detection (ZCD)

The NCP1623 turns on DRV at the valley of the drain−source voltage to minimize switching loss and noise. After ZCD blanking time (600 ns $t_{ZCD(BLANK)}$), $V_{CS/ZCD}$ is compared with the sum of the filtered $V_{CS/ZCD}$ and $V_{ZCD(TH-H/L)}$ hysteresis to generate ZCD signal.

When no signal is received that triggers the ZCD comparator during the off−time, an internal 200 μs ($t_{ZCD(WDG)}$) watchdog timer initiates the next drive pulse. At the end of this delay, CS/ZCD pin sources 50 μA $I_{ZCD(GND)}$ and compare $V_{CS/ZCD}$ with 240 mV $V_{ZCD(GND)}$ to detect a possible grounding of this pin and prevent a subsequent fault operation.

Line Sensing

A low pass filtered CS/ZCD voltage, V_{SNS}, is an image of the input voltage. The blanking time (25 ms, $t_{LD(BLANK)}$) for

low−line (LL) detection is set longer than a half−line cycle but not that long to quickly detects an abrupt line transient from high to low. When the line changes from low to high and V_{SNS} is over $V_{CS/ZCD(HL)}$, high line mode is immediately entered. When high−line is detected (that is, when signal "LL" of Figure 7 is low), the loop gain, t_{ON} / (V_{CTRL} − $V_{CTRL(MIN)}$) μs/V, is divided by about 2.5 to ensure a 2−level feedforward.

The FB pin of the A version sources the current $I_{FB(LL)}$ when low−line is detected. This is used to reduce the regulation level at low−line and hence provide the follower boost capability. Also, when follower boost is enabled, the line sensing result is forced to high−line if DRV switching is disabled for a line detection watch dog time (500 ms $t_{LD(WDG)}$).

Brown Out

The NCP1623 uses V_{SNS} (filtered $V_{CS/ZCD}$) for the input voltage detection same as the line sensing. By default, when powered, the circuit is in a fault state ("BONOK" high) and BONOK is set to low when V_{SNS} exceeds $V_{CS/ZCD(BO−EX)}$.

As shown in Figure 7, when V_{SNS} is lower than the brown−out enter voltage ($V_{CS/ZCD(BO−EN)}$) for BO blanking time (50 ms $t_{BO(BLANK)}$), BONOK signal is high and the drive is not immediately disabled. Instead, a 30 μA current source ($I_{VCTRL(BO)}$) gradually reduces V_{CTRL}. As a result, the circuit keeps generating DRV pulses until the STATICOVP trips (that is when V_{CTRL} reaches the minimum clamp level, 0.5 V $V_{CTRL(MIN)}$ as shown in Figure 6). This method relieves the risk of input voltage bouncing the fault line detection caused by EMI filter oscillation from an abrupt DRV stop.

Second Over Voltage Protection (OVP2)

During the FET turn−off time, the CS/ZCD pin signal is proportional to the output voltage and can hence unveil overshoots. This provides an additional protection to protect the PFC stage in case of a failure of the resistive network at FB pin. When an OVP2 fault is detected after OVP2 blanking time ($t_{OVP2(BLANK)}$) from DRV off, the circuit stops generating DRV pulses for 75 ms $t_{OVP2(RST)}$ typically. OVP2 is disabled for 60 ms at startup and for 10 ms at the end of 75 ms $t_{OVP2(RST)}$ time to prevent an abnormal OVP2 detection at the transient condition, but the output voltage could be over the OVP2 level if the bulk voltage is abruptly charged during these OVP2 disabling times.

THERMAL SHUT−DOWN

An internal thermal sensing circuitry disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150°C. The NCP1623 remains off until the junction temperature drops below about 100°C (50°C hysteresis). The temperature shutdown remains active as long as V_{CC} is higher than $V_{CC(RST)}$. The reset action forces the TSD threshold to 150°C so that any cold start−up will be done with the proper TSD level.

OFF MODE

The NCP1623 turns off DRV switching and enters the OFF mode when one of the following faults is detected:

- UVLO when $V_{CC} < V_{CC(OFF)}$.
- TSD when $T_J > 150°C$.
- UVP when $V_{FB} < V_{FB(UVP)}$.
- STATICOVP triggered by BO or DIS sleep mode.

In OFF mode, V_{CTRL} is grounded and PFCOK signal is reset to low. Also, the major part of the circuit sleeps except for UVLO, TSD, UVP, BO and DIS blocks.

In case of OFF mode triggered by DIS function, the circuit consumption is further minimized to $I_{CC(DIS)}$ (100 μA max).

DISABLE FUNCTION

The NCP1623 operation is disabled when the DIS pin voltage exceeds the DIS sleep mode enter voltage ($V_{DIS(EN)}$, 2.1 V maximum) for DIS blanking time ($t_{DIS(BLANK)}$). Practically, this occurs if the DIS pin is let floating since an internal 530 kΩ resistor pulls up the pin. In this case, the V_{CC} current consumption is reduced to $I_{CC(DIS)}$ (100 μA maximum) and the PFC stage stops operating.

Similar to power reducing sequence in brown−out, the drive is not immediately disabled and 30 μA current source gradually reduces V_{CTRL} until the STATICOVP function trips in Figure 6. The DIS sleep mode is maintained until the DIS pin is externally pulled down below the DIS sleep mode exit voltage ($V_{DIS(EX)}$, 0.8 V minimum).

If the NCP1623 enters the OFF mode by other fault detections (not by STATICOVP in DIS process), the DIS pin is grounded through a 530 kΩ resistor.

OUTPUT DRIVE

The output stage in DRV pin contains a totem pole optimized to minimize cross−conduction currents, making the NCP1623 compatible with high−frequency operation. Its high current capability (−500 mA / +800 mA) allows it to effectively drive high gate charge power FET. In the large V_{CC} range (up to 30 V), the DRV pin turn−on voltage is clamped up to 14 V.

FAILURE DETECTION

When manufacturing a power supply, components can be accidently shorted or improperly soldered. Such failures can also happen to occur later on because of the components fatigue or excessive stress. The false open/short circuits are generally required not to cause fire, smoke nor big noise. The NCP1623 integrates functions which help meet this requirement.

FB Pin Open Protection

A 250 nA sink current ($I_{FB(UVP)}$) pulls down the FB pin voltage if it is floating so that the UVP protection trips. This current source is small (450 nA maximum) so that its impact

on the bulk voltage regulation level remains negligible with typical feedback resistor dividers.

GND Pin Open Protection

If the GND pin is not connected, GND pin voltage is floating and could be higher than PFC stage power ground level. If NCP1623 detects a reversed voltage between GND and CS/ZCD pin for 800 μs, IC is reset with no switching operation.

CZ/ZCD Pin Short Protection

If ZCD signal is not detected at all at CS/ZCD pin short condition, ZCD watchdog timer doesn't allow DRV turn−on for 200 μs $t_{ZCD(WDG)}$. After the watchdog time, the NCP1623 checks the CS/ZCD pin short condition where the operation stops if $V_{CS/ZCD}$ is lower than 275 mV ($V_{ZCD(GND)}$ maximum) when shortly sourcing 40 μA ($I_{ZCD(GND)}$ minimum). Therefore, CS/ZCD pin external impedance should be higher than 7 kΩ.

Bypass Diode Short Protection

A bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current. When the bypass diode is short−circuited, the inductor current enters deep CCM as the discharging inductor current slope is very gentle. In such case, the overstress protection (OVS) can trip and stop the drive switching for 800 μs $t_{OVS(WDG)}$.

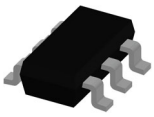
Table 4. ORDERING INFORMATION

Device	Marking	Package	Shipping†
NCP1623ASNT1G	UPD	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP1623ADR2G	1623A	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1623CDR2G	1623C		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

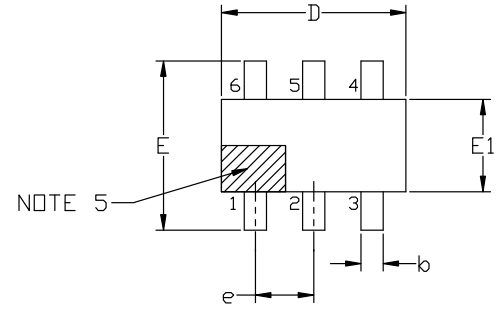
Table 5. CIRCUITS SPECIFIC OPTIONS

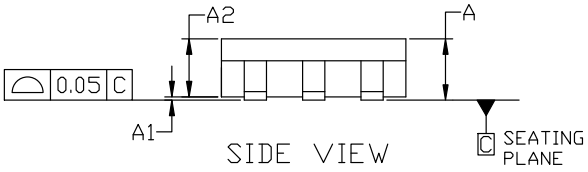
Options	NCP1623 Versions	
	A	C
Package	TSOP6 / SOIC8	SOIC8
Follower Boost	Yes	No
Maximum On−time at LL/HL	12.5 μs / 5.0 μs	16.6 μs / 6.6 μs
DIS Mode Detection Blanking Time (SOIC8 Only)	25 ms	25 μs
OVP2 Protection	No	Yes
Brown−Out Protection	No	No

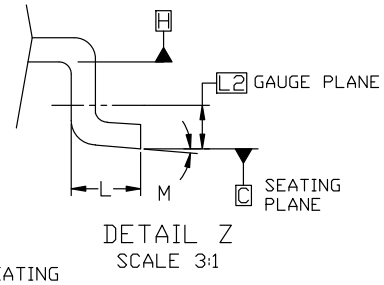


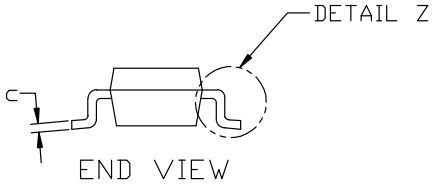
TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

DATE 26 FEB 2024



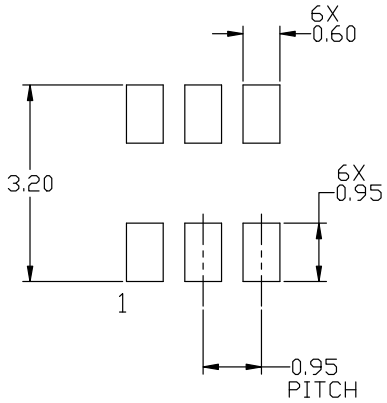






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN 1 INDICATOR MUST BE LOCATED IN THE INDICATED ZONE

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	---	10°



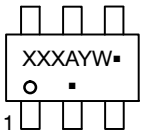
RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download th e ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

TSOP−6 3.00x1.50x0.90, 0.95P
CASE 318G
ISSUE W

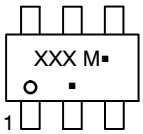
DATE 26 FEB 2024

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

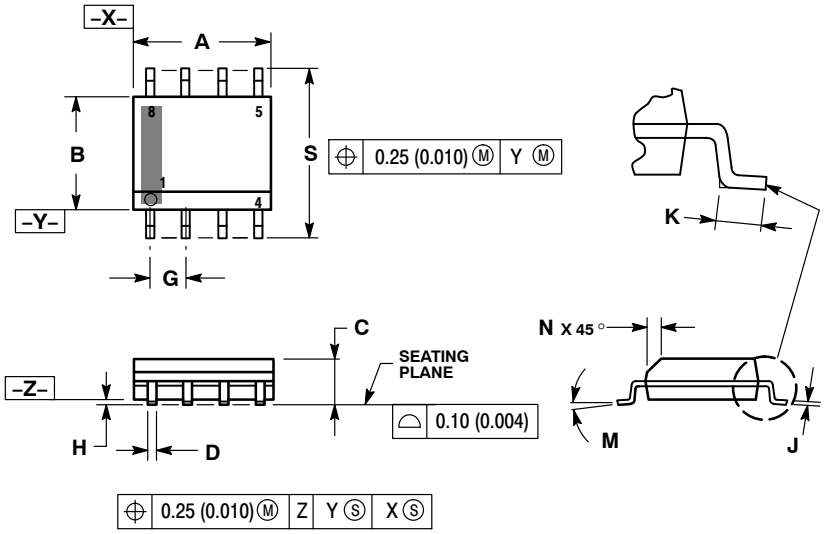
STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

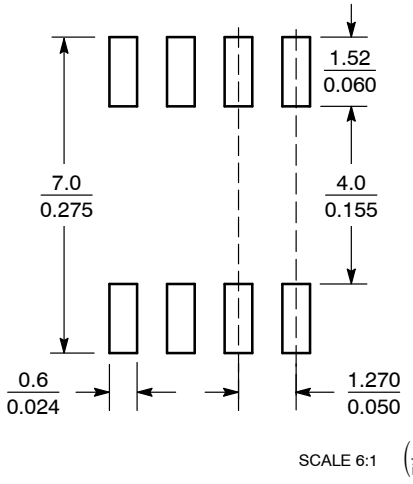
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

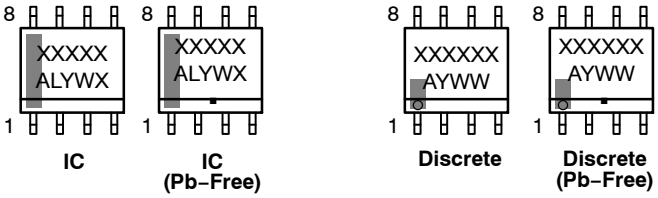
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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