ON Semiconductor

Is Now

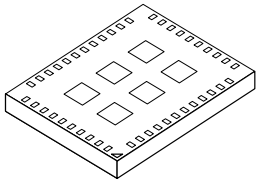
To learn more about onsemi™, please visit our website at
www.onsemi.com

KNX System-in-Package (SiP)

NCN5140S SiP

ON Semiconductor®

www.onsemi.com



SIP50, 10x8
CASE 127FD

Introduction

The NCN5140S System-In-Package enables building a complete KNX system in a very small form factor, utilizing a minimal number of external components.

The NCN5140S integrates an ARM® Cortex®-M0+ micro-controller together with all necessary passive components into one package. A certified KNX-stack comes with the NCN5140S System-in-Package, enabling rapid development of KNX-switch-applications in a very short time frame.

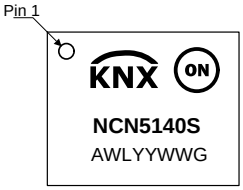
Key Features

- Fully-certified KNX-switch Application
  - Certified Physical Layer
  - Certified KNX Stack
- Several Pre-certified Hardware Designs:
  - Up to 8 Rocker Switch Buttons with RGB LEDs
  - Up to 8 Capacitive Touch Switch Buttons with RGB LEDs
- Built-in ARM® Cortex®-M0+ Micro-controller
- Full-featured NCN5130 KNX transceiver
- Only Three External Components Needed:
  - Vfilt Capacitor
  - Tx Resistor
  - Fanin Resistor
- Low Hardware and Software Development Effort
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Capacitive Touch Switches, up to 8 Buttons
- Rocker Switches, up to 8 Buttons
- RGB LEDs illuminating the Buttons

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NCN5140STXG	SIP50 (Pb−Free)	3000 / Tape & Reel
NCN5140SG	SIP50 (Pb−Free)	200 / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

TYPICAL APPLICATION DIAGRAM

Figure 1 shows a schematic for a KNX switch using the NCN5140S. This application has 4 capacitive touch buttons and RGB LEDs. Unused pins should be left floating unless otherwise noted.

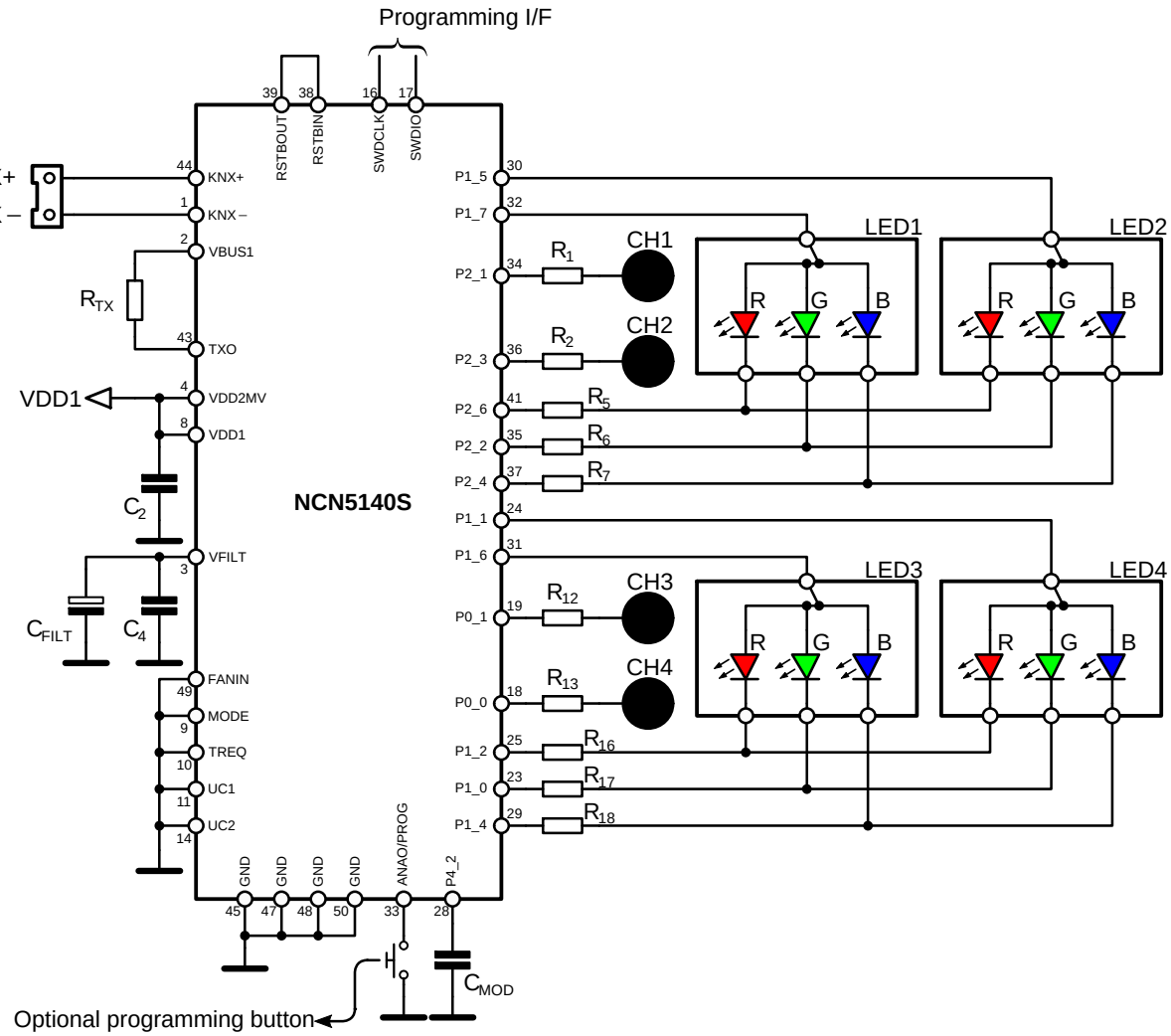


Figure 1. Typical Application Diagram for a KNX Switch using the NCN5140S

PACKAGE OUTLINE AND PIN DESCRIPTION

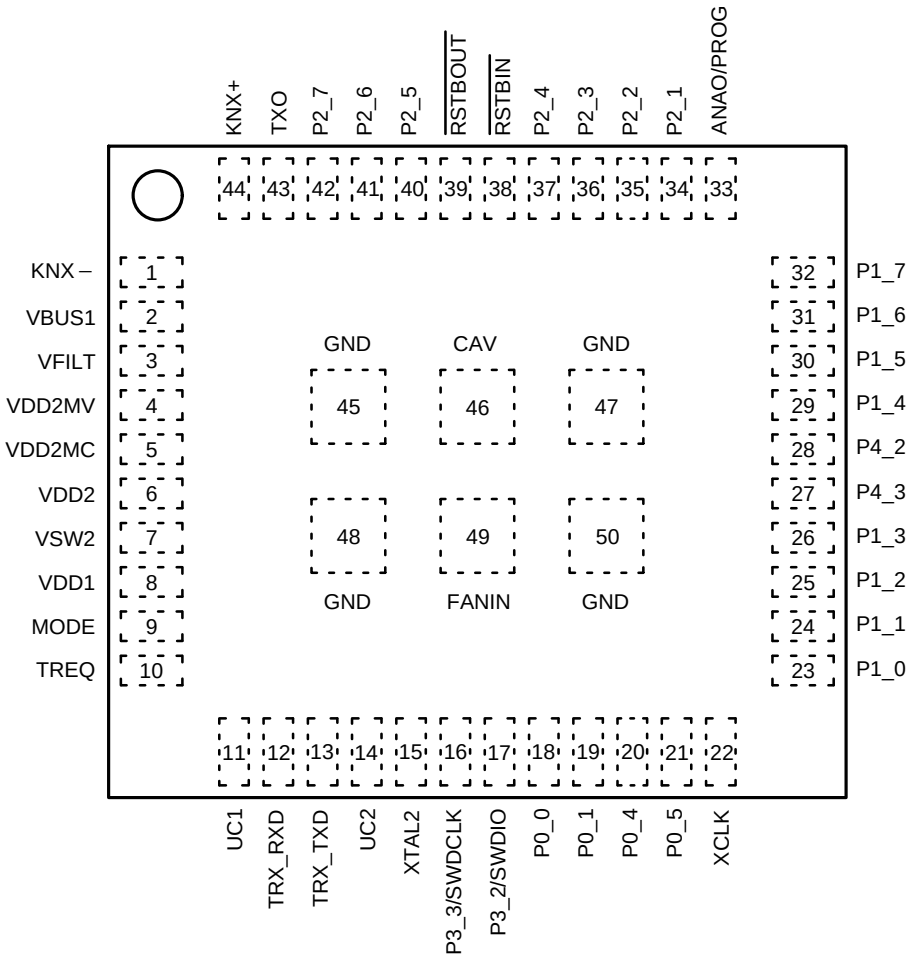


Figure 2. Pin Connection Diagram (Top View)

For detailed information on pin functionality, see the NCN5130 datasheet.

Table 1. PIN LISTING

Pin Number	Pin name	Type	Description
1	KNX−	Supply	KNX bus ground connection
2	VBUS1	Supply	KNX transmitter input
3	VFILT	Supply	Filtered bus voltage
4	VDD2MV	Analog Input	Voltage monitoring input Voltage Converter 2
5	VDD2MC	Analog Input	Current monitoring input Voltage Converter 2
6	VDD2	Analog Input	Second current monitoring input Voltage Converter 2
7	VSW2	Analog Output	Switching node Voltage Converter 2
8	VDD1	Analog Input	Current and Voltage monitoring input Voltage Converter 1
9	MODE	Digital Input	Mode selection input
10	TREQ	Digital Input	Test pin, tie to ground
11	UC1	Digital Input	UART configuration input
12	TRX_RXD	Digital Input	UART receive input
13	TRX_TXD	Digital Output	UART transmit output
14	UC2	Digital Input	UART configuration input

Table 1. PIN LISTING (continued)

Pin Number	Pin name	Type	Description
15	XTAL2	Analog Output	Quartz clock generator output
16	SWDCLK/P3_3	I/O	Serial wire debugging clock input or digital input output 3_3
17	SWDIO/P3_2	I/O	Serial wire debugging data input output or digital input output 3_2
18	P0_0	I/O	Digital input output 0_0
19	P0_1	I/O	Digital input output 0_1
20	P0_4	I/O	Digital input output 0_4
21	P0_5	I/O	Digital input output 0_5
22	XCLK	Digital Output	Oscillator clock output
23	P1_0	I/O	Digital input output 1_0
24	P1_1	I/O	Digital input output 1_1
25	P1_2	I/O	Digital input output 1_2
26	P1_3	I/O	Digital input output 1_3
27	P4_3	I/O	Digital input output 4_3
28	P4_2	I/O	Digital input output 4_2 or C_{mod} capacitor input for capacitive touch buttons
29	P1_4	I/O	Digital input output 1_4
30	P1_5	I/O	Digital input output 1_5
31	P1_6	I/O	Digital input output 1_6
32	P1_7	I/O	Digital input output 1_7
33	ANAO/PROG	Analog Output/ Digital Input	Monitoring pin analog parameters / Programming button input pin
34	P2_1	I/O	Digital input output 2_1
35	P2_2	I/O	Digital input output 2_2
36	P2_3	I/O	Digital input output 2_3
37	P2_4	I/O	Digital input output 2_4
38	RSTBIN	Digital Input	Microcontroller reset signal input
39	RSTBOUT	Digital Output	Reset digital output (open drain with pull-up)
40	P2_5	I/O	Digital input output 2_5
41	P2_6	I/O	Digital input output 2_6
42	P2_7	I/O	Digital input output 2_7
43	TXO	Analog Output	KNX transmitter output
44	KNX+	Supply	KNX bus supply connection
45	GND	Supply	Supply voltage ground
46	CAV	Analog I/O	Test pin, leave floating
47	GND	Supply	Supply voltage ground
48	GND	Supply	Supply voltage ground
49	FANIN	Analog Input	Fan-In input
50	GND	Supply	Supply voltage ground

ABSOLUTE MAXIMUM RATINGS

Convention: currents flowing in the circuit are defined as positive.

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{KNX+}	Voltage on KNX+ pin	−0.3	45	V
V_{TXO}	KNX Transmitter Output Voltage	−0.3	45	V
I_{TXO}	KNX Transmitter Output Current (Note 1)		250	mA
V_{BUS1}	Voltage on VBUS1 pin	−0.3	45	V
$V_{ANAO/PROG}$	Voltage on ANAO/PROG pin	−0.3	3.6	V
I_{BUS1}	Current Consumption VBUS1 pin	0	120	mA
V_{FILT}	Voltage on VFILT pin	−0.3	45	V
V_{DD2MV}	Voltage on VDD2MV pin	−0.3	3.6	V
V_{DD2MC}	Voltage on VDD2MC pin	−0.3	45	V
V_{DD2}	Voltage on VDD2 pin	−0.3	45	V
V_{SW2}	Voltage on VSW2 pin	−0.3	45	V
V_{DD1}	Voltage on VDD1 pin	−0.3	3.6	V
V_{ST}	Voltage on pins MODE, TREQ, UC1, TRX_TXD, TRX_RXD, UC2, XCLK, RESETBOUT, and FANIN	−0.3	3.6	V
V_{XTAL2}	Voltage on XTAL2 pin	−0.3	3.6	V
V_{GPIO_ABS}	MCU GPIO voltage (Px_x)	−0.5	3.6	V
I_{GPIO_ABS}	Maximum current per MCU GPIO pin	−25	25	mA
I_{LU}	Pin current for latch−up (Note 2)	−100	100	mA
T_{ST}	Storage temperature	−40	85	°C
T_J	Junction temperature (Note 3)	−40	85	°C
T_I	Internal operating temperature range	−40	85	°C
V_{HBM}	Human Body Model electronic discharge immunity (Note 4)	−2	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Room temperature, 27 Ω shunt resistor for transmitter, 250 mA over temperature range.
2. Tested according to JEDEC JESD78
3. Normal performance within the limitations is guaranteed up to the Thermal Warning level. Between Thermal Warning and Thermal Shutdown temporary loss of function or degradation of performance (which ceases after the disturbance ceases) is possible.
4. According to JEDEC JESD22−A114

RECOMMENDED OPERATING CONDITIONS

Table 3. OPERATING RANGES

Symbol	Parameter	Min	Max	Unit
V_{BUS1}	VBUS1 Voltage (Note 5)	20	33	V
V_{DD1}	Digital and Analog Supply Voltage	3.13	3.47	V
V_{IN}	Input Voltage DC−DC converter 1 and 2	(Note 6)	33	V
V_{DD2}	Input Voltage on VDD2 pin	1.2	21	V
V_{DD2MC}	Input Voltage on VDD2MC pin	1.2	21.1	V
V_{DD2MV}	Input Voltage on VDD2MV pin	1.2	V_{DD1}	V
V_{DIG}	Input Voltage on pins UC1, UC2, TRX_RXD, Px_x, RSTBIN, MODE, TREQ and PROG	0	V_{DD1}	V
V_{FANIN}	Input Voltage on FANIN pin	0	3.6	V
T_A	Ambient temperature	−40	85	°C
T_J	Junction temperature (Note 7)	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Static DC−value. During an equalization pulse the bus voltage must be between 11 V and 45 V.
6. Minimum operating voltage on the VIN pin should be at least 1 V above V_{DD1} and V_{DD2}.
7. Higher junction temperatures can result in reduced lifetime.

ELECTRICAL SPECIFICATIONS

Convention: currents flowing in the circuit are defined as positive.

Table 4. DC SPECIFICATIONS

Symbol	Pin(s)	Parameter	Remarks / Test Conditions	Min	Typ	Max	Unit
POWER SUPPLY							
V_{BUS}	VBUS1	Bus DC voltage	Excluding active and equalization pulse	20		33	V
I_{BUS1_Int}		Bus Current Consumption	V_{BUS} = 30 V, R_{FANIN} = 39 kΩ (fan−in 10 mA), DC2, V20V disabled, no crystal or clock		2.00	2.70	mA
			V_{BUS} = 20 V, R_{FANIN} = 9.8 kΩ (fan−in 40 mA)		3.50	4.40	
V_{BUSH}		Undervoltage release level	V_{BUS1} rising	17.1	18.0	18.9	V
V_{BUSL}		Undervoltage trigger level	V_{BUS1} falling	15.9	16.8	17.7	V
V_{BUS_Hyst}		Undervoltage hysteresis		0.6			V
KNX BUS COUPLER							
$\Delta I_{coupler}/\Delta t$	VBUS1	Bus Coupler Current Slope Limitation	FANIN floating, $V_{FILT} > V_{FILTH}$		0.40	0.50	A/s
			FANIN = GND, $V_{FILT} > V_{FILTH}$		0.80	1.00	
			R_{FANIN} = 10 kΩ, $V_{FILT} > V_{FILTH}$		1.51	1.95	
			R_{FANIN} = 13.3 kΩ, $V_{FILT} > V_{FILTH}$		1.17	1.47	
			R_{FANIN} = 20 kΩ, $V_{FILT} > V_{FILTH}$		0.78	0.98	
			R_{FANIN} = 42.2 kΩ, $V_{FILT} > V_{FILTH}$		0.37	0.48	
			R_{FANIN} = 93.1 kΩ, $V_{FILT} > V_{FILTH}$		0.17	0.23	
$\Delta I_{coupler\_lim, startup}$	VBUS1	Bus Coupler Startup Current Limitation	FANIN floating, $V_{FILT} > V_{FILTH}$	20.0	25.0	30.0	mA
			FANIN = GND, $V_{FILT} > V_{FILTH}$	40.0	50.0	60.0	
			R_{FANIN} = 10 kΩ, $V_{FILT} > V_{FILTH}$	45.0	72.2	114.0	
			R_{FANIN} = 13.3 kΩ, $V_{FILT} > V_{FILTH}$	45.0	70.7	86.0	
			R_{FANIN} = 20 kΩ, $V_{FILT} > V_{FILTH}$	40.0	48.5	57.5	
			R_{FANIN} = 42.2 kΩ, $V_{FILT} > V_{FILTH}$	19.5	23.4	27.8	
			R_{FANIN} = 93.1 kΩ, $V_{FILT} > V_{FILTH}$	9.4	11.3	13.1	
$\Delta I_{coupler\_lim}$	VBUS1	Bus Coupler Current Limitation	FANIN floating, $V_{FILT} > V_{FILTH}$	10.6	11.4	12	mA
			FANIN = GND, $V_{FILT} > V_{FILTH}$	20.5	22.3	24	
			R_{FANIN} = 10 kΩ, $V_{FILT} > V_{FILTH}$	39.6	43.9	47.0	
			R_{FANIN} = 13.3 kΩ, $V_{FILT} > V_{FILTH}$	30.0	33.0	35.2	
			R_{FANIN} = 20 kΩ, $V_{FILT} > V_{FILTH}$	20.3	22.1	23.6	
			R_{FANIN} = 42.2 kΩ, $V_{FILT} > V_{FILTH}$	9.4	10.7	11.9	
			R_{FANIN} = 93.1 kΩ, $V_{FILT} > V_{FILTH}$	4.2	5.1	6.0	
V_{FILTH}	VFILT	Undervoltage release level	V_{FILT} rising	10.1	10.6	11.2	V
V_{FILTL}		Undervoltage trigger level	V_{FILT} falling	8.4	8.9	9.4	V
FIXED DC-DC CONVERTER							
V_{IN}	VIN	Input voltage		4.47		33	V
V_{DD1}	VDD1	Output voltage		3.13	3.3	3.47	V
V_{DD1_rip}		Output voltage ripple	V_{IN} = 25 V, I_{DD1} = 40 mA		40		mV
I_{DD1_lim}		Overcurrent threshold		−100		−200	mA

Table 4. DC SPECIFICATIONS (continued)

Symbol	Pin(s)	Parameter	Remarks / Test Conditions	Min	Typ	Max	Unit
ADJUSTABLE DC-DC CONVERTER							
V_{IN}	VIN	Input voltage		V_{DD2} + 1		33	V
V_{DD2}	VDD2	Output voltage	$V_{IN} \geq V_{DD2}$ + 1 V	1.2		21	V
V_{DD2H}		Undervoltage release level	V_{DD2} rising		0.9 x V_{DD2}		V
V_{DD2L}		Undervoltage trigger level	V_{DD2} falling		0.8 x V_{DD2}		V
V_{DD2_rip}		Output voltage ripple	V_{IN} = 25 V, V_{DD2} = 3.3 V, I_{DD2} = 40 mA, L2 = 220 μH		40		mV
I_{DD2_lim}		Overcurrent threshold	R_3 = 1 Ω	−100		−250	mA
η_{VDD2}		Power efficiency (DC converter only)	V_{in} = 25 V, V_{DD2} = 3.3 V, I_{DD2} = 35 mA, L_2 = 220 μH (1.26 Ω ESR)		90		%
$R_{DS(on)\_p2}$		$R_{DS(on)}$ of power switch	See Figure 5			8	Ω
$R_{DS(on)\_n2}$		$R_{DS(on)}$ of flyback switch	See Figure 5			4	Ω
V_{DD2M}	VDD2MC	Input voltage on VDD2MC pin				21.1	V
R_{VDD2M}	VDD2MV	Input resistance VDD2MV pin		1			MΩ
$I_{leak,vsw2}$		Half-bridge leakage				20	μA
FAN-IN CONTROL							
$I_{pu,fanin}$	FANIN	Pull-up current FANIN pin	FANIN shorted to GND, pull-up connected to V_{AUX}	10	20	40	μA
DIGITAL INPUTS							
V_{IL}	UC2, TRX_RXD, UC1, TREQ, MODE, XCLK, XTAL2	Logic low threshold		0		0.7	V
V_{IH}		Logic high threshold		2.65		V_{DD1}	V
R_{DOWN}		Internal pull-down resistor	UC2, TRX_RXD and UC1 pins excluded. Only valid in Normal State.	5	10	28	kΩ
DIGITAL OUTPUTS							
V_{OL}	TRX_TXD, XCLK	Logic low output level		0		0.4	V
V_{OH}		Logic high output level		V_{DD1} − 0.45		V_{DD1}	V
I_L	UC2, XCLK, TRIG	Load Current				8	mA
	TRX_TXD, UC1					4	mA
V_{OL_OD}	SAVEB, RESETB	Logic low level open drain	I_{OL} = 4 mA			0.4	V
R_{up}		Internal pull-up resistor		20	40	80	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

INTERNAL SCHEMATIC

Figure 3 shows how the SiP is structured internally. Figure 2 shows the pin out of the chip as seen from the top.

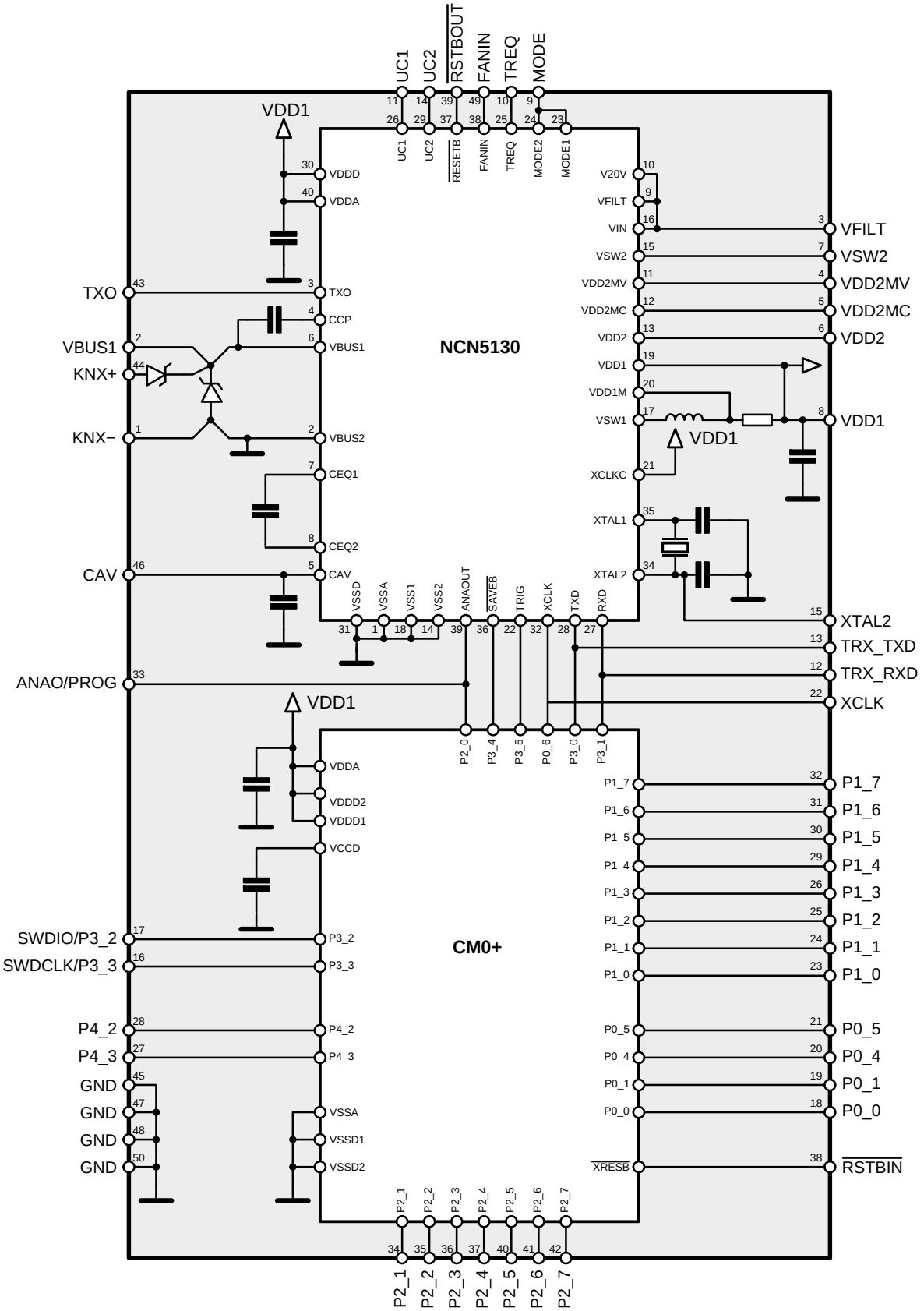


Figure 3. Schematic of the Internals of the SiP

FUNCTIONAL DESCRIPTION

The NCN5140S incorporates nearly all components necessary to build a complete KNX application. This greatly simplifies the application design effort and reduces the time to market significantly.

The NCN5140S supports KNX switch applications with either tactile or capacitive touch buttons. It is capable to drive up to eight buttons with RGB LED lighting for every individual button. Two fully certified hardware designs are available as evaluation boards showing the NCN5140S being used for an eight button switch application. The NCN5140BSCGEVB is the tactile button version and the NCN5140TSCGEVB the touch button version.

A fully certified software binary is delivered with these designs. This allows to apply for a derived KNX certificate without any software development and minimal hardware development. Refer to the KNX Association website for more information.

Only three components need to be added externally: a buffer capacitor C_{filt}, transmit resistor R_{tx} and fanin resistor R_{fanin}. The buffer capacitor and fanin resistor have to be dimensioned according to the current consumption of the application. In the following sections the correct dimensioning is explained. More information on dimensioning C_{filt} and the fan−in−resistor, can be found in the Application note AND90055/D.

Dimensioning C_{filt}

Abrupt load current steps are not allowed on the KNX bus. For this reason the buffer capacitor C_{filt} is present. This capacitor will absorb these load steps.

To dimension this capacitor, there are four requirements that have to be taken into account.

Capacitor Value Limits

The capacitance must always be $12.5\ \mu F < C_{filt} < 4000\ \mu F$, irrespective of other requirements. This is mandatory to guarantee normal operation of the device.

Start−up Time

A second requirement is the start−up time of the system. According to the KNX specification the total start−up time must be below 10 s.

The start−up time is determined by the time necessary to charge C_{filt} to 11 V and the time needed for the rest of the system to start up. A larger filtering capacitor results in a smaller start−up time for the rest of the system.

$$C < \left(10s - t_{startup,system}\right) \cdot \frac{I_{startup\_lim}}{V_{FILTH}} \qquad \text{(eq. 1)}$$

Note that the current limit during start−up is determined by the value of the fan−in resistor (see ‘*Selecting the correct fan−in*’).

Load Step

When a too large load step occurs, the voltage across C_{filt} will drop below V_{FILTL} and causes the device to go into reset. To avoid this, the capacitor should be dimensioned so it can handle the largest load step that might occur in the application.

$$C > \frac{\Delta I_{step}^{\ 2}}{2 \cdot \left(V_{BUS} - V_{coupler\_drop} - V_{FILTL}\right) \cdot I_{slope}} \qquad \text{(eq. 2)}$$

Warning Time

A last requirement is the desired warning time. This is the time between SAVEB going low followed by RESETB (Figure 4). During this time the microcontroller will write crucial data to flash memory. $t_{warning}$ is determined by the total current consumption of the system.

$$C > I_{system} \cdot \frac{\left(t_{warning} + t_{busfilter}\right)}{\left(V_{BUS} - V_{coupler\_drop} - V_{FILTL}\right)} \qquad \text{(eq. 3)}$$

Load Step during Start−up

During start−up abrupt load steps can easily cause the device to go into reset even if C_{filt} was dimensioned correctly. When the system indicates to the microcontroller that start−up is complete, C_{filt} is only charged to around 11 V. The capacitor holds much less charge than when one would wait for the C_{filt} to fully charge ($Q = C \cdot V$). So when the microcontroller directly applies a large load step in this situation, the system will go into reset.

To avoid this situation, there are two solutions:

- Implement a start−up delay in the microcontroller. During this time the microcontroller does nothing but wait for the delay to pass. This ensures that C_{filt} can charge fully before any loads are applied. This time must be accounted for when using Equation 1 by adding it to $t_{startup,system}$.
- Select a larger C_{filt} so that it can handle the large load step when it is only charged to 11 V.

The startup time of the binary which is delivered with the NCN5140S cannot be changed.

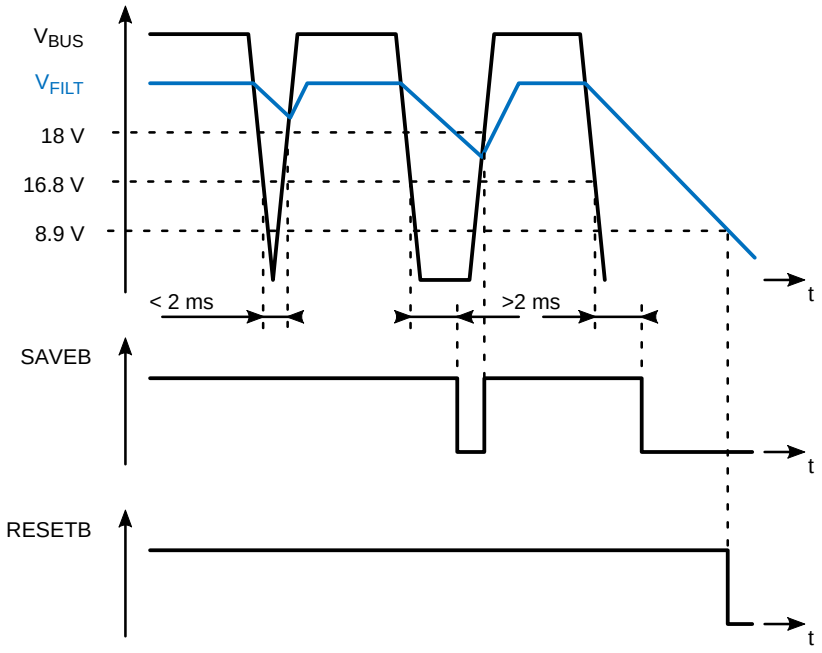


Figure 4. Behavior of SAVEB and RESETB during Shutdown

Selecting the Correct Fan-in

A KNX application can only draw a limited amount of current from the bus. The maximum amount of current the application can draw is defined during production and specified in the end product datasheet. This allows the network installer to calculate the required power rating of the KNX power supply.

The FANIN pin defines the maximum allowed bus current and bus current slopes. Table 5 gives an overview of possible fan-in settings.

For other resistor values, the typical current limit can be approximated using Equation 4.

$$I_{BUS} = 0.4 \times 10^{-3} + \frac{434}{R_6}\ [A] \qquad \text{(eq. 4)}$$

For more information refer to the ON Semiconductor Fan-In Application note AND90055/D. Definitions for Start-Up and Normal Operation can be found in the KNX Specification.

Adjustable DC−DC Converter

DC-DC2 provides a programmable voltage by means of an external resistor divider. DC-DC2 is not needed as an internal supply making it optional to use this DC-DC converter. If this supply is not used, tie the VDD2MV pin to VDD1.

The voltage divider can be calculated as follows:

$$R_4 = R_5 \cdot \frac{V_{DD2} - 1.2}{1.2} \qquad \text{(eq. 5)}$$

The DC-DC converter makes use of slope control to improve EMC performance.

Although the DC-DC converter is capable of delivering 100 mA, the maximum current capability will not always be usable. One always needs to make sure that the power consumption stays within the KNX specification. The allowed maximum output current for the DC-DC converters can be estimated as follows[1]:

$$\frac{V_{BUS} \cdot I_{BUS}}{2 \cdot \left[\left(V_{DD1} \cdot I_{DD1}\right) + \left(V_{DD2} \cdot I_{DD2}\right)\right]} \geq 1 \qquad \text{(eq. 6)}$$

I_{BUS} will be limited by the KNX standard and should be lower or equal to $I_{coupler}$ (see Table 4). The minimum V_{BUS} voltage is 20 V (see KNX standard). V_{DD1} and V_{DD2} can be found in Table 4. I_{DD1} and I_{DD2} must be chosen in a correct way to be in line with the KNX specification. Although the DC−DC converter can operate up to 21 V, it will not be possible to generate this voltage under all operating conditions.

See ON Semiconductor application note AND9135 for defining the optimum inductor and capacitor of the DC-DC converter. When using low series resistance output capacitors it is advised to split the current sense resistor as shown in Figure 5 to reduce ripple current for low load conditions.

[1] This formula is for a typical KNX-application. It's only given as guidance and does not guarantee compliance with the KNX standard.

Table 5. FANIN SETTINGS

Resistance [kΩ]	Bus Current Limit (min) [mA]	Start-up Current Limit (max) [mA]	Bus Current Slope (max) [mA/s]
250 − ∞	10.6	30.0	0.50
≤ 2	20.5	60.0	1.00
10.0	39.6	114.0	1.95
13.3	30.0	86.0	1.47
20.0	20.3	57.5	0.98
42.2	9.4	27.8	0.48
93.1	4.2	13.1	0.23

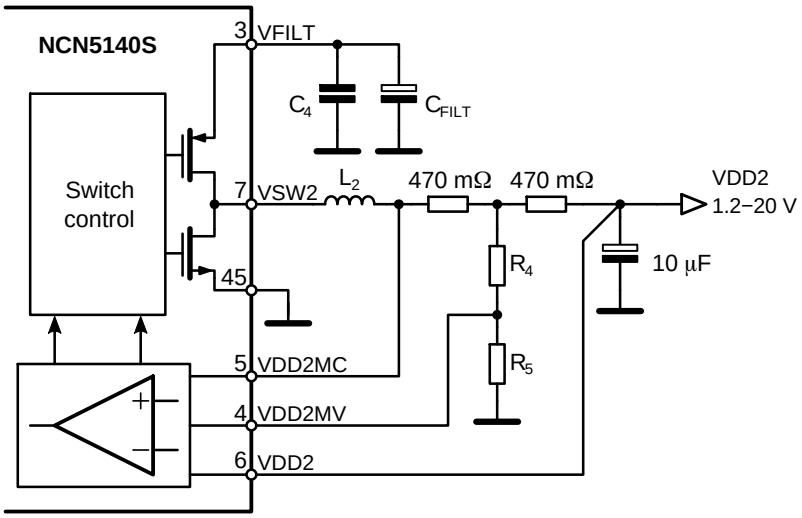


Figure 5. Adjustable DC−DC Converter

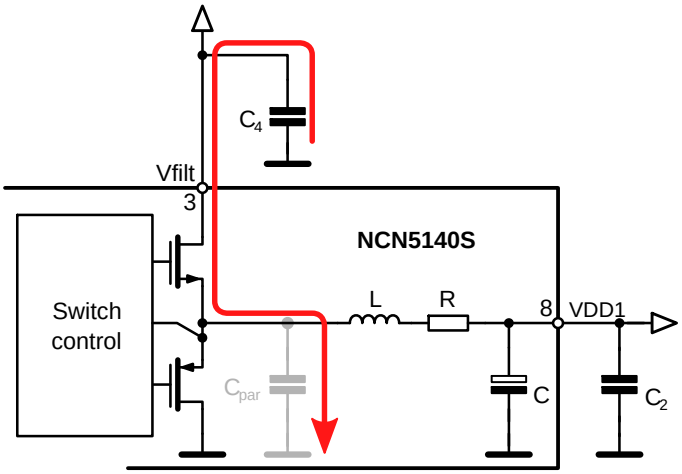


Figure 6. Critical Current Loop for the DC−DC Converter

Transmit Resistor

The last component that must be added externally is the transmit resistor. The KNX transmitter will use this resistor to generate active pulses on the KNX bus. As much current as necessary will be sunk through the resistor to make the bus voltage drop between 6 V to 9 V regardless of the bus impedance[2].

The resistor value must be between 24.3 Ω to 29.7 Ω to fulfil the KNX specification. The recommended nominal value is 27 Ω. As the resistor has to sink currents up to 400 mA, it must have a power rating of 1 W.

[2] Maximum bus impedance is specified in the KNX Twisted Pair Standard.

LAYOUT GUIDELINES

To guarantee a normal operation of the application, strict layout guidelines must be followed. The first series of guidelines ensure good EMC performance. Another critical layout section is the capacitive touch buttons. Many layout aspects must be taken into account to ensure proper operation of the buttons.

EMC Performance

Electromagnetic interference is dominated by the DC-DC converter. It switches at a frequency of around 300 kHz. Sufficient thought must be put into the layout to prevent radiated emissions from becoming an issue.

Figure 6 shows the most critical current loop. When the top transistor of the DC-DC converter is switched on, the instantaneous current will come from C_4. This current will charge the parasitic capacitor at the output of the converter. The layout in Figure 7 shows how to keep this loop as short as possible by placing C_4 close to the VFILT pin.

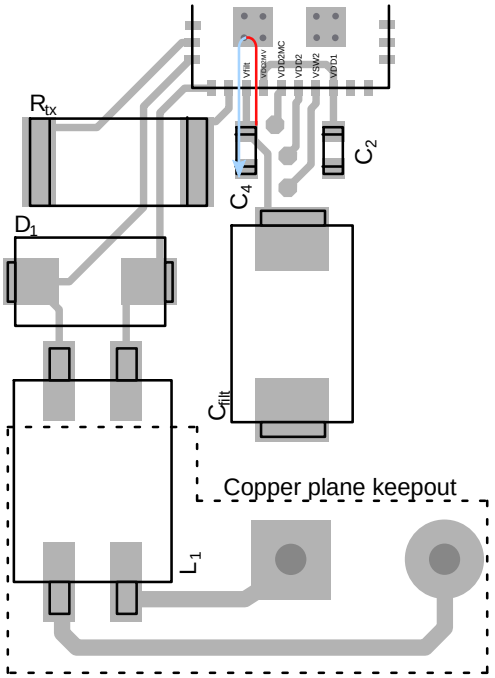


Figure 7. Recommended Layout for the KNX Front End

Figure 7 shows a recommended example layout for the complete KNX front-end. Keeping all the tracks short is crucial to meet the EMC guidelines.

A first thing to consider is keeping the track going to the VFILT capacitor short as well as the ground return path. The current must be able to flow to the four central ground pads of the NCN5140S without any interruptions. Make sure to avoid any tracks on the bottom layer of the PCB that block return paths.

The layout of the transmit resistor R_{tx} (resistor between TXO and VBUS1) is also important. These tracks can easily radiate during data transmission. Keeping them short can be achieved by keeping the transmit resistor close to the chip. This resistor has a large package size (6432 metric) allowing the KNX+ and KNX− signals to be routed underneath it. This avoids the use of any vias.

A common-mode choke footprint (L_1) is present in the example layout. The choke only has to be included when necessary. A regular switch application does not require a common mode choke at the input terminals. When, for example, using binary inputs with long lengths of cable going to the switch, a common mode choke might be required.

When using a common-mode choke, no copper planes or traces (on all layers) should be present under the choke. This avoids common−mode noise from coupling into other traces/planes. To further improve common-mode noise immunity, the copper planes around the primary side signals of the choke should be removed.

Keep the KNX+ and KNX− signals short to avoid radiated emissions.

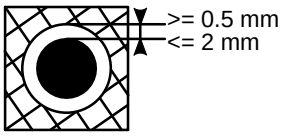


Figure 8. Limitation of the Gap between the Ground Hatch and the Touch Button

Capacitive Touch

When using capacitive touch buttons the layout of the buttons is critical for proper operation. A good layout is required in order to achieve good button sensitivity and Signal-to-Noise Ratio (SNR). Here only the most important layout guidelines will be discussed. For a complete guide on capacitive sensing applications refer to Cypress™ AN85951.

Parasitic Sensor Capacitance

Capacitive touch buttons operate on the principle of measuring changes in capacitance. To make the system work correctly, the parasitic capacitance C_P must be kept low. The main components contributing to C_P are trace capacitance, sensor pad capacitance, and pin capacitance of the device. The pin capacitance is device-dependent, only the sensor and trace capacitance can be adjusted during the design in order to meet the required C_P criteria.

The relationship between C_P and the PCB layout is rather complex. The parasitic capacitance increases with an increase in the sensor pad size. Increasing the length and width of the trace going to the sensor will also increase C_P. Both the sensor pad and trace capacitance is altered by changing the gap between the sensor pad and the ground hatch (Figure 8). Decreasing the gap between the sensor pad and the ground hatch increases C_P.

The parasitic capacitance must be kept low. In order to decrease C_P:

- Keep the trace lengths short. Reducing the trace length, increases noise immunity. (Section '*Trace Length and Width*')
- Use small track widths (≤ 0.18 mm).
- Reducing the sensor pad size is an option, but as a consequence reduces the finger capacitance and the sensitivity.
- Increase the gap between the ground hatch and the sensor pad. However this will also decrease noise immunity. The width of the gap between the hatched ground and the sensor pads should be equal to the thickness of the button overlay. Never make the gap larger than 2 mm or smaller than 0.5 mm. So when using a 3 mm thick overlay, only use a 2 mm wide gap.

In some special cases, it might be desired to use a small sensor pad size and very small trace lengths. This situation can occur when the sensor pad is placed very close to the NCN5140S. In this case there is a possibility that C_P is lower than the supported minimum.

If during the design of the sensor pads this is the case, add a footprint of a capacitor across the sensor as a precaution. When during application testing C_P seems to be lower than the supported minimum, place a 4.7 pF capacitor on the footprint. This will increase C_P and make sure it is in the supported range.

Board Layers

Most applications use a two-layer board. The sensor pads and the hatched ground planes are usually placed on the top side while all other components are placed on the bottom side. More complex designs use four layer PCBs.

- FR4−based PCBs perform well with a board thickness ranging from 0.5 mm to 1.6 mm.
- Flex circuits also work well with capacitive touch designs. Flex circuits can be used for curved surfaces. All PCB guidelines specified here also apply to flex circuits. Flex circuits with a thickness 0.25 mm or more should be used. The high breakdown voltage of the Kapton® material (290 kV/mm) used in flex circuits provides built-in ESD protection for the touch sensors.

Button Shapes

The design of the capacitive sensing button itself is very important. It is recommended to always use a circular sensor pad. Rectangular pads with rounded corners are also acceptable (Figure 9). Sharp corners (less than 90°) are not recommended since they concentrate electric fields. Recommended button shapes are shown in Figure 9.

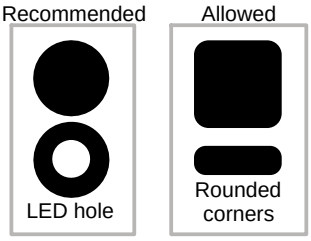


Figure 9. Allowed Button Shapes

The button diameter should be between 5 mm to 15 mm, where 10 mm is suitable for most applications. A thicker button overlay requires a larger button diameter. For an acrylic overlay the maximum overlay thickness is 5 mm. For other materials this value can be scaled according to their relative permittivity ε_r. Acrylic has an ε_r of around 2.5, so for other materials use the ratio $\varepsilon_r/2.5$ to calculate the maximum thickness.

Two adjacent buttons must be spaced such that when touching one button, the finger is not close to the gap between the other button and the ground hatch. This prevents false touch detection on adjacent buttons as Figure 10 shows.

Sensor and Device Placement

During the design of the application, follow these guidelines for the placement of the sensors and the NCN5140S:

- Minimize the trace length from the NCN5140S to the sensor pad.
- Mount series resistors within 10 mm from the GPIO pins in order to reduce RF-interference and to provide ESD-protection. Refer to section *Series Resistors on capacitive touch pins* for more information.
- If possible mount the NCN5140S and other components on the bottom side of the PCB.
- Avoid using a connector between the sensor pads and the GPIO pins of the NCN5140S. Connectors will increase C_P and noise pickup.

Trace Length and Width

Keep the traces going to the sensor pads as short as possible and use narrow trace widths. This minimizes the parasitic capacitance of the sensor. Trace lengths should be 300 mm maximum for standard PCBs and 50 mm for flex circuits. The trace width must be smaller than 0.18 mm. Surround the traces with hatched ground copper with a trace-to-hatch clearance of 0.25 mm to 0.51 mm.

Trace Routing

The traces going to the sensor pads must be routed on the opposite layer of the sensor pads (bottom layer in most cases). This is necessary to avoid any interaction between the finger and the traces. Routing traces under sensor pads other than the one it is connected to, is not allowed.

A large source of interference are other switching signals on the boards. This can be communication signals such as UART, SPI,... or, for example, a PWM-signal going to an LED. Keep a distance of at least 0.25 mm between capacitive touch sensor lines and other switching and communication lines. Increasing the distance between the sensing traces and other signals increases noise immunity.

Avoid running the sensing lines in parallel with communication and switching lines. Route the lines which can cause interference away from the sensing lines as shown in Figure 11. When it is necessary to cross the sensing lines with communication/switching lines on different layers, make sure they cross at a right angle as Figure 12 shows.

If due to spacing constraints sensor traces run in parallel with high-speed switching signals, it is recommended to place ground copper in between the sensor trace and the high−speed trace. Examples of high-speed signals are UART/SPI-communication lines,…

The width of the ground copper trace running between the lines should be at least 0.18 mm. Keep a spacing between the touch sensor trace and the ground copper of at least 0.254 mm in order to reduce the C_P of the capacitive touch sensor.

When it is not possible to run ground copper in between the traces, then follow the 3W rule to reduce crosstalk. The 3W rules states that “to reduce crosstalk from adjacent traces, a minimum spacing of two trace widths should be maintained from edge to edge”. This is illustrated in Figure 14.

Additional Crosstalk Solutions

Many applications use an LED as backlighting for panel overlay of the touch sensor buttons. This is commonly done by mounting an LED under the sensor pad which shines through a hole in the middle of the sensor pad (through the PCB). Another common technique is to use edge lighting in which the LED emits light in the side of the panel.

To control the brightness of the LED, PWM-control is commonly used. The LED is constantly switched ON and OFF, causing voltage transients. These can couple into the capacitive sensing traces creating noisy sensor data. To avoid crosstalk in this situation follow the guidelines in section *Trace Routing*.

Next to these guidelines it is also possible to reduce crosstalk by filtering the rapid voltage transitions. To do this place a low pass filter in the line driving the LED as Figure 15 shows. Design the filter based on the required LED response speed. C_1 is typically 100 nF and R_1 1 kΩ.

Vias

Use as little as possible vias to route the signals going to the sensor pads. This minimizes the parasitic capacitance. Place the vias near the edge of the buttons as shown in Figure 16 in order to reduce trace lengths.

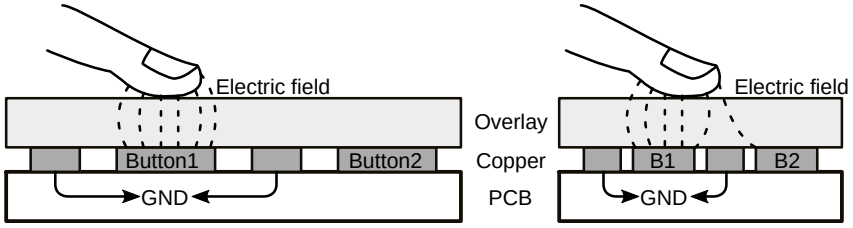


Figure 10. Placing Sensor Pads too close to each other can lead to False Touch Detection

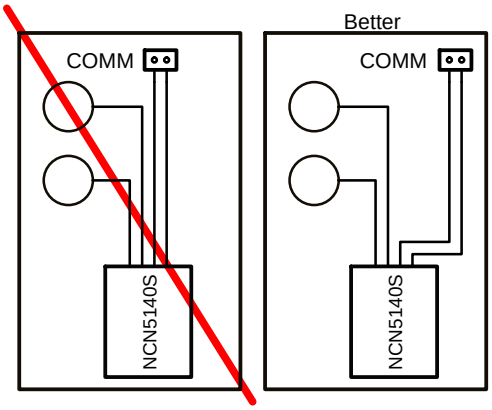


Figure 11. Recommended Ways to route Switching and Communication Signals

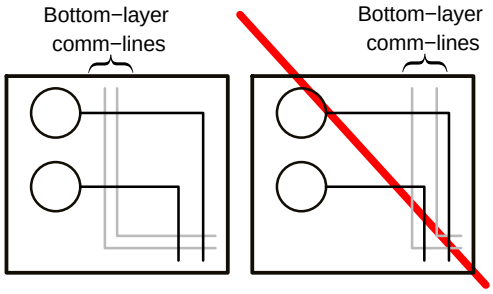


Figure 12. Crossing Sensing Signals on Different Layers

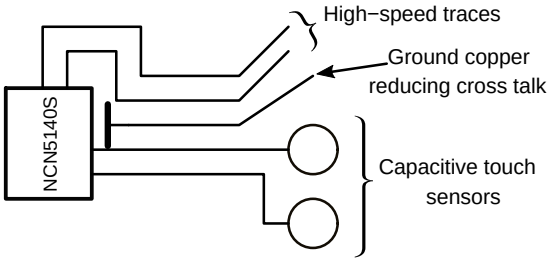


Figure 13. Running Ground Copper between High−speed Signals and a Sensor Trace to reduce Crosstalk

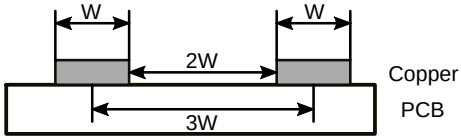


Figure 14. Illustration of the 3 W Rule used to minimize Crosstalk

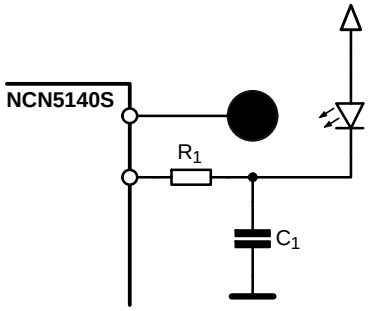


Figure 15. Adding a Low Pass Filter in a Switching LED Signal to reduce Crosstalk

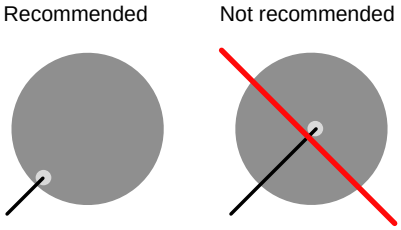


Figure 16. Recommended Placement of the Vias to reduce Trace Lengths

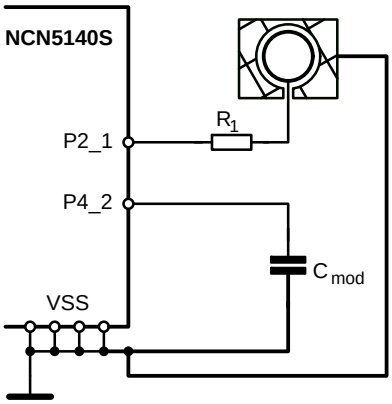


Figure 17. Schematic Representation of connecting the Different Grounds at a Single Star Point

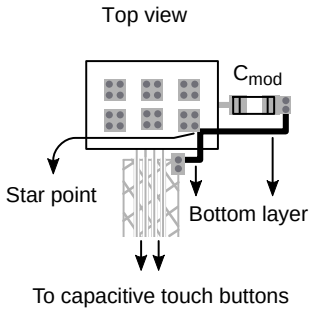


Figure 18. Capacitive Touch related Grounds Star Connected under the Chip

Ground Plane

A proper design of the necessary ground planes is crucial for a proper operation of the device. Strictly follow the guidelines below.

- The tracks going to the sensor buttons and the buttons itself should be surrounded by a hatched ground plane. Use a 25% hatching (0.178 mm line, 1.143 mm spacing) on the top layer and 17% (0.178 mm line, 1.778 mm spacing) on the bottom layer.
- Fill other parts of the board with solid copper connected to ground as much as possible.
- Stitch the ground copper on the different layers to the solid ground plane as much as possible. Good stitching is required to lower the ground inductance and brings the chip ground closer to the supply ground. This is really important as high current sinking can cause ground shifts.
- Make sure that the capacitive sensing ground planes are all connected to a central point (star topology). This includes the hatched ground planes surrounding the buttons and the ground connection of the C_{MOD} integrating capacitor. Figure 17 and Figure 18 show how this can be done for the NCN5140S.

All ground planes related to the capacitive touch sensing, should have an inductance of less than 0.2 nH from the central point. To achieve this, place the C_{MOD} as close as possible to the chip and keep their ground planes thick enough.

The ground connection of the C_{mod} capacitor and the ground hatches must first be routed to the four bottom ground pads of the NCN5140S as shown in Figure 18. Then everything can be connected to the rest of the ground copper. When using a top and bottom hatch, only one of the two is routed to the central pads. Both hatches are via stitched together.

Series Resistors on Capacitive Touch Pins

Every pin used for capacitive touch sensing has some parasitic capacitance C_P associated with it. Adding an external resistor in series with the sensor pad, forms a low-pass RC-filter as shown in Figure 19. This filter attenuates RF noise that is coupled into the capacitive touch trace. The low-pass filter will also reduce RF emissions coming from the pin.

These series resistors should be placed close to the device pins to filter the radiated noise picked up by the PCB traces at the input of the device. It is recommended to place the resistors within 10 mm of the device pins.

For regular FR-4 PCBs the recommended resistor value is 560 Ω. Increasing the resistance, also increases the time constant of the switched-capacitor circuit that converts C_P into an equivalent resistor. If the series resistance is larger than 560 Ω, the slower time constant of the switching circuit suppresses the emissions and interference, but limits the amount of charge that can be transferred. This lowers the signal level, which in turn lowers the SNR. Smaller values are better in terms of SNR, but are less effective at blocking RF interference.

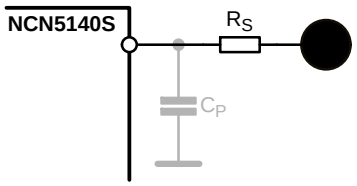


Figure 19. A Series Resistor on the Capacitive Touch Pin forms a Low-pass Filter with the Parasitic Capacitance

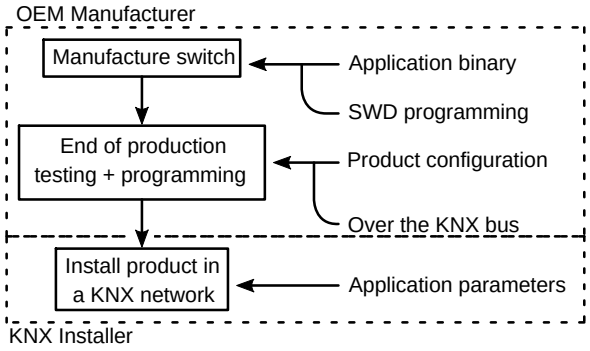


Figure 20. Production Flow of a KNX Switch using the NCN5140S

KNX STACK AND APPLICATION SOFTWARE

The NCN5140S is being supplied as a blank device and needs to be flashed during production. A binary containing a fully-certified KNX stack and application software is downloadable from the ON Semiconductor website. This binary enables building switch applications with up to 8 capacitive touch/tactile buttons and RGB LEDs with a very short time-to-market.

The included stack is the NGS Compact stack from Weinzierl Engineering GmbH and supports configuring of the device through ETS in System Mode[3]. In System Mode the customer has maximum flexibility when configuring the device.

On top of the NGS Compact stack runs a KNX switch application program developed by Weinzierl Engineering GmbH. The complete program is being supplied as a single binary file. This binary can be used in conjunction with the certified hardware designs offered by ON Semiconductor. It is possible to configure the certified hardware designs to your needs. This configuration is limited to the amount of buttons which are used (1 to 8) and the layout of the buttons. Refer to the manual of the boards for more information.

Programming the Device

As the NCN5140S is delivered as a blank device, it must be flashed during the production of the application.

Only two pins (SWDIO and SWDCLK) are required to program the device through the SWD-interface. This allows for a small programming connector on the PCB (5-pins connector minimum).

For mass production the connector could be replaced with SMD pads. These can be used in combination with a pogo pin programming setup to minimize BoM cost and PCB size.

Refer to the evaluation boards manual for more information on programming the device.

Configuring the Device

Programming the end of production configuration into the device is done over the KNX bus. These configuration parameters include the device serial number, amount of buttons used,... For a complete list of all the parameters refer to the evaluation board manual.

ETS Database

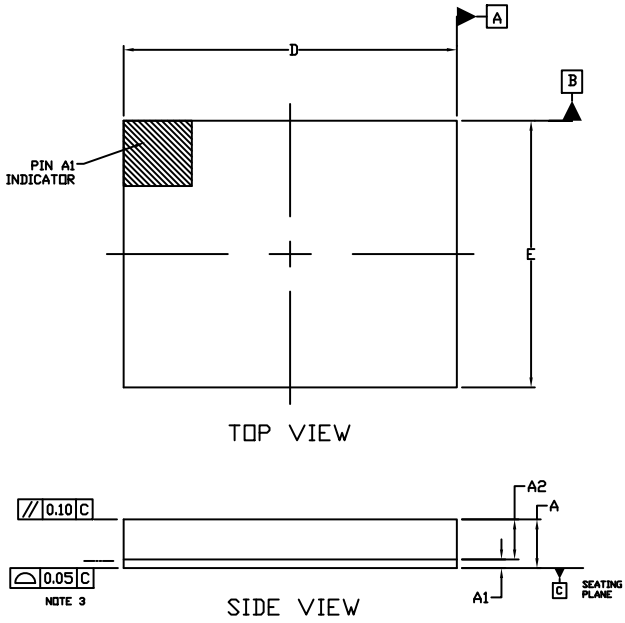
When the device is installed in the field the customization is done through ETS. This installation is done by a certified installer. The installer will program the group objects, used to control other devices in the network, and other parameters such as LED colors into the device. For more information on all the available group objects/settings refer to the installers manual.

The ETS database can be adjusted to include the product manufacturers logo and to include an adjusted description and pictures of the final product.

[3] Refer to the KNX standard for the different configuration modes.

PACKAGE DIMENSIONS

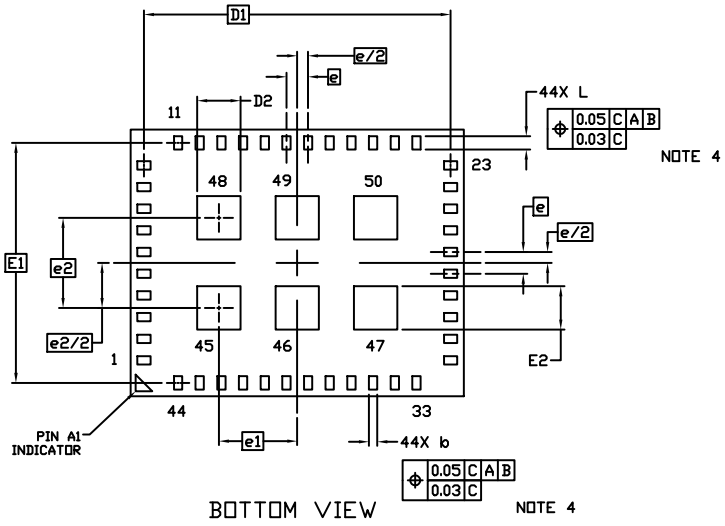
SIP50, 10x8
CASE 127FD
ISSUE O

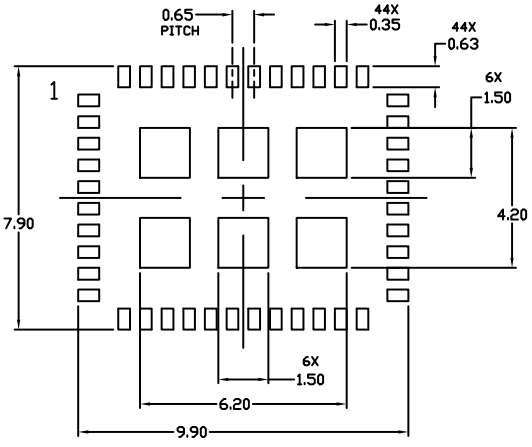


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE PADS.
3. POSITIONAL TOLERANCE APPLIES TO ALL OF THE PADS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.40	1.46	1.52
A1		0.26 REF	
A2	1.16	1.20	1.24
b	0.20	0.25	0.30
D	9.90	10.00	10.10
D1		9.20 BSC	
D2	1.25	1.30	1.35
E	7.90	8.00	8.10
E1		7.20 BSC	
E2	1.25	1.30	1.35
e		0.65 BSC	
e1		2.35 BSC	
e2		2.70 BSC	
L	0.35	0.40	0.45





PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

ON Semiconductor Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

onsemi:

NCN5140SG NCN5140STXG