NB3N121K

3.3V Differential 1:21 Fanout Clock and Data Driver with HCSL Outputs

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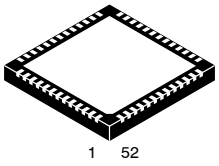


QFN−52
MN SUFFIX
CASE 485M

Description

The NB3N121K is a differential 1:21 Clock and Data fanout buffer with High−speed Current Steering Logic (HCSL) outputs optimized for ultra low propagation delay variation. The NB3N121K is designed with HCSL PCI Express clock distribution and FBDIMM applications in mind.

Inputs can directly accept differential LVPECL, HCSL, and LVDS signals per Figures 7, 8, and 9. Single ended LVPECL, HCSL, LVCMOS, or LVTTL levels are accepted with a proper external V_{th} reference supply per Figures 4 and 10. Input pins incorporate separate internal 50 Ω termination resistors allowing additional single ended system interconnect flexibility.

Output drive current is set by connecting a 475 Ω resistor from IREF (Pin 1) to GND per Figure 6. Outputs can also interface to LVDS receivers when terminated per Figure 11.

The NB3N121K specifically guarantees low output−to−output skew. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB3N121K's performance to distribute low skew clocks across the backplane or the motherboard.

Features

- Typical Input Clock Frequency 100, 133, 166, 200, 266, 333 and 400 MHz
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- 100 ps Max Within Device Skew
- 150 ps Max Device−to−Device Skew
- Δtpd 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- 0.1 ps Typical RMS Additive Phase Jitter
- LVDS Output Levels Optional with Interface Termination
- Operating Range: V_{CC} = 3.0 V to 3.6 V with GND = 0 V
- Typical HCSL Output Level (700 mV Peak−to−Peak)
- These are Pb−Free Devices

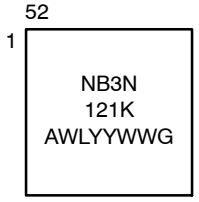
Applications

- Clock Distribution
- PCIe I, II, III
- Networking
- High End Computing
- Routers

End Products

- Servers
- FBDIMM Memory Card

MARKING DIAGRAM*



A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

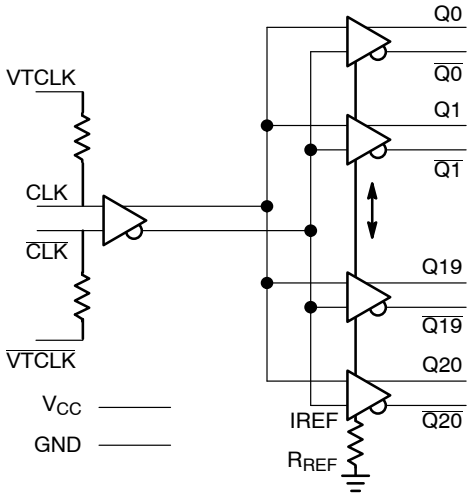


Figure 1. Simplified Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

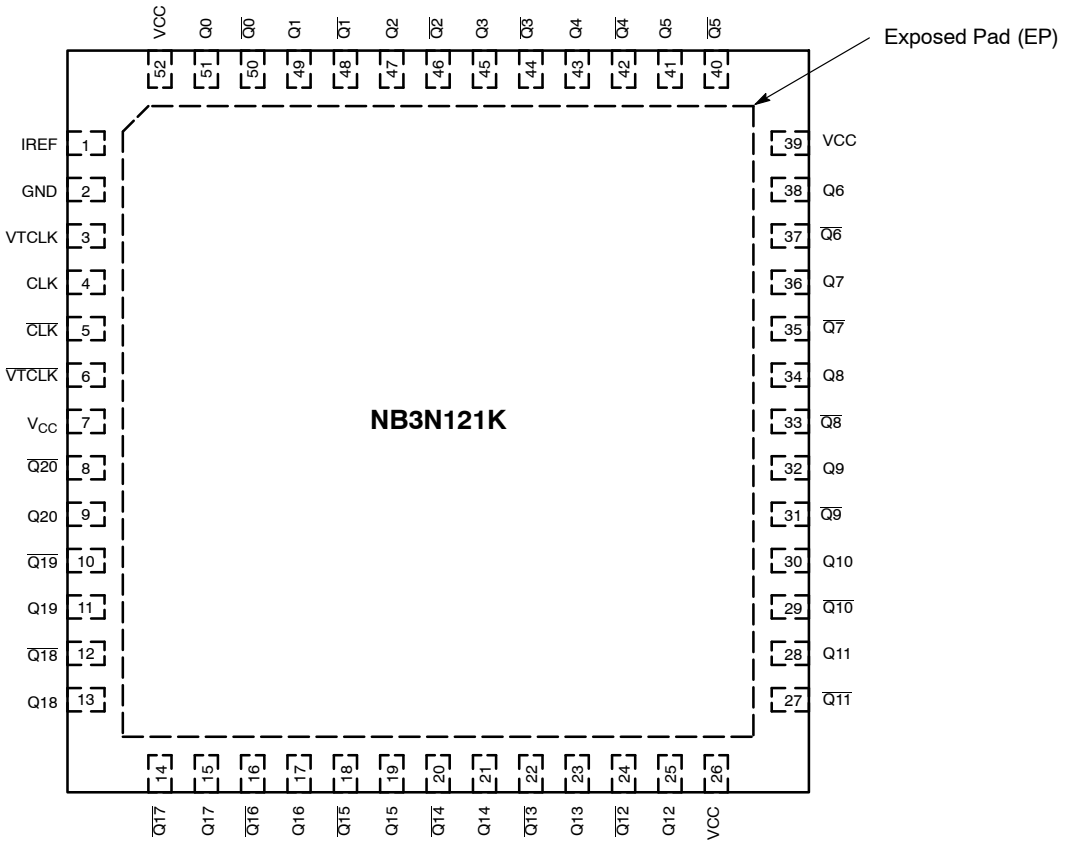


Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	IREF	Output	Use the IREF pin to set the output drive. Connect a 475 Ω RREF resistor from the IREF pin to GND to produce 2.63 mA of IREF current. A current mirror multiplies IREF by a factor of 5.4 to force 14.2 mA through a 50 Ω output load. See Figures 6 and 12. Minimize capacitance.
2	GND	–	Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation.
3, 6	VTCLK, $\overline{\text{VTCLK}}$	–	Internal 50 Ω Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self−oscillation.
4	CLK	LVPECL, HCSL, LVCMOS or LVTTL Input	Clock (TRUE) Input
5	$\overline{\text{CLK}}$	LVPECL, HCSL, LVCMOS or LVTTL Input	Clock (INVERT) Input
7, 26, 39, 52	VCC	–	Positive Supply pins. VCC pins must be externally connected to a power supply to guarantee proper operation.
8, 10, 12, 14, 16, 18, 20, 22, 24, 27, 29, 31, 33, 35, 37, 40,42, 44, 46, 48, 50	$\overline{\text{Q[20−0]}}$	HCSL or LVDS (Note 1) Output	Output (INVERT) (Note 1)
9, 11, 13, 15, 17, 19, 21, 23, 25, 28, 30, 32, 34, 36, 38, 41, 43, 45, 47, 49, 51	Q[20−0]	HCSL or LVDS (Note 1) Output	Output (TRUE) (Note 1)
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat−sinking conduit for proper thermal operation. The pad is electrically connected ot GND and must be connected to GND on the PC board.

1. Outputs can also interface to LVDS receiver when terminated per Figure 11.

Table 2. ATTRIBUTES

Characteristic		Value
ESD Protection	Human Body Model Machine Model	>2 kV 200 V
Moisture Sensitivity (Note 2)	QFN−52	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		409
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Positive Input	GND = 0 V		GND − 0.3 ≤ V_I ≤ V_{CC}	V
I_{OUT}	Output Current	Continuous Surge		50 100	mA mA
T_A	Operating Temperature Range	QFN−52		−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 lfpm 500 lfpm	QFN−52 QFN−52	25 19.6	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 4)	QFN−52	21	°C/W
T_{sol}	Wave Solder Pb−Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 4. DC CHARACTERISTICS (V_{CC} = 3.0 V to 3.6 V, T_A = −40°C to +85°C Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
I_{GND}	GND Supply Current (All Outputs Loaded)		120	150	mA
I_{CC}	Power Supply Current (All Outputs Loaded)		440	500	mA
I_{IH}	Input HIGH Current		2.0	150	μA
I_{IL}	Input LOW Current	−150	−2.0		μA
R_{TIN}	Internal Input Termination Resistor	45	50	55	Ω
DIFFERENTIAL INPUT DRIVEN SINGLE − ENDED (See Figures 4 and 5)					
V_{th}	Input Threshold Reference Voltage Range (Note 6)	350		V_{CC} − 1000	mV
V_{IH}	Single−Ended Input HIGH Voltage	V_{th} + 150		V_{CC}	mV
V_{IL}	Single−Ended Input LOW Voltage	GND		V_{th} − 150	mV
DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 7, 8 and 9)					
V_{IHD}	Differential Input HIGH Voltage	425		V_{CC} − 850	mV
V_{ILD}	Differential Input LOW Voltage	GND		V_{CC} − 1000	mV
V_{ID}	Differential Input Voltage (V_{IHD} − V_{ILD})	150		V_{CC} − 850	mV
V_{CMR}	Input Common Mode Range	350		V_{CC} − 1000	mV
HCSL OUTPUTS (Figure 4)					
V_{OH}	Output HIGH Voltage	600	740	900	mV
V_{OL}	Output LOW Voltage	−150	0	150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

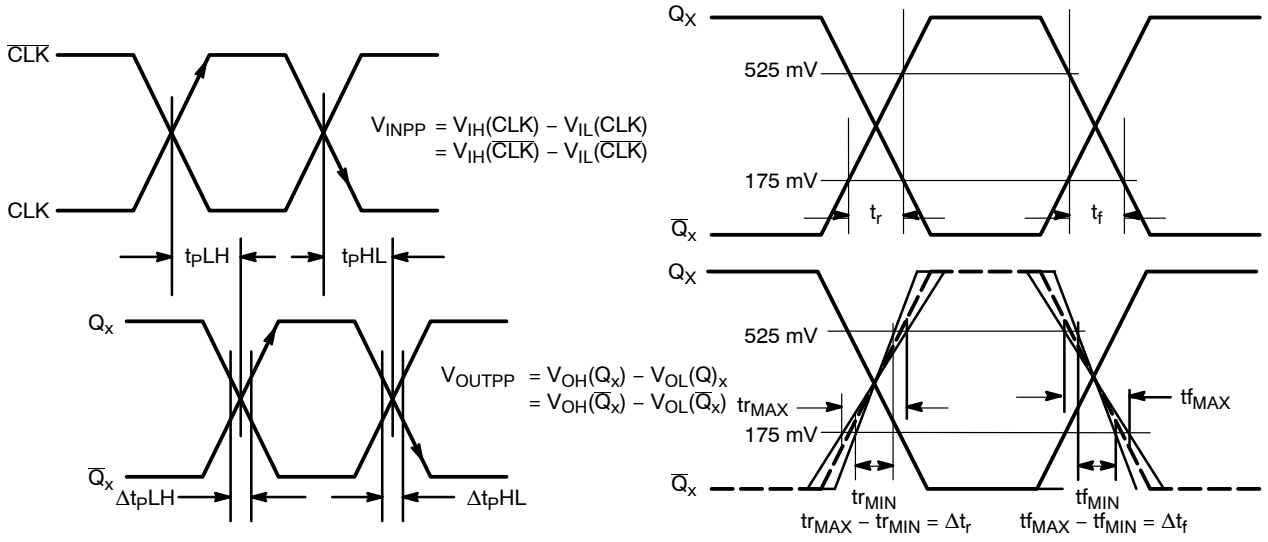
5. Measurements taken with with outputs loaded 50 Ω to GND. Connect a 475 Ω resister from IREF (Pin 1) to GND. See Figure 6.
6. V_{th} is applied to the complementary input when operating in single ended mode per Figure 4.

Table 5. AC CHARACTERISTICS V_{CC} = 3.0 V to 3.6 V, GND = 0 V; −40°C to +85°C (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \le 400$ MHz		725	1000	mV
t_{PLH}, t_{PHL}	Propagation Delay (See Figure 3a) CLK/$\overline{CLK}$ to Qx/$\overline{Qx}$	550	800	950	ps
Δt_{PLH}, Δt_{PHL}	Propagation Delay Variations Per Each Diff Pair (Note 8) (See Figure 3a) CLK/$\overline{CLK}$ to Qx/$\overline{Qx}$			100	ps
t_{SKEW}	Duty Cycle Skew (Note 9) Within -Device Skew Device to Device Skew (Note 10)			20 100 150	ps
t_{JIT}	Additive RMS Phase Jitter (Note 11) F_{in} = 100 MHz		0.1		ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration)	150		V_{CC} − 850	mV
V_{CROSS}	Absolute Crossing Magnitude Voltage (See Figure 3c)	250		550	mV
ΔV_{CROSS}	Variation in Magnitude of V_{CROSS} (See Figure 3c)			150	mV
t_r , t_f	Absolute Magnitude in Output Risetime and Falltime (from 175 mV to 525 mV) (See Figure 3b) Qx, $\overline{Qx}$	100	340	700	ps
Δtr, Δtf	Variation in Magnitude of Risetime and Falltime (Single−Ended) (See Figure 3b) Qx, $\overline{Qx}$			125	ps

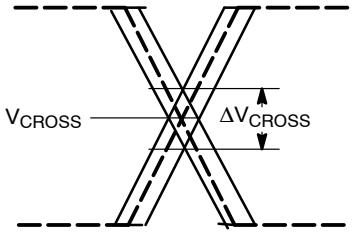
NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. Connect a 475 Ω resister from IREF (Pin 1) to GND. All outputs loaded 50 Ω to GND per Figure 6.
8. Measured from the input pair crosspoint to each single output pair crosspoint across temp and voltage ranges per Figure 3.
9. Duty cycle skew is measured between differential outputs using the deviations of the sum of Tpw- and Tpw+.
10. Skew is measured between outputs under identical conditions @ 50 MHz.
11. Phase noise integrated from 12 kHz to 20 MHz



(a) Propagation Delay and Propagation Delay Variation

(b) tr, tf and Δtr, Δtf



(c) VCROSS and ΔVCROSS

Figure 3. AC Reference Measurement

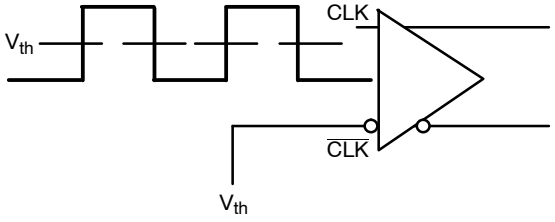


Figure 4. Single−Ended Interconnect V_{th} Reference Voltage

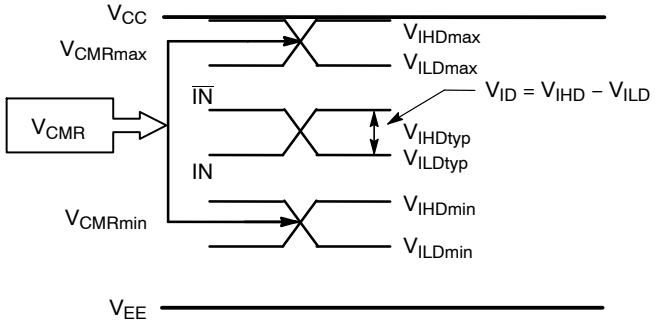
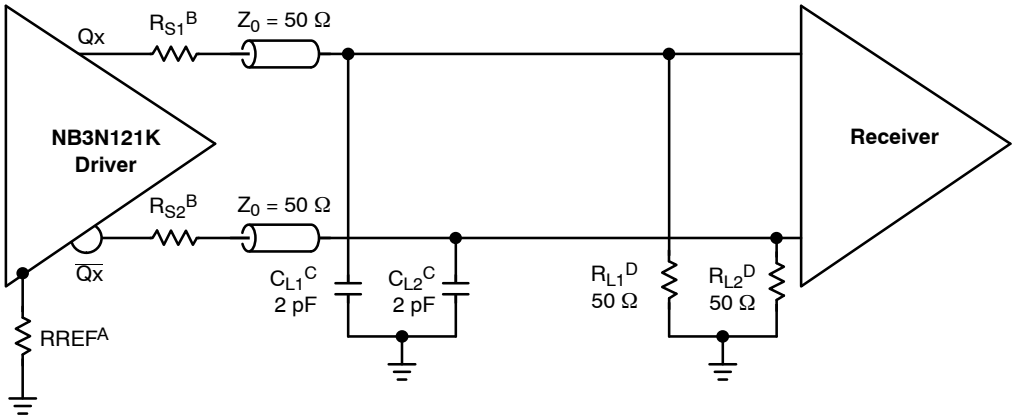
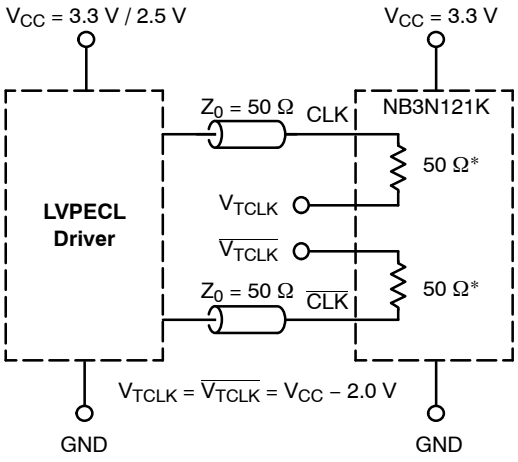


Figure 5. V_{th} Diagram



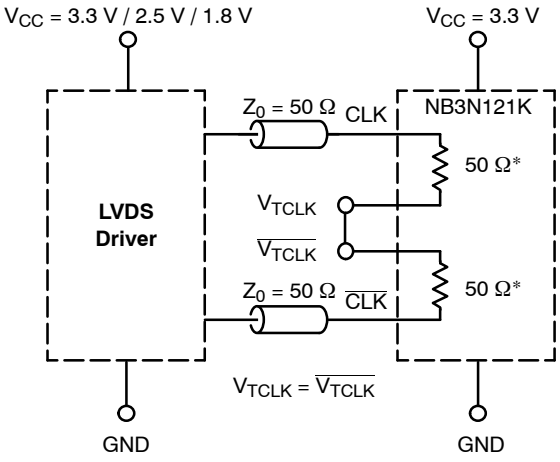
A. Connect 475 Ω resistor RREF from IREF pin to GND.
B. R_{S1}, R_{S2}: 0 Ω for Test and Evaluation. Select to Minimizing Ringing.
C. C_{L1}, C_{L2}: Receiver Input Simulation (for test only not added to application circuit.
D. R_{L1}, R_{L2} Termination and Load Resistors Located at Receiver Inputs.

Figure 6. Typical Termination Configuration for Output Driver and Device Evaluation



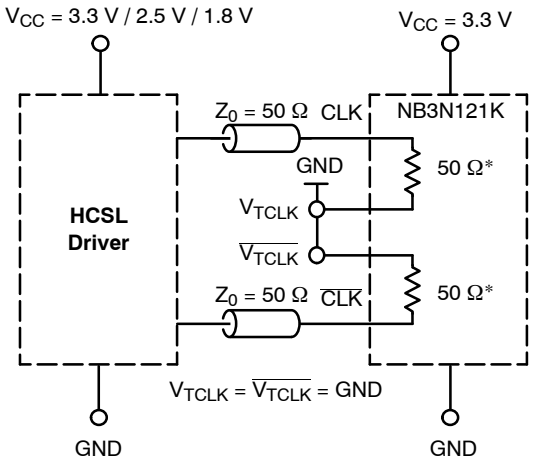
*RTIN, Internal Input Termination Resistor

Figure 7. LVPECL Interface



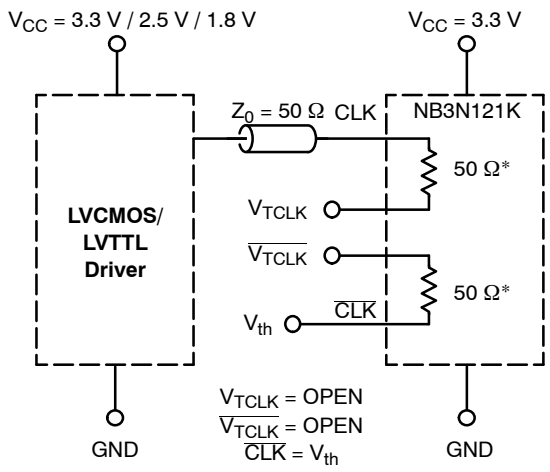
*RTIN, Internal Input Termination Resistor

Figure 8. LVDS Interface



*RTIN, Internal Input Termination Resistor

Figure 9. Standard 50 Ω Load HCSL Interface



*RTIN, Internal Input Termination Resistor

Figure 10. LVCMOS/LVTTL Interface

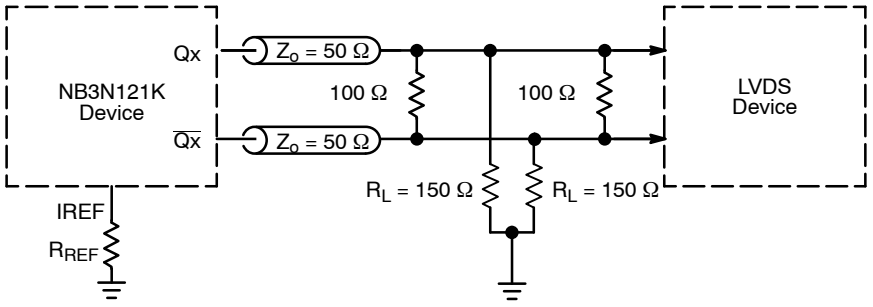


Figure 11. HCSL Interface Termination to LVDS

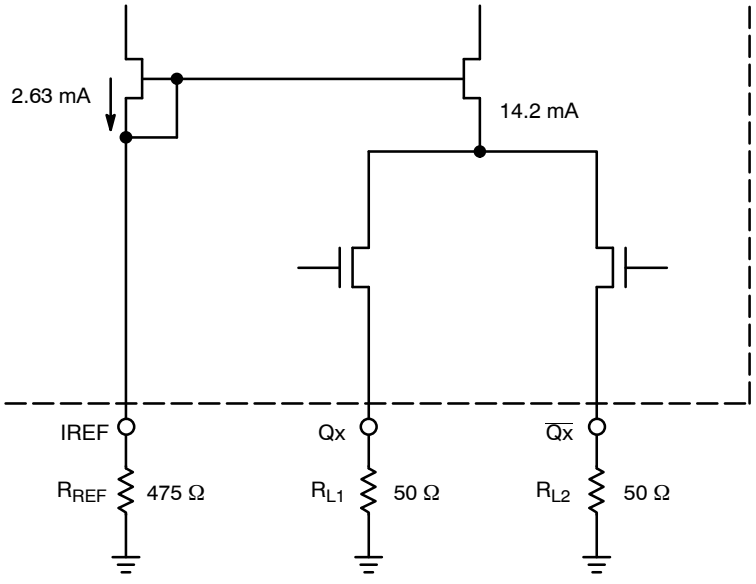


Figure 12. Simplified HCSL Output Structure

ORDERING INFORMATION

Device	Package	Shipping†
NB3N121KMNG	QFN−52 (Pb−Free)	260 Units / Tray
NB3N121KMNR2G	QFN−52 (Pb−Free)	2000 / Tape & Reel

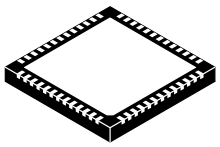
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

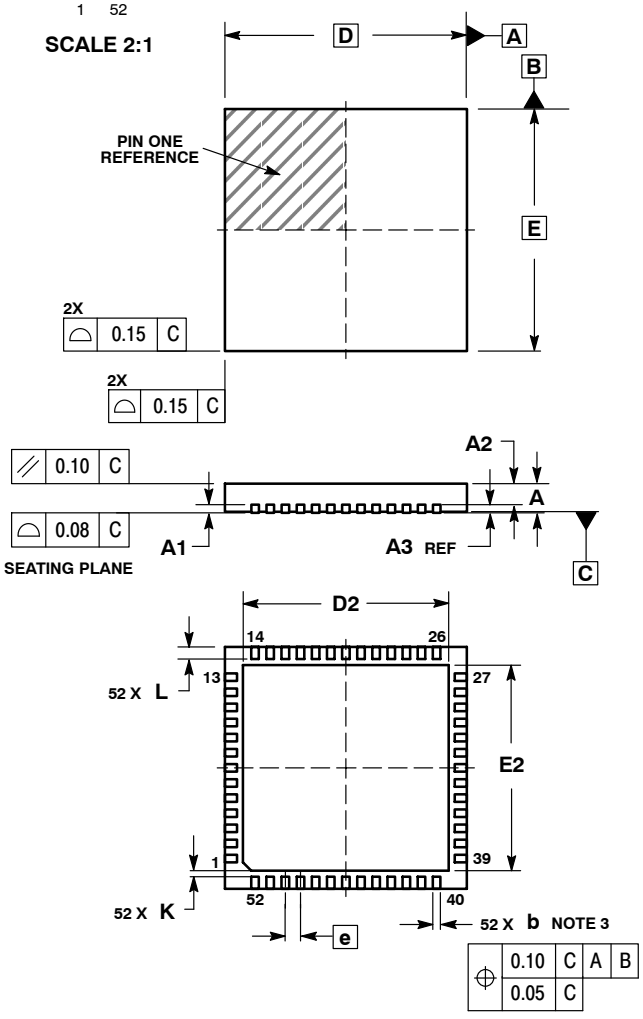
ON Semiconductor®

QFN52 8x8, 0.5P
CASE 485M−01
ISSUE C

DATE 16 FEB 2010



SCALE 2:1



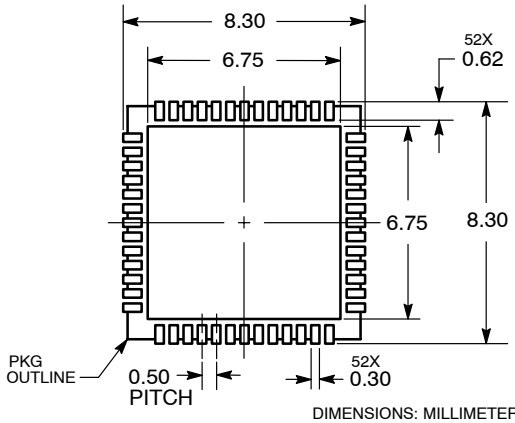
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

GENERIC MARKING DIAGRAM

XXXXXXXXX	= Device Code
A	= Assembly Site
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

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DESCRIPTION:	**52 PIN QFN, 8X8, 0.5P**	**PAGE 1 OF 1**

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