

MT9M114_55CSP_Demo3_Headboard

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Rev	Who	Date	Description
Rev 0.0	jwrede	10/06/2014	Base Schematic for Custom Design
Rev 0.1	aralex	09/22/2015	- Design is based from MT9M114 CSP package Demo2 Rev1 board - Added Feedback clock to Demo3 circuitry
		09/30/2015	-Removed TP3 and TP4 : I2C test points -Removed C50, C51, C59, C60 decaps for 5V and 1.2V, Added TP7
		10/01/2015	-Removed I2C Debug Circuitry, C65 - Implemented the Master slave configuration as per that used in AR1335 HB
		10/07/2015	-Updated with review comments -Removed short in EEPROM section, corrected VDD and VDDIO nets near sensor, R2 deleted, changed voltage of RESET ckt from 3.3V to VDDIO_LS
			-Updated U3 from 24LC64-I/SN to 24FC64-I/SN -Changed net names from OE_N to OE_L; SEN_RST_N to SEN_RST_L
			-Swapped the power headers for layout: JP4, JP5, JP6, JP7, JP8
		10/07/2015	-Updated block diagram -changed R3 from 0603 to 0402 -changed C1, C30 from 0603 to 0402 [For BOM consolidation]
		10/08/2015	-changed C37 manf Murata to Panasonic (0402) [For BOM consolidation] - Changed the Master slave circuit connections to cater to multi slave configuration, instead of one master and one slave
		10/09/2015	-Changed revision to 0.1, to keep BOM at same revision Changed note for P2 as per review comment by Shawyee (sync note)
		10/12/2015	Swapped pin connections on JP4, JP7, JP8 as per Joe's feedback to maintain uniformity between jumper power nets
		10/13/2015	Updated the Mutlicamera Configuration, I2C Daisy Chain and Clock chain Block Diagrams

		
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Block Diagram



SENSOR MT9M114_55CSP PINOUT

	1	2	3	4	5	6	7	8
A	VAA	Reserved ¹	DOUT[6]	Dout[4]	Dout[2]	VDD	Dout[1]	VDD
B	GND	VAA	VDD_IO	Dout[5]	Dout[3]	GND	Dout[0]	VDD_IO
C	VDD	OE_BAR	AGND	GND	VDD_IO	FV	LV	
D	CONFIG	SCLK	SDATA	DOUT[7]	Reserved ¹	DOUT_LSB1	GND	VDD
E	VDD_IO	CHAIN	Reserved ¹	SADDR	RESET_BAR	DOUT_LSB0	GND	Vdd_PHY
F	EXTCLK	PIXCLK	GND	TRST_BAR	DATA_N	DATA_P	CLK_P	CLK_N
G	VDD	FLASH	VDD	PGND ²	PGND ²	VDD_PLL	GND_PLL	GND_PLL



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Title

Pinout

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MT9M114_55CSP_Demo3_Headboard

0.1

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Friday, October 09, 2015

Sheet

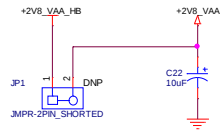
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of

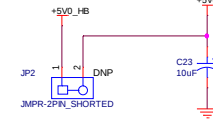
8

Power Supply

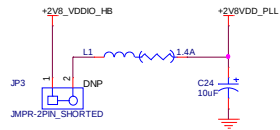
2.8V VAA Power supply



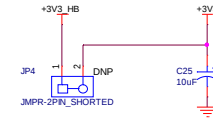
Peripheral 5V Power Supply



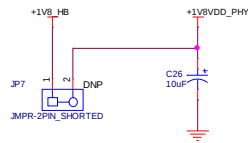
VDD_PLL Power Supply



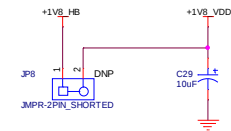
Peripheral 3.3V Supply



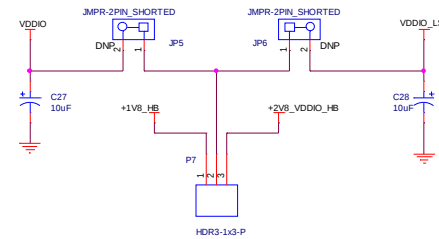
VDD-PHY Power Supply



VDD Power Supply

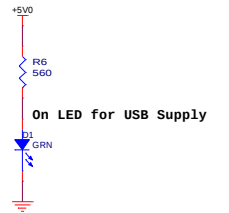


VDDIO & VDDIO_LS 1.8V/ 2.8VSupply

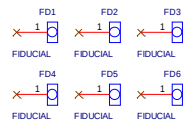


P7 Default Setting: 1-2 Short (1V8 operation)

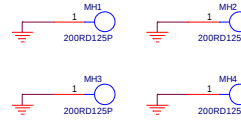
Layout: Mount
LED on bottom
side of PCB



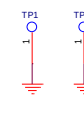
Fiducials



Mounting Holes



Ground Testpoints

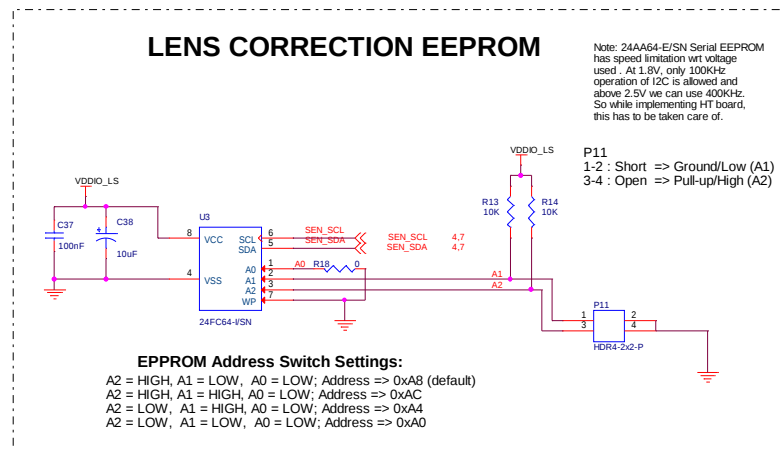
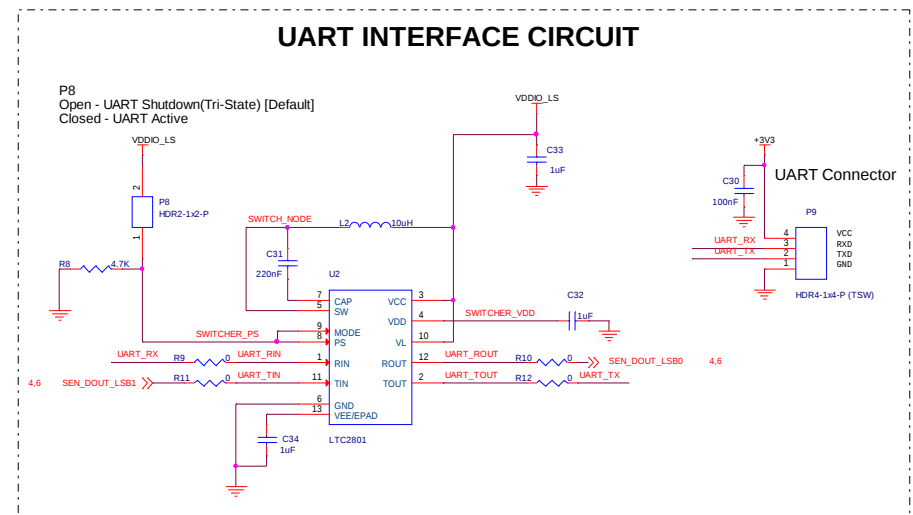
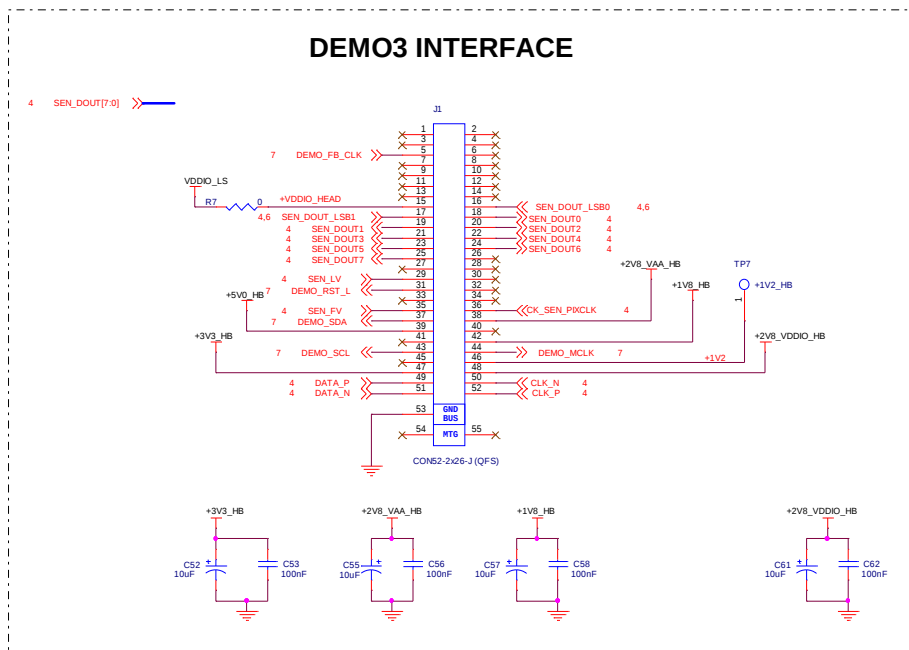


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Power Supply		
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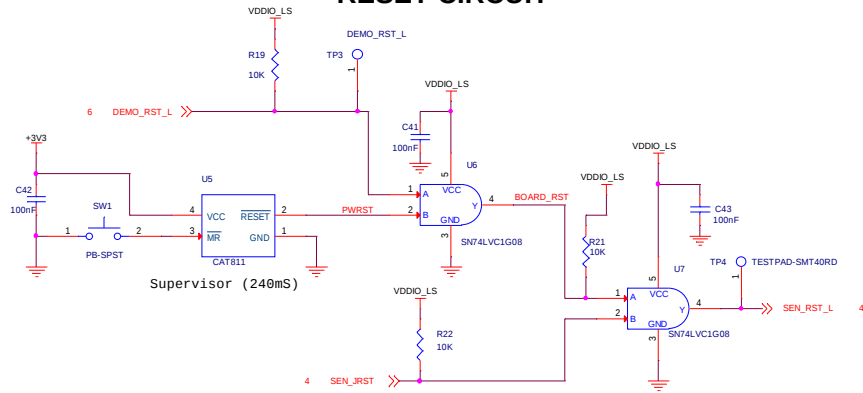
4,5,7 VDDIO_LS 5,7 +3V3

4,5,7 GND

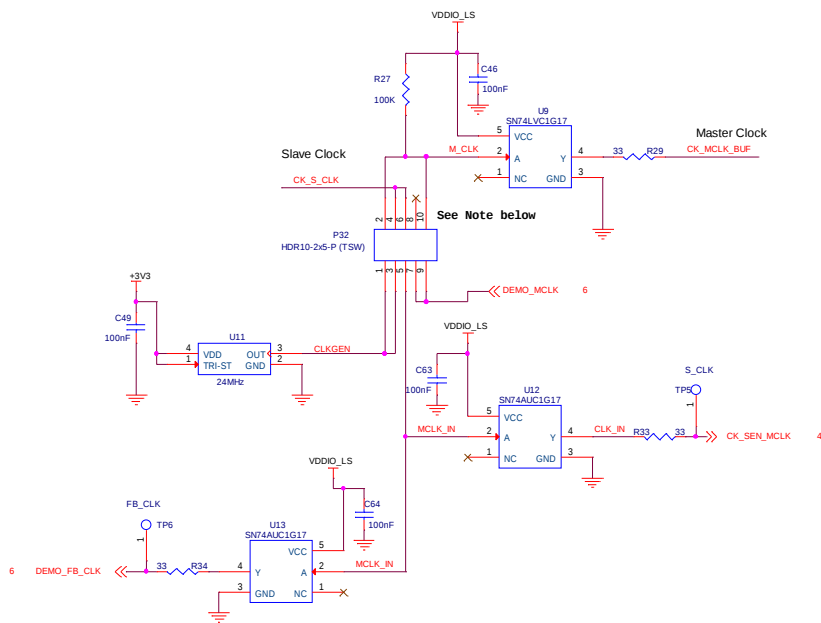


Clock & Reset

RESET CIRCUIT

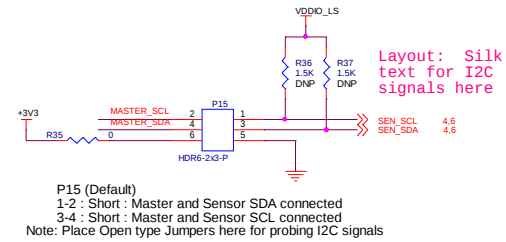


CLOCK CIRCUIT

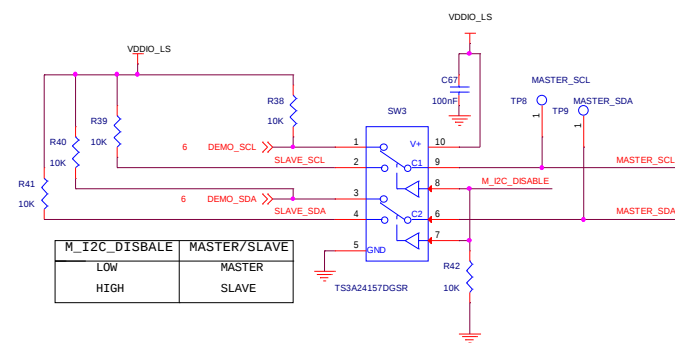


NOTE: P32 Oscillator Configurations
 3-5 -> Normal Single Camera Operation, using on board oscillator.
 5-7 -> Normal Single Camera Operation, using external clock from Demo3.
 3-5 & 1-2 -> Master in Multi-Camera Operation, oscillator to Slave Cameras (Default)
 5-6 -> Slave in Multi-Camera Operation, oscillator from Master Camera.
 5-6 & 2-4 -> Multi Slave in Multi-Camera Operation, oscillator from Master Camera.
 5-7 & 9-10 -> Master in Multi-Camera Operation, using external clock from Demo3.

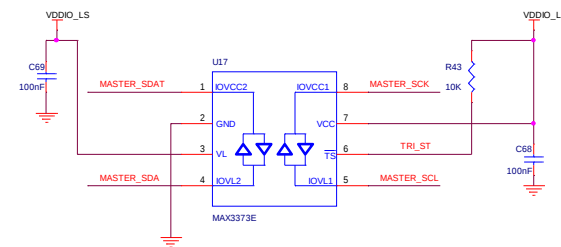
Multi-Camera Interface



I2C Selection Switch for Master



I2C Repeater for Master Slave Config

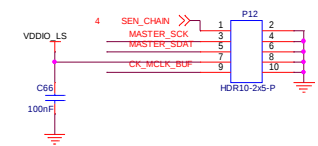


Master or Multi Slave Camera modes

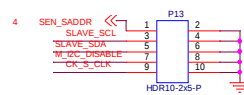
- 1) Single Mode, No connection on both Master(P12) and Slave (P13)Connector
- 2) Multi-Camera Slave Mode, Slave Connector(P13) be connected to the Master Connector(P12) of Master Unit
- 3) Master Mode, Connect Master Connector(P12) to the Slave Connector(P13) of Slave Unit. No connection on the Master Unit's Slave Connector.



Master

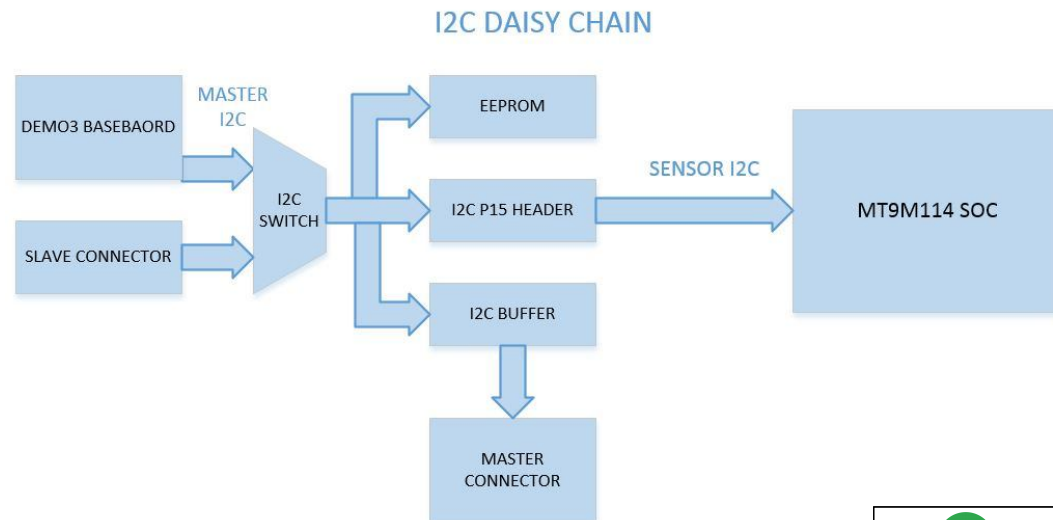
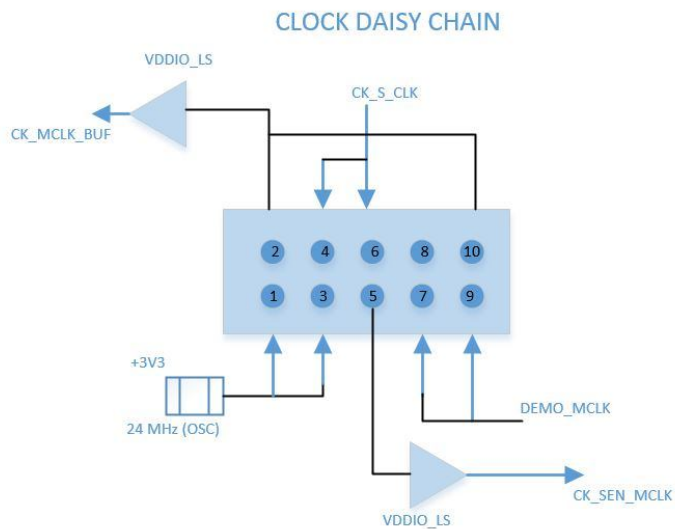
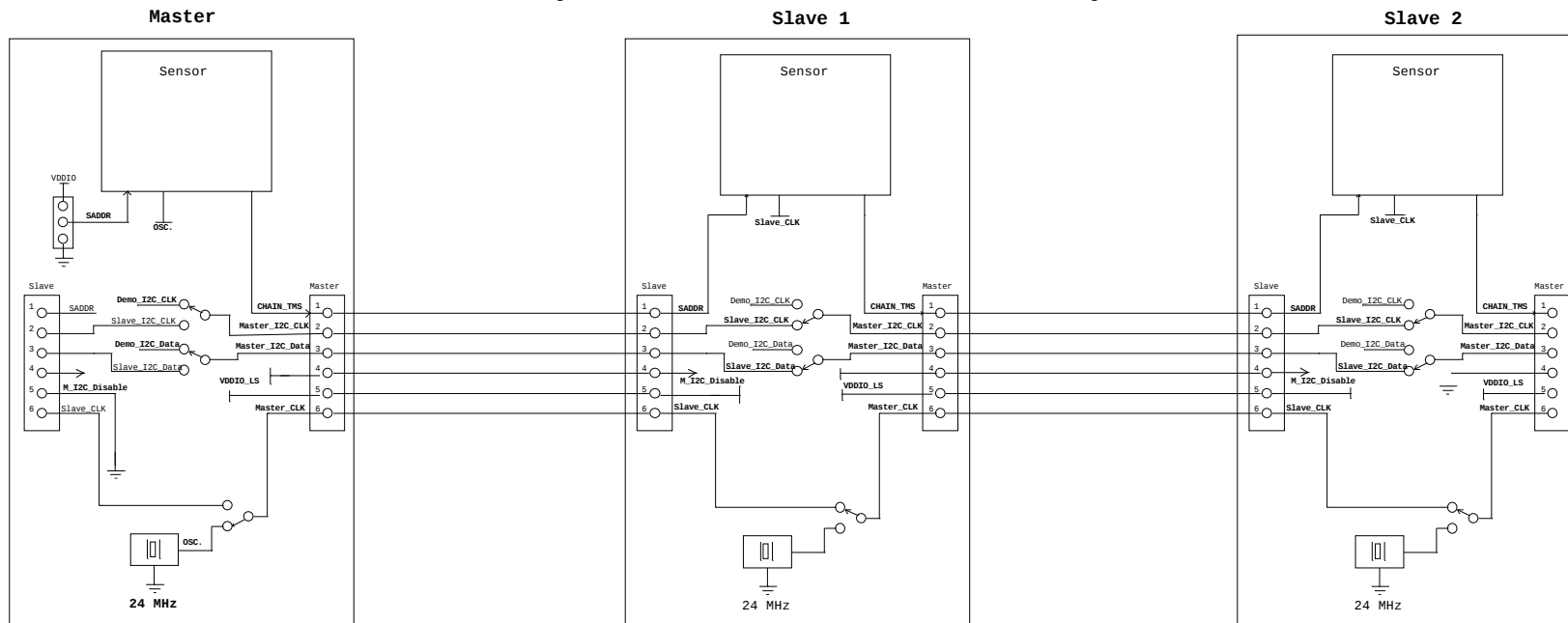


Slave



Multi-Camera Configuration

Block diagram below shows cameras in a Multi-Camera Configuration



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