

MC74AC153, MC74ACT153

Dual 4-Input Multiplexer

The MC74AC153/74ACT153 is a high-speed dual 4-input multiplexer with common select inputs and individual enable inputs for each section. It can select two lines of data from four sources. The two buffered outputs present data in the true (non-inverted) form. In addition to multiplexer operation, the MC74AC153/74ACT153 can act as a function generator and generate any two functions of three variables.

- Outputs Source/Sink 24 mA
- 'ACT153 Has TTL Compatible Inputs
- These are Pb-Free Devices

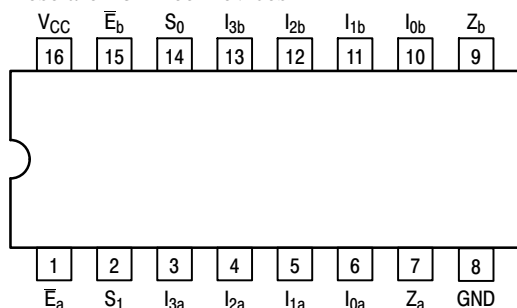


Figure 1. Pinout: 16-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION
I _{0a} –I _{3a}	Side A Data Inputs
I _{0b} –I _{3b}	Side B Data Inputs
S ₀ , S ₁	Common Select Inputs
E _a	Side A Enable Input
E _b	Side B Enable Input
Z _a	Side A Output
Z _b	Side B Output

TRUTH TABLE

Select Inputs		Inputs (a or b)						Output
S ₀	S ₁	E	I ₀	I ₁	I ₂	I ₃		Z
X	X	H	X	X	X	X		L
L	L	L	L	X	X	X		L
L	L	L	H	X	X	X		H
H	L	L	X	L	X	X		L
H	L	L	X	H	X	X		H
L	H	L	X	X	L	X		L
L	H	L	X	X	H	X		H
H	H	L	X	X	X	L		L
H	H	L	X	X	X	H		H

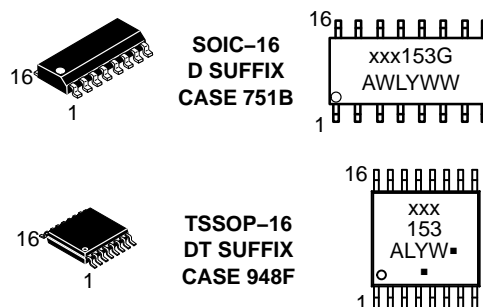
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial



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MARKING DIAGRAMS



xxx = AC or ACT
A = Assembly Location
WL or L = Wafer Lot
Y = Year
WW or W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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FUNCTIONAL DESCRIPTION

The MC74AC153/74ACT153 is a dual 4-input multiplexer. It can select two bits of data from up to four sources under the control of the common Select inputs (S_0 , S_1). The two 4-input multiplexer circuits have individual active-LOW Enables ($\overline{E}_a, \overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a, \overline{E}_b$) are HIGH, the corresponding outputs (Z_a, Z_b) are forced LOW. The MC74AC153/74ACT153 is the logic implementation of a 2-pole, 4-position switch, where the position of the switch is determined by the logic levels supplied to the two Select inputs. The logic equations for the outputs are shown below.

$$Z_a = \overline{E}_a \cdot (I_{0a} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1a} \cdot \overline{S}_1 \cdot S_0 + I_{2a} \cdot S_1 \cdot \overline{S}_0 + I_{3a} \cdot S_1 \cdot S_0)$$

$$Z_b = \overline{E}_b \cdot (I_{0b} \cdot \overline{S}_1 \cdot \overline{S}_0 + I_{1b} \cdot \overline{S}_1 \cdot S_0 + I_{2b} \cdot S_1 \cdot \overline{S}_0 + I_{3b} \cdot S_1 \cdot S_0)$$

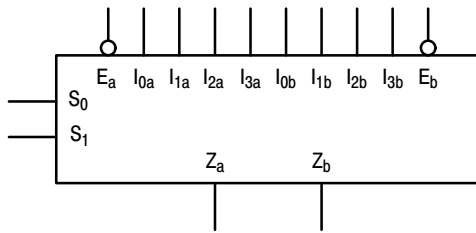
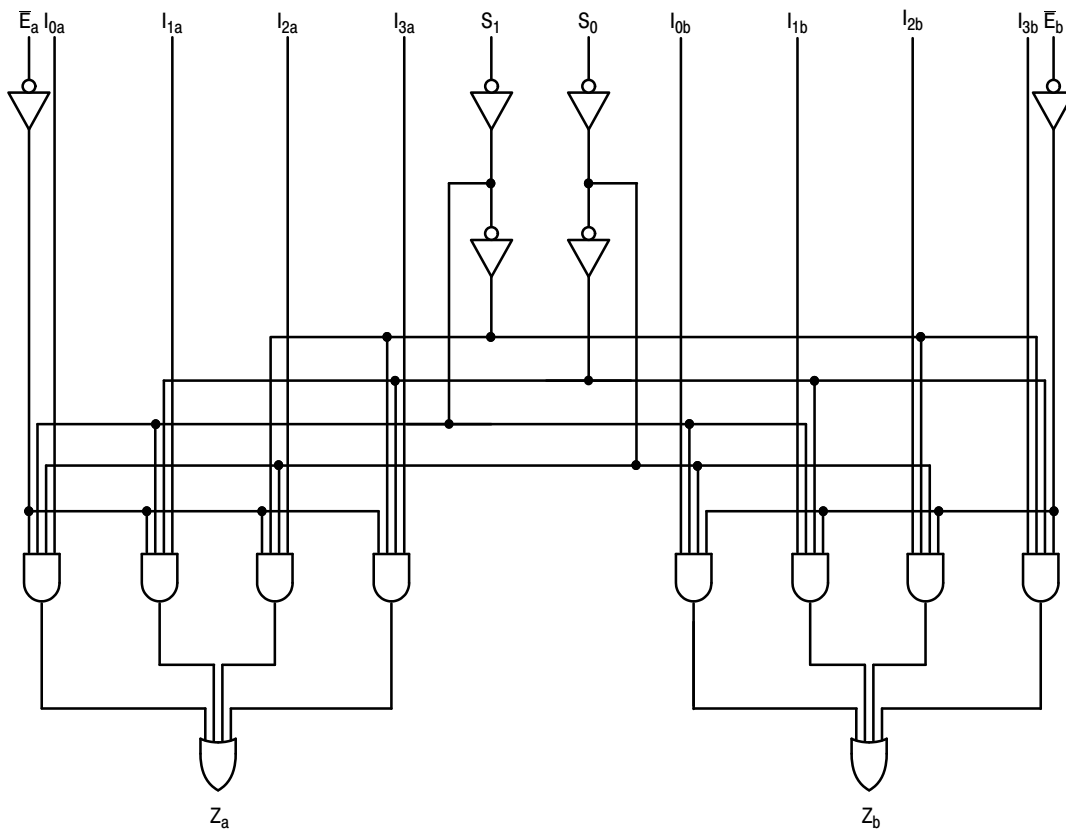


Figure 2. Logic Symbol



NOTE: This diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 3. Logic Diagram

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	− 0.5 to +7.0	V
V _I	DC Input Voltage	− 0.5 ≤ V _I ≤ V _{CC} + 0.5	V
V _O	DC Output Voltage (Note 1)	− 0.5 ≤ V _O ≤ V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	± 20	mA
I _{OK}	DC Output Diode Current	± 50	mA
I _O	DC Output Sink/Source Current	± 50	mA
I _{CC}	DC Supply Current per Output Pin	± 50	mA
I _{GND}	DC Ground Current per Output Pin	± 50	mA
T _{STG}	Storage Temperature Range	− 65 to + 150	°C
T _L	Lead temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction temperature under Bias	+ 150	°C
θ _{JA}	Thermal Resistance (Note 2) SOIC TSSOP	69.1 103.8	°C/W
P _D	Power Dissipation in Still Air at 65°C (Note 3) SOIC TSSOP	500 500	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 30% – 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 4) Machine Model (Note 5) Charged Device Model (Note 6)	> 2000 > 200 > 1000	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and Below GND at 85°C (Note 7)	± 100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.
2. The package thermal impedance is calculated in accordance with JEDEC51-7.
3. 500 mW at 65°C; derate to 300 mW by 10 mW/°C from 65°C to 85°C.
4. Tested to EIA/JESD22-A114-A.
5. Tested to EIA/JESD22-A115-A.
6. Tested to JESD22-C101-A.
7. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage	'AC	2.0	5.0	V
		'ACT	4.5	5.0	
V _{IN} , V _{OUT}	DC Input Voltage, Output Voltage (Ref. to GND)	0	–	V _{CC}	V
t _r , t _f	Input Rise and Fall Time (Note 1) 'AC Devices except Schmitt Inputs	V _{CC} @ 3.0 V	–	150	ns/V
		V _{CC} @ 4.5 V	–	40	
		V _{CC} @ 5.5 V	–	25	
t _r , t _f	Input Rise and Fall Time (Note 2) 'ACT Devices except Schmitt Inputs	V _{CC} @ 4.5 V	–	10	ns/V
		V _{CC} @ 5.5 V	–	8.0	
T _J	Junction Temperature (PDIP)	–	–	140	°C
T _A	Operating Ambient Temperature Range	–40	25	85	°C
I _{OH}	Output Current – High	–	–	–24	mA
I _{OL}	Output Current – Low	–	–	24	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. V_{IN} from 30% to 70% V_{CC}; see individual Data Sheets for devices that differ from the typical input rise and fall times.
2. V_{IN} from 0.8 V to 2.0 V; see individual Data Sheets for devices that differ from the typical input rise and fall times.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74AC		74AC		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	3.0	1.5	2.1	2.1		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	3.15	3.15			
		5.5	2.75	3.85	3.85			
V _{IL}	Maximum Low Level Input Voltage	3.0	1.5	0.9	0.9		V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V
		4.5	2.25	1.35	1.35			
		5.5	2.75	1.65	1.65			
V _{OH}	Minimum High Level Output Voltage	3.0	2.99	2.9	2.9		V	I _{OUT} = -50 μA
		4.5	4.49	4.4	4.4			
		5.5	5.49	5.4	5.4			
		3.0	–	2.56	2.46		V	*V _{IN} = V _{IL} or V _{IH} -12 mA I _{OH} -24 mA -24 mA
		4.5	–	3.86	3.76			
		5.5	–	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	3.0	0.002	0.1	0.1		V	I _{OUT} = 50 μA
		4.5	0.001	0.1	0.1			
		5.5	0.001	0.1	0.1			
		3.0	–	0.36	0.44		V	*V _{IN} = V _{IL} or V _{IH} 12 mA I _{OL} 24 mA 24 mA
		4.5	–	0.36	0.44			
		5.5	–	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	–	±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{OLD}	†Minimum Dynamic Output Current	5.5	–	–	75		mA	V _{OLD} = 1.65 V Max
I _{OHD}		5.5	–	–	-75		mA	V _{OHD} = 3.85 V Min
I _{CC}	Maximum Quiescent Supply Current	5.5	–	8.0	80		μA	V _{IN} = V _{CC} or GND

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

NOTE: I_{IN} and I_{CC} @ 3.0 V are guaranteed to be less than or equal to the respective limit @ 5.5 V V_{CC}.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74AC			74AC		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = −40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	3.3 5.0	2.5 2.0	9.5 6.5	15.0 11.0	2.5 2.0	17.5 12.5	ns	3–6
t _{PHL}	Propagation Delay S _n to Z _n	3.3 5.0	3.0 2.5	8.5 6.5	14.5 11.0	2.5 2.0	16.5 12.0	ns	3–6
t _{PLH}	Propagation Delay E _n to Z _n	3.3 5.0	2.5 1.5	8.0 5.5	13.5 9.5	2.0 1.5	16.0 11.0	ns	3–6
t _{PHL}	Propagation Delay E _n to Z _n	3.3 5.0	2.5 2.0	7.0 5.0	11.0 8.0	2.0 1.5	12.5 9.0	ns	3–6
t _{PLH}	Propagation Delay I _n to Z _n	3.3 5.0	2.5 1.5	7.5 5.5	12.5 9.0	2.0 1.5	14.5 10.5	ns	3–5
t _{PHL}	Propagation Delay I _n to Z _n	3.3 5.0	1.5 1.5	7.0 5.0	11.5 8.5	1.5 1.5	13.0 10.0	ns	3–5

*Voltage Range 3.3 V is 3.3 V ±0.3 V.

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

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DC CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	74ACT		74ACT		Unit	Conditions
			T _A = +25°C		T _A = -40°C to +85°C			
			Typ	Guaranteed Limits				
V _{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I _{OUT} = -50 μA	
		5.5	5.49	5.4	5.4			
		4.5	—	3.86	3.76	V	*V _{IN} = V _{IL} or V _{IH} -24 mA I _{OH} -24 mA	
		5.5	—	4.86	4.76			
V _{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I _{OUT} = 50 μA	
		5.5	0.001	0.1	0.1			
		4.5	—	0.36	0.44	V	*V _{IN} = V _{IL} or V _{IH} 24 mA I _{OL} 24 mA	
		5.5	—	0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5	—	±0.1	±1.0	μA	V _I = V _{CC} , GND	
ΔI _{CCT}	Additional Max. I _{CC} /Input	5.5	0.6	—	1.5	mA	V _I = V _{CC} - 2.1 V	
I _{OLD}	†Minimum Dynamic Output Current	5.5	—	—	75	mA	V _{OLD} = 1.65 V Max	
I _{OHD}		5.5	—	—	-75	mA	V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5	—	8.0	80	μA	V _{IN} = V _{CC} or GND	

*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS

Symbol	Parameter	V _{CC} * (V)	74ACT			74ACT		Unit	Fig. No.
			T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF			
			Min	Typ	Max	Min	Max		
t _{PLH}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.0	13.5	ns	3–6
t _{PHL}	Propagation Delay S _n to Z _n	5.0	3.0	7.0	11.5	2.5	13.5	ns	3–6
t _{PLH}	Propagation Delay E _n to Z _n	5.0	2.0	6.5	10.5	2.0	12.5	ns	3–6
t _{PHL}	Propagation Delay E _n to Z _n	5.0	3.0	6.0	9.5	2.5	11.0	ns	3–6
t _{PLH}	Propagation Delay I _n to Z _n	5.0	2.5	5.5	9.5	2.0	11.0	ns	3–5
t _{PHL}	Propagation Delay I _n to Z _n	5.0	2.0	5.5	9.5	2.0	11.0	ns	3–5

*Voltage Range 5.0 V is 5.0 V ±0.5 V.

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	65	pF	V _{CC} = 5.0 V

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ORDERING INFORMATION

Device Order Number	Package	Shipping†
MC74AC153DG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74AC153DR2G	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74AC153DTR2G	TSSOP–16 (Pb–Free)	2500 Tape & Reel
MC74ACT153DG	SOIC–16 (Pb–Free)	48 Units / Rail
MC74ACT153DR2G	SOIC–16 (Pb–Free)	2500 Tape & Reel
MC74ACT153DTR2G	TSSOP–16 (Pb–Free)	2500 Tape & Reel

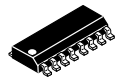
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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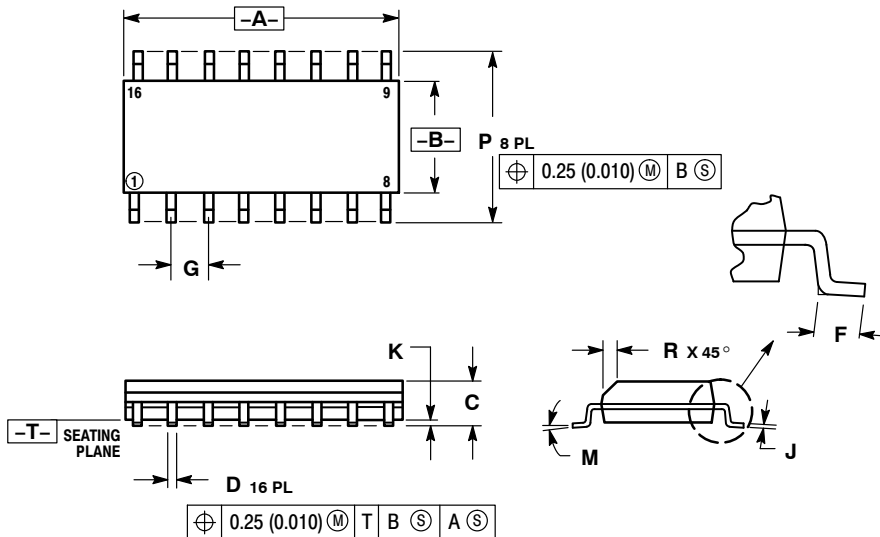
ON



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

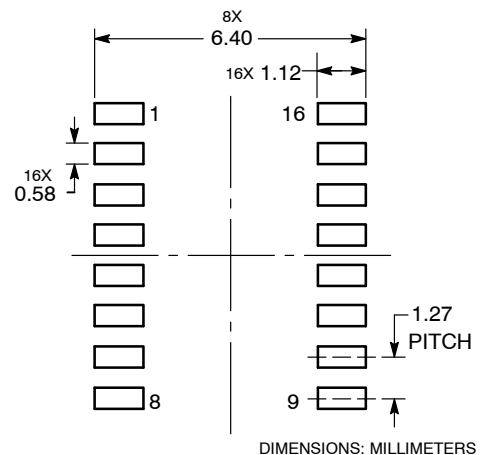
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

SOLDERING FOOTPRINT



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