

MC14532B

8-Bit Priority Encoder

The MC14532B is constructed with complementary MOS (CMOS) enhancement mode devices. The primary function of a priority encoder is to provide a binary address for the active input with the highest priority. Eight data inputs (D0 thru D7) and an enable input (E_{in}) are provided. Five outputs are available, three are address outputs (Q0 thru Q2), one group select (GS) and one enable output (E_{out}).

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V_{in} , V_{out}	-0.5 to $V_{DD} + 0.5$	V
Input or Output Current (DC or Transient) per Pin	I_{in} , I_{out}	± 10	mA
Power Dissipation, per Package (Note 1)	P_D	500	mW
Ambient Temperature Range	T_A	-55 to +125	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (8 Sec Soldering)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: "D/DW" Package: -7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

TRUTH TABLE

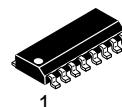
Input									Output				
E_{in}	D7	D6	D5	D4	D3	D2	D1	D0	GS	Q2	Q1	Q0	E_{out}
0	X	X	X	X	X	X	X	X	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	0	1
1	1	X	X	X	X	X	X	X	1	1	1	1	0
1	0	1	X	X	X	X	X	X	1	1	1	0	0
1	0	0	1	X	X	X	X	X	1	1	0	1	0
1	0	0	0	1	X	X	X	X	1	1	0	0	0
1	0	0	0	0	1	X	X	X	1	0	1	1	0
1	0	0	0	0	0	1	X	X	1	0	1	0	0
1	0	0	0	0	0	0	1	X	1	0	0	1	0
1	0	0	0	0	0	0	0	1	1	0	0	0	0

X = Don't Care



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SOIC-16
D SUFFIX
CASE 751B

PIN ASSIGNMENT

D4	1	16	V_{DD}
D5	2	15	E_{out}
D6	3	14	GS
D7	4	13	D3
E_{in}	5	12	D2
Q2	6	11	D1
Q1	7	10	D0
V_{SS}	8	9	Q0

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YY, Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14532B

ORDERING INFORMATION

Device	Package	Shipping†
MC14532BDG	SOIC–16 (Pb–Free)	48 Units / Rail
MC14532BDR2G	SOIC–16 (Pb–Free)	2500 / Tape & Reel
NLV14532BDR2G*	SOIC–16 (Pb–Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC–Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	– 55° C		25° C			125° C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	–3.0	–	–2.4	–4.2	–	–1.7	–	mAdc
		5.0	–0.64	–	–0.51	–0.88	–	–0.36	–	
		10	–1.6	–	–1.3	–2.25	–	–0.9	–	
		15	–4.2	–	–3.4	–8.8	–	–2.4	–	
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I _{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (1.74 μA/kHz) f + I _{DD} I _T = (3.65 μA/kHz) f + I _{DD} I _T = (5.73 μA/kHz) f + I _{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.005.

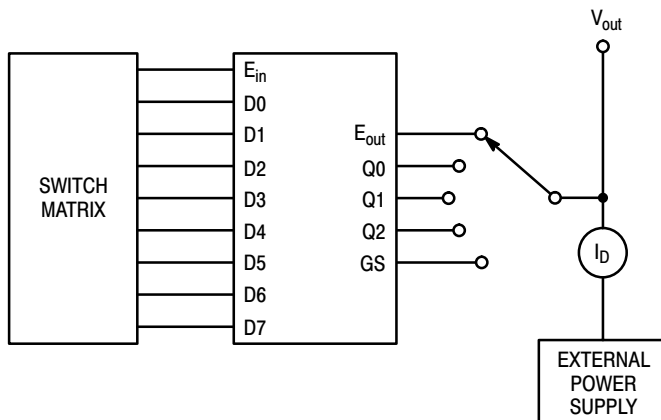
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SWITCHING CHARACTERISTICS ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$) (Note 5)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	t_{TLH}, t_{THL}	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time — E_{in} to E_{out} $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 120 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 77 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 55 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	205 110 80	410 220 160	ns
Propagation Delay Time — E_{in} to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 90 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 57 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 40 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	175 90 65	350 180 130	ns
Propagation Delay Time — E_{in} to Q_n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	280 140 100	560 280 200	ns
Propagation Delay Time — D_n to Q_n $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 265 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 137 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 85 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	300 170 110	600 340 220	ns
Propagation Delay Time — D_n to GS $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 195 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 107 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 75 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	— — —	280 140 100	560 280 200	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.



Output Under Test	$V_{GS} = V_{DD}$ $V_{DS} = V_{out}$ Sink Current		$V_{GS} = -V_{DD}$ $V_{DS} = V_{out} - V_{DD}$ Source Current			
	D0 thru D7	E_{in}	D0 thru D6	D7	E_{in}	
E_{out}	X	0	0	0	1	
Q0	X	0	0	1	1	
Q1	X	0	0	1	1	
Q2	X	0	0	1	1	
GS	X	0	0	1	1	

Figure 1. Typical Sink and Source Current Characteristics

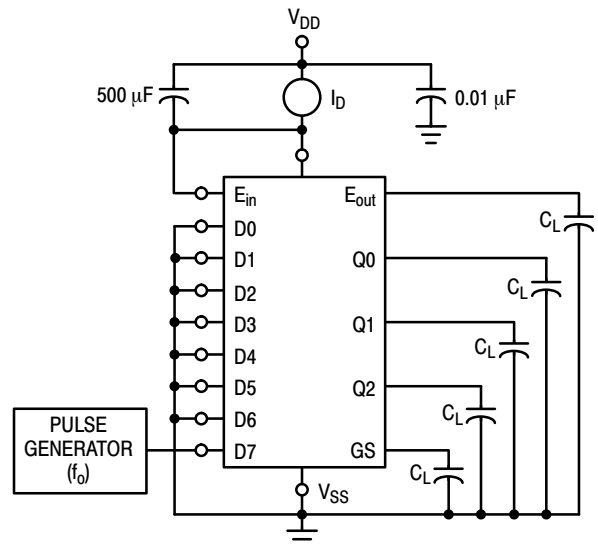


Figure 2. Typical Power Dissipation Test Circuit

MC14532B

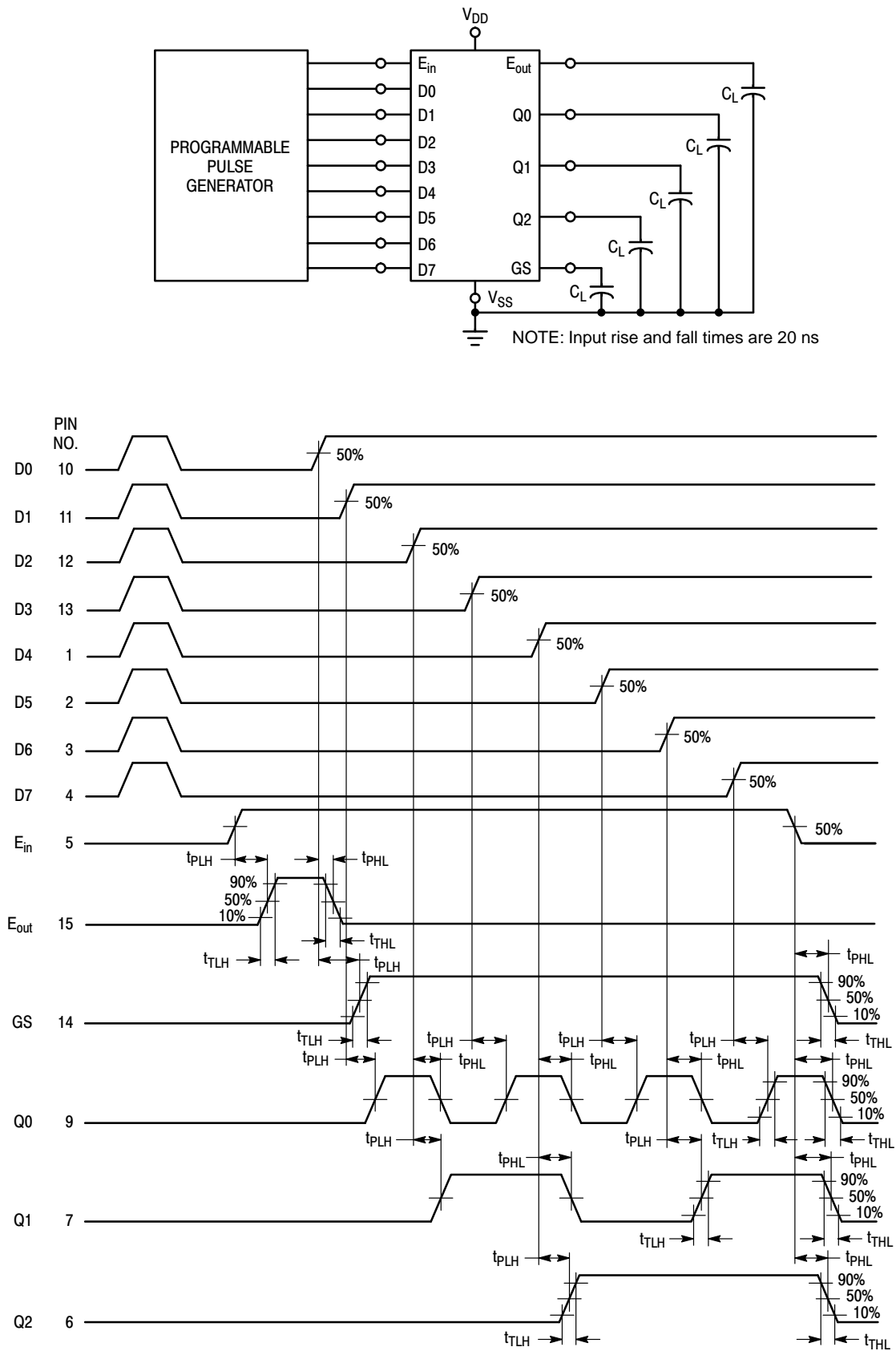


Figure 3. AC Test Circuit and Waveforms

MC14532B

LOGIC EQUATIONS

$$E_{out} = E_{in} \cdot \bar{D0} \cdot \bar{D1} \cdot \bar{D2} \cdot \bar{D3} \cdot \bar{D4} \cdot \bar{D5} \cdot \bar{D6} \cdot \bar{D7}$$

$$Q0 = E_{in} \cdot (D1 \cdot \bar{D2} \cdot \bar{D4} \cdot \bar{D6} + D3 \cdot \bar{D4} \cdot \bar{D6} + D5 \cdot \bar{D6} + D7)$$

$$Q1 = E_{in} \cdot (D2 \cdot \bar{D4} \cdot \bar{D5} + D3 \cdot \bar{D4} \cdot \bar{D5} + D6 + D7)$$

$$Q2 = E_{in} \cdot (D4 + D5 + D6 + D7)$$

$$GS = E_{in} \cdot (D0 + D1 + D2 + D3 + D4 + D5 + D6 + D7)$$

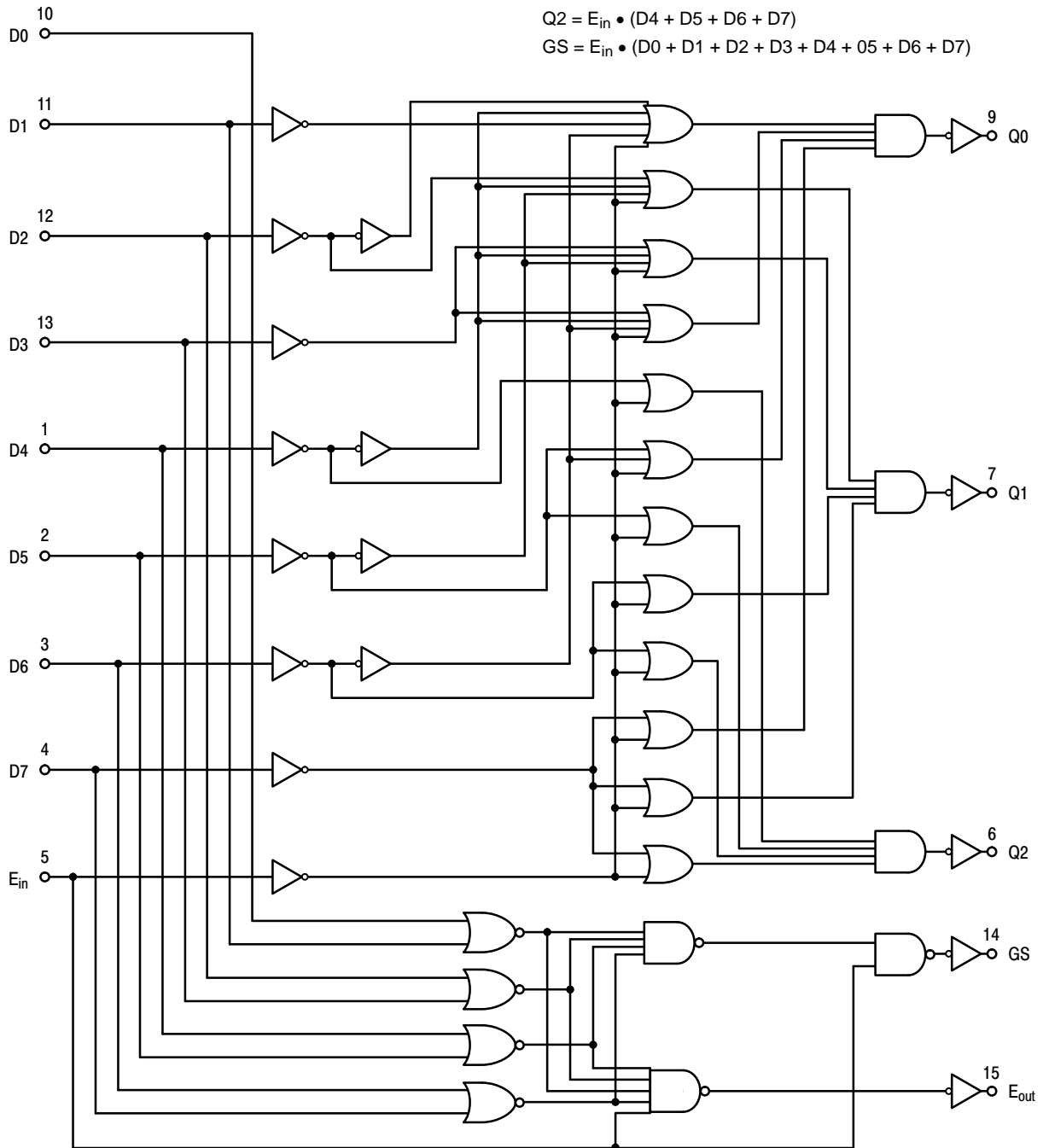


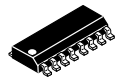
Figure 4. Logic Diagram
(Positive Logic)

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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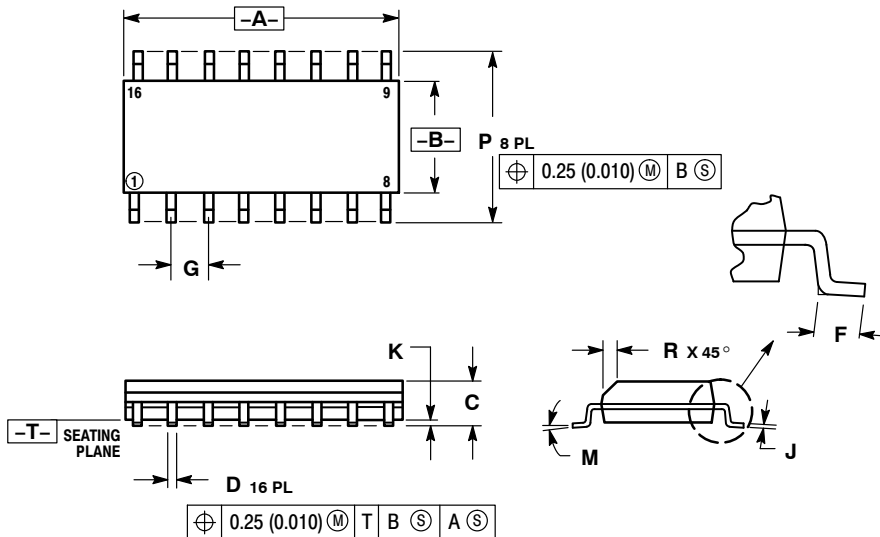
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SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

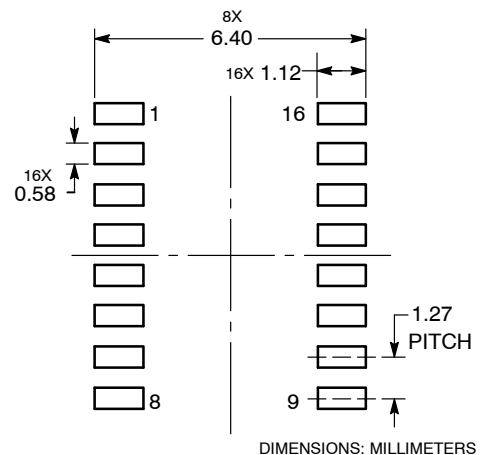
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
E	0.40	1.25	0.016	0.049
F	1.27 BSC		0.050 BSC	
G	0.19	0.25	0.008	0.009
H	0.10	0.25	0.004	0.009
I	0°	7°	0°	7°
J	5.80	6.20	0.229	0.244
K	0.25	0.50	0.010	0.019

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:
PIN 1. COLLECTOR	PIN 1. CATHODE	PIN 1. COLLECTOR, DYE #1	PIN 1. COLLECTOR, DYE #1
2. BASE	2. ANODE	2. BASE, #1	2. COLLECTOR, #1
3. EMITTER	3. NO CONNECTION	3. EMITTER, #1	3. COLLECTOR, #2
4. NO CONNECTION	4. CATHODE	4. COLLECTOR, #1	4. COLLECTOR, #2
5. EMITTER	5. CATHODE	5. COLLECTOR, #2	5. COLLECTOR, #3
6. BASE	6. NO CONNECTION	6. BASE, #2	6. COLLECTOR, #3
7. COLLECTOR	7. ANODE	7. EMITTER, #2	7. COLLECTOR, #4
8. COLLECTOR	8. CATHODE	8. COLLECTOR, #2	8. COLLECTOR, #4
9. BASE	9. CATHODE	9. COLLECTOR, #3	9. BASE, #4
10. EMITTER	10. ANODE	10. BASE, #3	10. EMITTER, #4
11. NO CONNECTION	11. NO CONNECTION	11. EMITTER, #3	11. BASE, #3
12. EMITTER	12. CATHODE	12. COLLECTOR, #3	12. EMITTER, #3
13. BASE	13. CATHODE	13. COLLECTOR, #4	13. BASE, #2
14. COLLECTOR	14. NO CONNECTION	14. BASE, #4	14. EMITTER, #2
15. EMITTER	15. ANODE	15. EMITTER, #4	15. BASE, #1
16. COLLECTOR	16. CATHODE	16. COLLECTOR, #4	16. EMITTER, #1

STYLE 5:	STYLE 6:	STYLE 7:
PIN 1. DRAIN, DYE #1	PIN 1. CATHODE	PIN 1. SOURCE N-CH
2. DRAIN, #1	2. CATHODE	2. COMMON DRAIN (OUTPUT)
3. DRAIN, #2	3. CATHODE	3. COMMON DRAIN (OUTPUT)
4. DRAIN, #2	4. CATHODE	4. GATE P-CH
5. DRAIN, #3	5. CATHODE	5. COMMON DRAIN (OUTPUT)
6. DRAIN, #3	6. CATHODE	6. COMMON DRAIN (OUTPUT)
7. DRAIN, #4	7. CATHODE	7. COMMON DRAIN (OUTPUT)
8. DRAIN, #4	8. CATHODE	8. SOURCE P-CH
9. GATE, #4	9. ANODE	9. SOURCE P-CH
10. SOURCE, #4	10. ANODE	10. COMMON DRAIN (OUTPUT)
11. GATE, #3	11. ANODE	11. COMMON DRAIN (OUTPUT)
12. SOURCE, #3	12. ANODE	12. COMMON DRAIN (OUTPUT)
13. GATE, #2	13. ANODE	13. GATE N-CH
14. SOURCE, #2	14. ANODE	14. COMMON DRAIN (OUTPUT)
15. GATE, #1	15. ANODE	15. COMMON DRAIN (OUTPUT)
16. SOURCE, #1	16. ANODE	16. SOURCE N-CH

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