# Summary of Specification for OIS & Open-AF Control LSI

# LC898128DP1XGTBG

### Overview

LC898128DP1XGTBG is a system LSI integrating an on−chip 32−bit DSP, a FLASH ROM and peripherals including analog circuits for OIS (Optical Image Stabilization) / Open−AF (Auto Focus) control, constant current drivers.

### Features

- On−chip 32bit DSP
  - Built−in Software for Digital Servo Filter
  - Built−in Software for Gyro Filter
- Memory
  - 40 KByte Flash Memory
  - Program ROM
  - Program SRAM
  - Data SRAM
- Peripherals
  - AD Converter
  - DA Converter
  - 2−wire Serial I/F Circuit
    (The Communication Protocol is Compatible with $I^2C$)
  - Hall Bias Circuit x2ch
  - Hall Amp x2ch
  - OSC (Oscillator)
  - LDO (Low Drop−Out Regulator)
  - Temperature Sensor
  - Digital Gyro I/F (SPI)
  - Interrupt I/F
- Driver
  - OIS
    Constant Current Linear Driver (x2ch, $I_{full}$ = 200 mA)
  - OP−AF (bi−direction)
    Constant Current Linear Driver (x1ch, $I_{full}$ = 130 mA)
- Power Supply Voltage
  - AD/DA/VGA/LDO/OSC/Flash:
    AVDD30 = 2.7 V to 3.3 V
  - Driver: VM1,2 = 1.8 V to 3.3 V
  - 1.8 V I/O: IOVDD = 1.7 V to 3.3 V
  - Core Logic: generated by on−chip LDO
    DVDD13 = typ. 1.38 V
    Connect 1 μF Capacitor to LDPO pin
- Package
  - WLCSP30 (4.300 mm x 1.175 mm) Thickness Max. 0.35 mm, without Back Coat
  - Ball 3 x 10
  - Pitch 0.4 mm
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**ON Semiconductor®**

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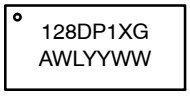
**WLCSP30, 1.175x4.3x0.33**
**CASE 567WW**

**MARKING DIAGRAM**




| | |
|---|---|
| 128DP1XG | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

## ORDERING INFORMATION

| Part Number | Package | Shipping† |
|---|---|---|
| LC898128DP1XGTBG | WLCSP30<br>(Pb−Free, Halogen−Free) | 4000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

## BLOCK DIAGRAM

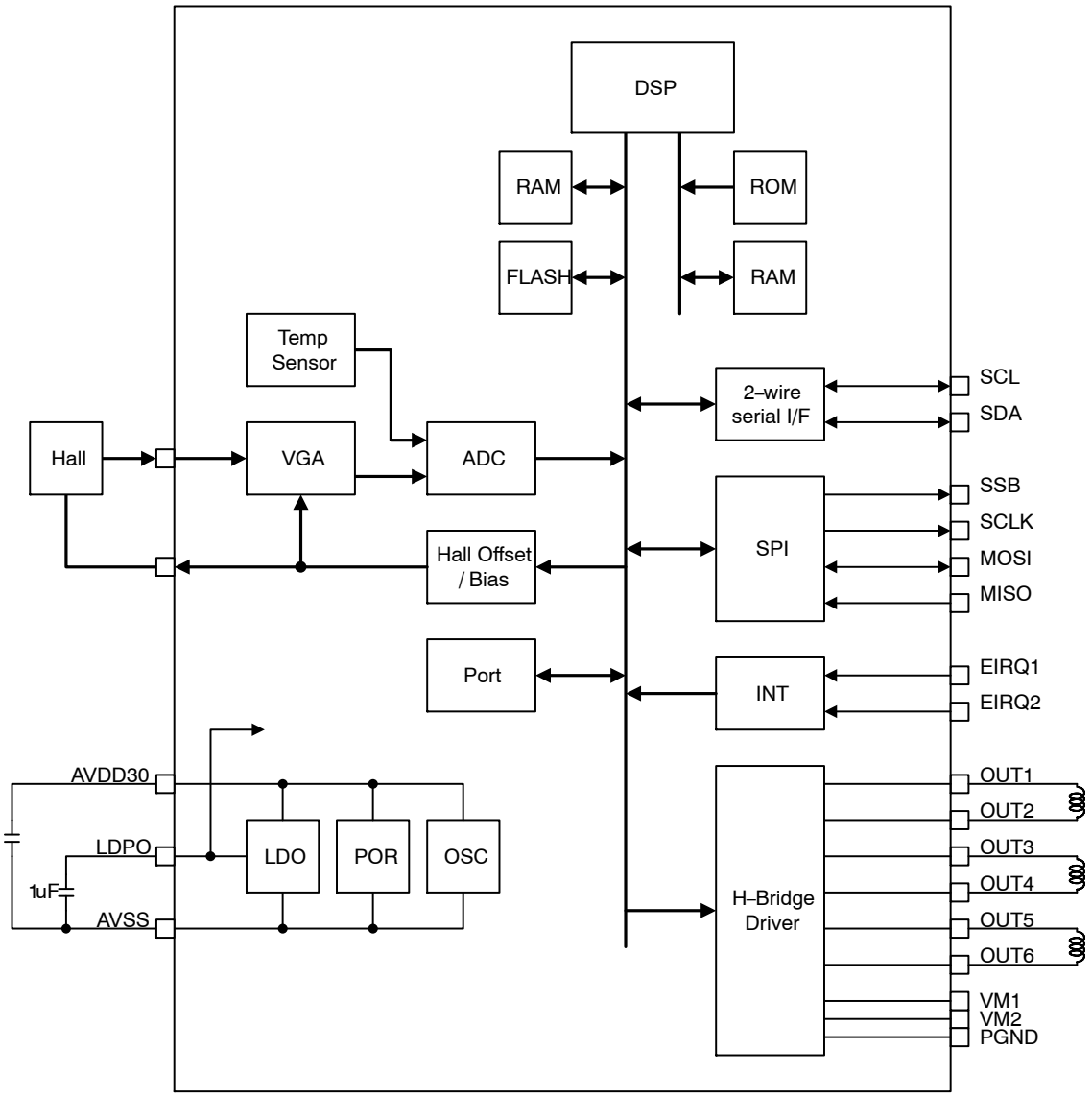



**Figure 1. Block Diagram**

## PIN LAYOUT

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 |
|---|---|---|---|---|---|---|---|---|---|---|
| C | OUT1 | OUT2 | OUT5 | HLXBO | HLYBO | EIRQ2 | MISO | MOSI | IOVDD | SCLK |
| B | VM1 | PGND | VM2 | AVSS | PCNT | OPINPX | OPINPY | MON1 | SSB | SDA |
| A | OUT3 | OUT4 | OUT6 | AVDD30 | LDPO | OPINMX | OPINMY | MON2 | EIRQ1 | SCL |

| | |
|---|---|
| | Driver |
| | VDD/VSS |
| | Internal VDD Output |
| | 1.8V I/O |

**Figure 2. Pin Layout (Bottom View)**

**Table 1. PIN DESCRIPTION**

| No. | Pin | I/O | I/O Pwr | Primary Function | Sub Functions | Init |
|---|---|---|---|---|---|---|
| 1 | MON1 | B | AVDD30 | Servo Monitor Analog In/Out | 2−wire serial Monitor Data | Z |
| 2 | MON2 | B | AVDD30 | Servo Monitor Analog In/Out | 2−wire serial Monitor Clock | Z |
| 3 | SCL | B | IOVDD | 2−wire serial HOST I/F Clock Slave | | Z |
| 4 | SDA | B | IOVDD | 2−wire serial HOST I/F Data Slave | | Z |
| 5 | IOVDD | P | | I/O Power (1.7 V to 3.3 V) | | |
| 6 | SSB | B | IOVDD | Digital Gyro Data I/F Chip Select Out (3/4−wire Master) | Digital Gyro Data I/F Chip Select In (3/4−wire Slave) | Z |
| 7 | SCLK | B | IOVDD | Digital Gyro Data I/F Clock Out (3/4−wire Master) | Digital Gyro Data I/F Clock In (3/4−wire Slave)<br>2−wire serial Sensor Hub I/F Clock Slave | Z |
| 8 | MOSI | B | IOVDD | Digital Gyro Data I/F Data InOut (3−wire Master)<br>Digital Gyro Data I/F Data Out (4−wire Master) | Digital Gyro Data I/F Data InOut (3wire Slave)<br>Digital Gyro Data I/F Data In (4−wire Slave)<br>2−wire serial Sensor Hub I/F Data Slave | Z |
| 9 | MISO | B | IOVDD | Digital Gyro Data I/F Data In (4−wire Master)<br>Digital Gyro Data I/F Chip Select 2 Out (3−wire Master) | Digital Gyro Data I/F Data Out (4−wire Slave) | U |
| 10 | EIRQ1 | B | IOVDD | Interrupt Input 1 | | Z |
| 11 | EIRQ2 | B | IOVDD | Interrupt Input 2 | | Z |
| 12 | PCNT | O | AVDD30 | No use | | Z |
| 13 | HLXBO | O | AVDD30 | OIS Hall X Bias Output | | Z |
| 14 | HLYBO | O | AVDD30 | OIS Hall Y Bias Output | | Z |
| 15 | OPINMX | I | AVDD30 | OIS Hall X Opamp Input Minus | | − |
| 16 | OPINPX | I | AVDD30 | OIS Hall X Opamp Input Plus | | − |
| 17 | OPINMY | I | AVDD30 | OIS Hall Y Opamp Input Minus | | − |
| 18 | OPINPY | I | AVDD30 | OIS Hall Y Opamp Input Plus | | − |
| 19 | OUT1 | O | VM1 | OIS Driver Output | | Z |
| 20 | OUT2 | O | VM1 | OIS Driver Output | | Z |
| 21 | OUT3 | O | VM1 | OIS Driver Output | | Z |
| 22 | OUT4 | O | VM1 | OIS Driver Output | | Z |
| 23 | OUT5 | O | VM2 | OP−AF Driver Output | | Z |
| 24 | OUT6 | O | VM2 | OP−AF Driver Output | | Z |
| 25 | AVDD30 | P | | Analog Power (2.7 V to 3.3 V) | | − |
| 26 | AVSS | P | | Analog GND | | − |
| 27 | VM1 | P | | OIS Driver Power (1.8 V to 3.3 V) | | − |
| 28 | VM2 | P | | OP−AF Driver Power (1.8 V to 3.3 V) | | − |
| 29 | PGND | P | | Driver GND | | − |
| 30 | LDPO | P | | Internal 1.38 V LDO Power Output | | − |

*Process when pins are not used

NOTES: PIN TYPE “O” − Ensure that it is set to OPEN.
PIN TYPE “I” − OPEN is inhibited. Ensure that it is connected to the $V_{DD}$ or $V_{SS}$ even when it is unused.
(Please contact ON Semiconductor for more information about selection of $V_{DD}$ or $V_{SS}$.)
PIN TYPE “B” − If you are unsure about processing method on the pin description of pin layout table, please contact us.

Note that incorrect processing of unused pins may result in defects.

## ELECTRICAL CHARACTERISTICS

**Table 2. ABSOLUTE MAXIMUM RATINGS** at AVSS = 0 V, PGND = 0 V

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Power supply voltage | $V_{AD}30$ max | Ta ≤ 25°C | −0.3 to 4.6 | V |
| | VM max | Ta ≤ 25°C | −0.3 to 4.6 | |
| | $V_{IO}$ max | Ta ≤ 25°C | −0.3 to 4.6 | |
| Input/Output voltage | $V_{AI}30$, $V_{AO}30$ | Ta ≤ 25°C | −0.3 to $V_{AD}30$ + 0.3 | V |
| | $V_{MI}30$, $V_{MO}30$ | Ta ≤ 25°C | −0.3 to $V_{M}30$ + 0.3 | |
| | $V_{II}$, $V_{IOO}$ | Ta ≤ 25°C | −0.3 to $V_{IO}$ + 0.3 | |
| Storage temperature | Tstg | | −55 to 125 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 3. ALLOWABLE OPERATING RATINGS** at Ta = −30 to 85°C, AVSS = 0 V, PGND = 0 V

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **3.0 V Power Supply (AVDD30)** | | | | | |
| Power supply voltage | $V_{AD}30$ | 2.7 | 2.8 | 3.3 | V |
| Input voltage range | $V_{INA}$ | 0 | – | $V_{AD}30$ | V |
| **3.0 V Power Supply (VM1, VM2)** (Note 1) | | | | | |
| Power supply voltage | $V_{M}30$ | 1.8 (Note 2) | 2.8 | the lower of 3.3 and AVDD30 + 0.5 | V |
| Input voltage range | $V_{INM}$ | 0 | – | $V_{M}30$ | V |
| **1.8 V Power Supply (IOVDD)** | | | | | |
| Power supply voltage | $V_{IO}$ | 1.7 | 1.8 | 3.3 | V |
| Input voltage range | $V_{INI}$ | 0 | – | $V_{IO}$ | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
1. The VM1 and VM2 pins should be connected.
2. Constant current.

**Table 4. D.C. CHARACTERISTICS: INPUT/OUTPUT**
at Ta = −30 to 85°C, AVSS = 0 V, PGND = 0 V, AVDD30 = 2.7 to 3.3 V, IOVDD = 1.7 to 3.3 V

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit | Applicable Pins |
|---|---|---|---|---|---|---|---|
| High−level input voltage | VIH | CMOS Schmitt | 0.7 IOVDD | | | V | SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| Low−level input voltage | VIL | | | | 0.3 IOVDD | V | |
| High−level input voltage | VIH | CMOS Schmitt | 0.7 AVDD30 | | | V | MON1, MON2 |
| Low−level input voltage | VIL | | | | 0.3 AVDD30 | V | MON1, MON2 |
| High−level output voltage | VOH | IOH = −3 mA | IOVDD − 0.2 | | | V | SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| Low−level output voltage | VOL | IOL = 3 mA | | | 0.2 | V | SCL, SDA, SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2 |
| High−level output voltage | VOH | IOH = −2 mA | AVDD30 − 0.2 | | | V | MON1, MON2 |
| Low−level output voltage | VOL | IOL = 2 mA | | | 0.2 | V | MON1, MON2 |
| Analog input voltage | VAI | | AVSS | | AVDD30 | V | MON1, MON2, OPINPX, OPINMX, OPINPY, OPINMY |
| Pull Up resistor | Rup | | 20 | | 250 | kΩ | SSB, SCLK, MOSI, MISO, EIRQ1, EIRQ2, MON1, MON2 |
| Pull Down resistor | Rdn | | 20 | | 250 | kΩ | |

**Table 5. DRIVER OUTPUT** at Ta = 25°C, AVSS = 0 V, PGND = 0 V, AVDD30 = VM = 2.8 V

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output Current OUT1 ~ OUT4 | Ifull | Full code | 190 | 200 | 210 | mA |
| Output Current OUT5, OUT6 | | Full code, OP−AF (bidirection) | 123.5 | 130 | 136.5 | mA |

**Table 6. NON−VOLATILE MEMORY CHARACTERISTICS**

| | | | | |
|---|---|---|---|---|
| Operating temperature | Topr1 | Read for FLASH | −30 ~ 85 | °C |
| | Topr2 | Program&Erase for FLASH | −10 ~ 65[1] | °C |

| Item | Symbol | Condition | Min | Typ | Max | Unit | Applicable Circuit |
|---|---|---|---|---|---|---|---|
| Endurance | EN | | | | 1000 | Cycles | Flash Memory |
| Data retention | RT | | 10 | | | Years | |
| Write time | tWT | | | | 3 | ms | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. All drivers must be in the standby state.

## AC CHARACTERISTICS

### Power Supply Timing

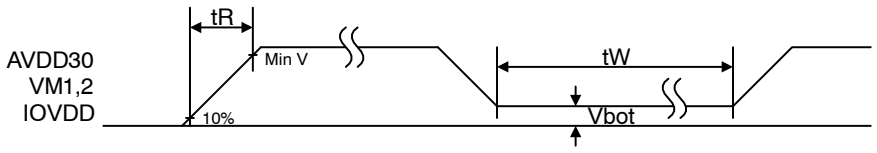



**Figure 3. $V_{DD}$ Supply Timing**

**Table 7.**

| Item | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Rise time | tR | | | 3 | ms |
| Wait time | tW | 100 | | | ms |
| Bottom Voltage | Vbot | | | 0.2 | V |

Injection order between AVDD30, VM1,2 and IOVDD is below.

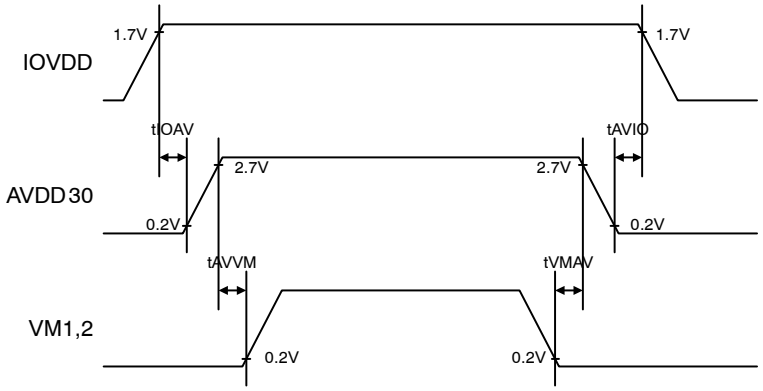



**Figure 4.**

**Table 8.**

| Item | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| IOVDD ON to AVDD30 ON | tIOAV | 0 | | | ms |
| AVDD30 ON to VM1,2 ON | tAVVM | 0 | | | ms |
| VM1,2 OFF to AVDD30 OFF | tVMAV | 0 | | | ms |
| AVDD30 OFF to IOVDD OFF | tAVIO | 0 | | ** | ms |

NOTES: VM1 = VM2 ≤ AVDD30 + 0.5 V
The VM1 and VM2 pins should be connected.

SDA, SCL, SSB, SCLK, MOSI, MISO, EIRQ1 and EIRQ2 tolerate 3 V input at the time of power off.

The data in the Flash memory may be rewritten unintentionally if you do not keep specifications. And it is forbidden to power off during Flash memory access. The data in the Flash memory may be rewritten unintentionally.

OIS, AF drivers are recommended to set standby before VM1 and VM2 power off.

** Please make IOPRSTB(D0_0064h,bit0)=0 before turning OFF AVDD30 when AVDD30 is turned off with keeping IOVDD on.

### 2−wire Serial Interface Timing

The 2−wire serial interface timing definition and electric characteristics are shown below. The communication protocol is compatible with I$^2$C. This circuit has clock stretch function.

Static Address : 7'b0100100

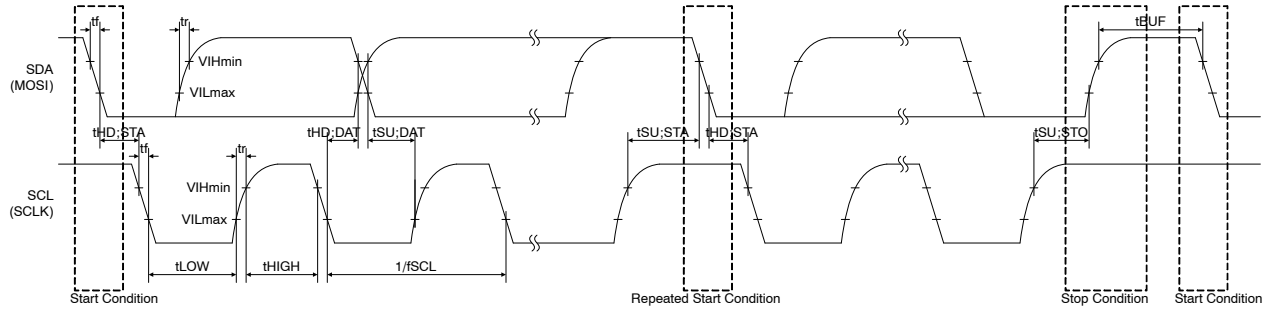



**Figure 5.**

**Table 9.**

| Item | Symbol | Standard−mode | | Fast−mode | | Fast−mode Plus | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| SCL clock frequency | fSCL | − | 100 | − | 400 | − | 1000 | kHz |
| START condition hold time | tHD;STA | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| SCL clock Low period | tLOW | 4.7 | − | 1.3 | − | 0.5 | − | μs |
| SCL clock High period | tHIGH | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| Setup time for repetition START condition | tSU;STA | 4.7 | − | 0.6 | − | 0.26 | − | μs |
| Data hold time | tHD;DAT | 0 (1) | 3.45 | 0 (1) | 0.9 | 0 (1) | 0.45 | μs |
| Data setup time | tSU;DAT | 250 | − | 100 | − | 50 | − | ns |
| SDA, SCL rising time | tr | − | 1000 | − | 300 | − | 120 | ns |
| SDA, SCL falling time | tf | − | 300 | − | 300 | − | 120 | ns |
| STOP condition setup time | tSU;STO | 4.0 | − | 0.6 | − | 0.26 | − | μs |
| Bus free time between STOP and START | tBUF | 4.7 | − | 1.3 | − | 0.5 | − | μs |

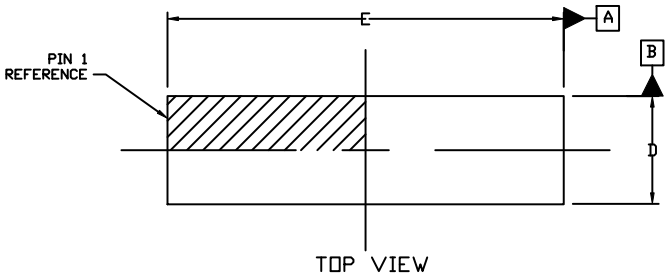
1. Although the I$^2$C specification defines a condition that 300 ns of hold time is required internally, this LSI is designed for a condition with typ. 40 ns of hold time. If SDA (MOSI) signal is unstable around falling point of SCL (SCLK) signal, please implement an appropriate treatment on board, such as inserting a resister.

Development product sample is a product that intend to verify whether it is matched the customer's application spec. We kindly ask you to evaluate surely and enough prior mass−production. Please contact our sales, if there are any problems.

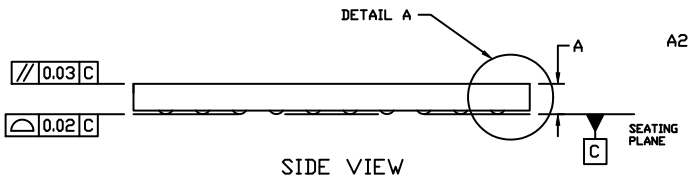
ON Semiconductor is licensed by the Philips Corporation to carry the I$^2$C bus protocol.

**WLCSP30, 1.175x4.3x0.33**
CASE 567WW
ISSUE O

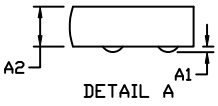
DATE 18 JUL 2018




TOP VIEW




SIDE VIEW

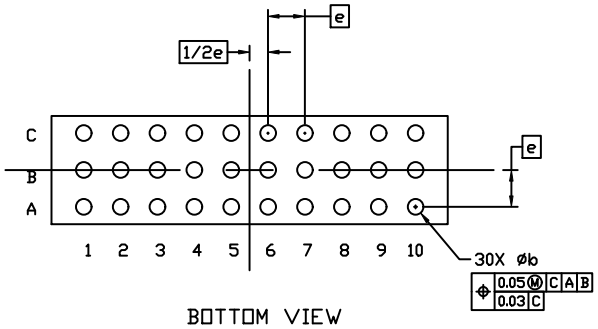



DETAIL A

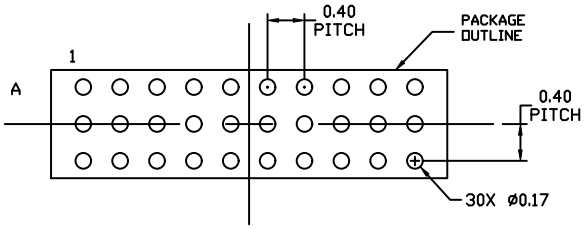
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPERICAL CROWNS OF THE CONTACT BALLS.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE CONTACT BALLS.
5. DIMENSION b IS MEASURED AT THE MAXIMUM CONTACT BALL DIAMETER PARALLEL TO DATUM C.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.31 | 0.33 | 0.35 |
| A1 | 0.034 | 0.040 | 0.046 |
| A2 | 0.278 | 0.290 | 0.303 |
| b | 0.15 | 0.17 | 0.19 |
| D | 1.15 | 1.175 | 1.20 |
| E | 4.275 | 4.30 | 4.325 |
| e | 0.40 BSC | | |




BOTTOM VIEW




RECOMMENDED
MOUNTING FOOTPRINT

**GENERIC**
**MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
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| **DESCRIPTION:** | **WLCSP30, 1.175x4.3x0.33** | | **PAGE 1 OF 1** |

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