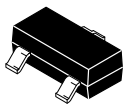
NPN Epitaxial Silicon Transistor

KSC3265

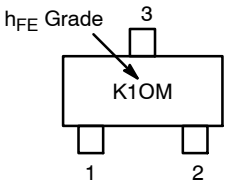


SOT−23
CASE 318

Low Frequency Power Amplifier

- Complement to KSA1298

MARKING DIAGRAM



K1O = Specific Device Code
M = Date Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Ratings	Unit
V_{CBO}	Collector−Base Voltage	30	V
V_{CEO}	Collector−Emitter Voltage	25	V
V_{EBO}	Emitter−Base Voltage	5	V
I_C	Collector Current	800	mA
I_B	Base Current	160	mA
P_C	Collector Power Dissipation	200	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping
KSC3265YMTF	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

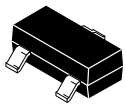
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{CEO}	Collector−Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0	25	–	–	V
BV_{EBO}	Emitter−Base Breakdown Voltage	I_E = 1 mA, I_C = 0	5	–	–	V
I_{CBO}	Collector Cut−off Current	V_{CB} = 30 V, I_E = 0	–	–	100	nA
I_{EBO}	Emitter Cut−off Current	V_{BE} = 5 V, I_C = 0	–	–	100	nA
h_{FE1} h_{FE2}	DC Current Gain	V_{CE} = 1 V, I_C = 100 mA V_{CE}= 6 V, I_C = 800 mA	100 40	– –	320 –	
V_{CE} (sat)	Collector−Emitter Saturation Voltage	I_C = 500 mA, I_B= 20 mA	–	–	0.4	V
V_{BE} (on)	Base−Emitter On Voltage	V_{CE} = 1 V, I_C = 10 mA	0.5	–	0.8	V
f_T	Current Gain Bandwidth Product	V_{CE} = 5 V, I_C = 10 mA	–	120	–	MHz
C_{ob}	Output Capacitance	V_{CB} = 10 V, I_E = 0, f = 1 MHz	–	13	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

h_{FE1} Classification

Classification	O	Y
h_{FE1}	100 ~ 200	160 ~ 320



SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

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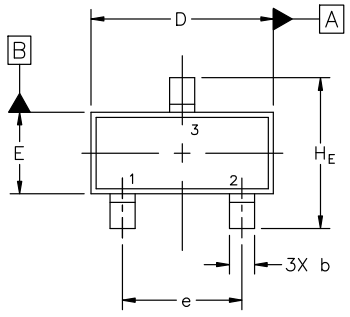
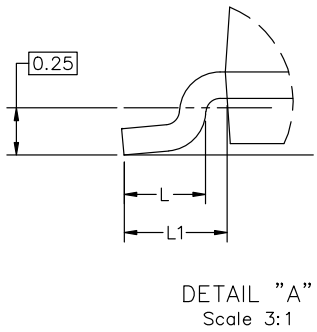
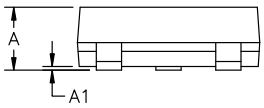


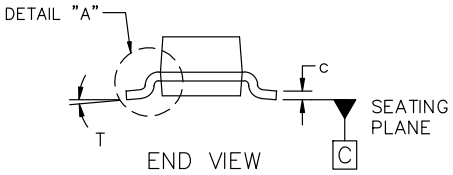
TOP VIEW



DETAIL "A"
Scale 3:1



SIDE VIEW

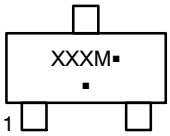


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	−−−	10°

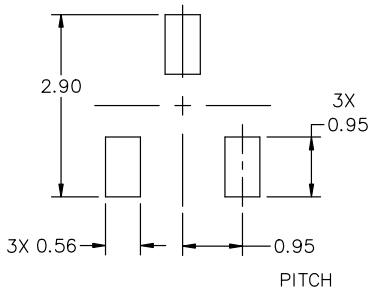
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC
MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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