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December 2013



## **IRLS640A** N-Channel Logic Level A-FET 200 V, 9.8 A, 180 mΩ

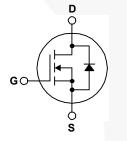
#### Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters, switch mode power supplies, DC-AC converters for uninterrupted power supply and motor control.

#### Features

- 9.8 A, 200 V,  $R_{DS(on)}$  = 180 m $\Omega$  @ V<sub>GS</sub> = 5 V Low Gate Charge (Typ. 40 nC)
- Low Crss (Typ. 95 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- Logic-Level Gate Drive





#### **Absolute Maximum Ratings**

Symbol	Characteristic	Value	Units	
V <sub>DSS</sub>	Drain-to-Source Voltage	200	V	
	Continuous Drain Current (T <sub>C</sub> =25°C)	9.8		
Ι <sub>D</sub>	Continuous Drain Current (T <sub>c</sub> =100℃)	6.2	A	
I <sub>DM</sub>	Drain Current-Pulsed (1)	63	А	
V <sub>GS</sub>	Gate-to-Source Voltage	±20	V	
E <sub>AS</sub> Single Pulsed Avalanche Energy ②		64	mJ	
I <sub>AR</sub>	Avalanche Current (1)	18	A	
E <sub>AR</sub>	Repetitive Avalanche Energy (1)	4.0	mJ	
dv/dt	Peak Diode Recovery dv/dt 3	5	V/ns	
	Total Power Dissipation (T <sub>c</sub> =25℃)	40	W	
P <sub>D</sub>	Linear Derating Factor	0.32	W/℃	
	Operating Junction and	55 to 1150		
$T_J$ , $T_STG$	Storage Temperature Range	- 55 to +150		
	Maximum Lead Temp. for Soldering	200	°C	
TL	Purposes, 1/8 " from case for 5-seconds	300		

#### Thermal Resistance

Symbol	Characteristic	Тур.	Max.	Units
$R_{ extsf{ heta}JC}$	Junction-to-Case		3.13	°0111
$R_{_{ ext{ heta}JA}}$	Junction-to-Ambient		62.5	°C/W

#### Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
IRLS640A	IRLS640A	TO-220F	Tube	N/A	N/A	50 units

## **Electrical Characteristics** ( $T_c$ =25 °C unless otherwise specified)

Symbol	Characteristic		Characteristic Min. Typ. M		Max.	Units	Test Condition
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage				V	V <sub>GS</sub> =0V,I <sub>D</sub> =250µA	
$\Delta \text{BV} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temp. Coeff.		0.17		V/℃	I <sub>D</sub> =250µA <b>See Fig 7</b>	
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	-	2.0	V	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250µA	
	Gate-Source Leakage, Forward			100	nA	V <sub>GS</sub> =20V	
I <sub>GSS</sub>	Gate-Source Leakage, Reverse			-100		V <sub>GS</sub> =-20V	
	Drain to Source Lookage Current			10		V <sub>DS</sub> =200V	
I <sub>DSS</sub>	Drain-to-Source Leakage Current			100	μA	V <sub>DS</sub> =160V,T <sub>C</sub> =125 ℃	
R <sub>DS(on)</sub>	Static Drain-Source On-State Resistance			0.18	Ω	V <sub>GS</sub> =5V,I <sub>D</sub> =4.9A ④	
9 <sub>fs</sub>	Forward Transconductance		13.3		S	V <sub>DS</sub> =40V,I <sub>D</sub> =4.9A ④	
C <sub>iss</sub>	Input Capacitance		1310	1705		(1 - 0)(1) = 25)(f - 1)(1)	
C <sub>oss</sub>	Output Capacitance		200	250	pF	$V_{GS}$ =0V, $V_{DS}$ =25V,f =1MHz	
C <sub>rss</sub>	Reverse Transfer Capacitance	-	95	120		See Fig 5	
t <sub>d(on)</sub>	Turn-On Delay Time		11	30			
t <sub>r</sub>	Rise Time Turn-Off Delay Time		8	25	ns	V <sub>DD</sub> =100V,I <sub>D</sub> =18A,	
t <sub>d(off)</sub>			46	100		R <sub>G</sub> =4.6Ω	
t <sub>f</sub>	Fall Time		15	40		See Fig 13 4 5	
Qg	Total Gate Charge		40	56		V <sub>DS</sub> =160V,V <sub>GS</sub> =5V,	
Q <sub>gs</sub>	Gate-Source Charge		6.8		nC	I <sub>D</sub> =18A	
Q <sub>gd</sub>	Gate-Drain("Miller") Charge		18.6			See Fig 6 & Fig 12 (4) (5)	

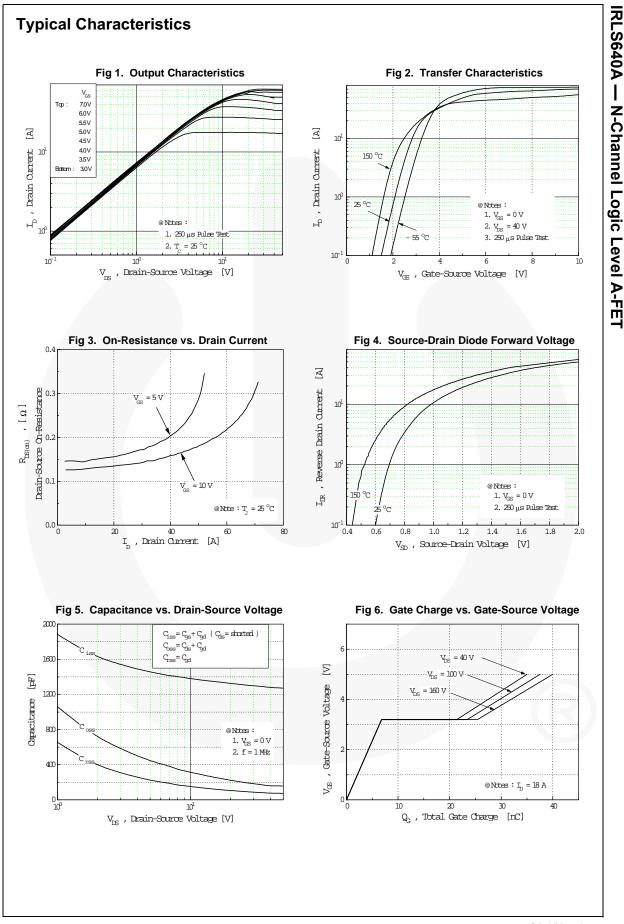
### Source-Drain Diode Ratings and Characteristics

Symbol	Characteristic	Min.	Тур.	Max.	Units	Test Condition	
I <sub>S</sub>	Continuous Source Current			18		Integral reverse pn-diode	
I <sub>SM</sub>	Pulsed-Source Current (1)			63	A	in the MOSFET	
V <sub>SD</sub>	Diode Forward Voltage ④			1.5	V	T <sub>J</sub> =25℃,I <sub>S</sub> =9.8A,V <sub>GS</sub> =0V	
t <sub>rr</sub>	Reverse Recovery Time		224		ns	T <sub>J</sub> =25℃,I <sub>F</sub> =18A	
Q <sub>rr</sub>	Reverse Recovery Charge		1.55		μC	di <sub>F</sub> /dt=100A/µs ④	

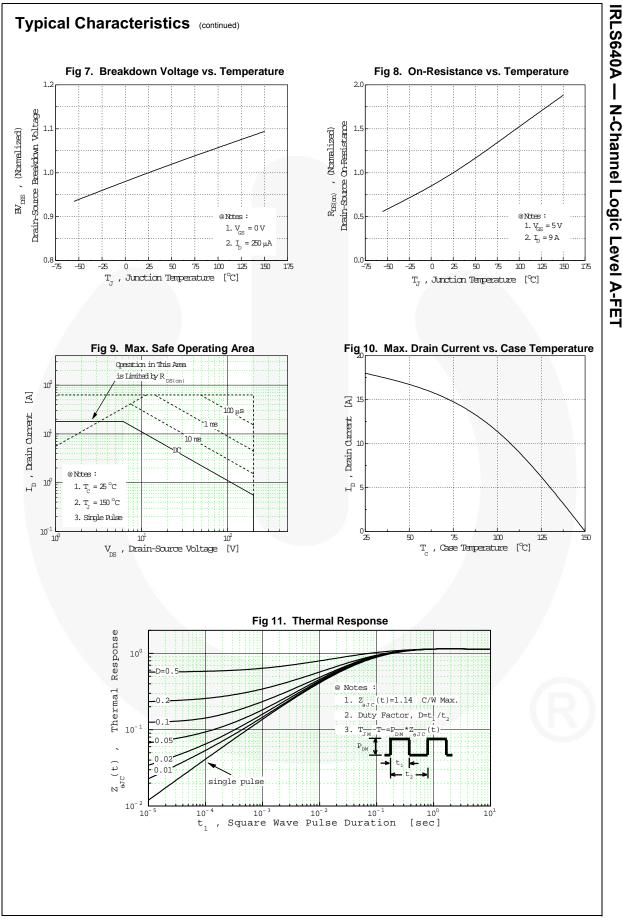
#### Notes :

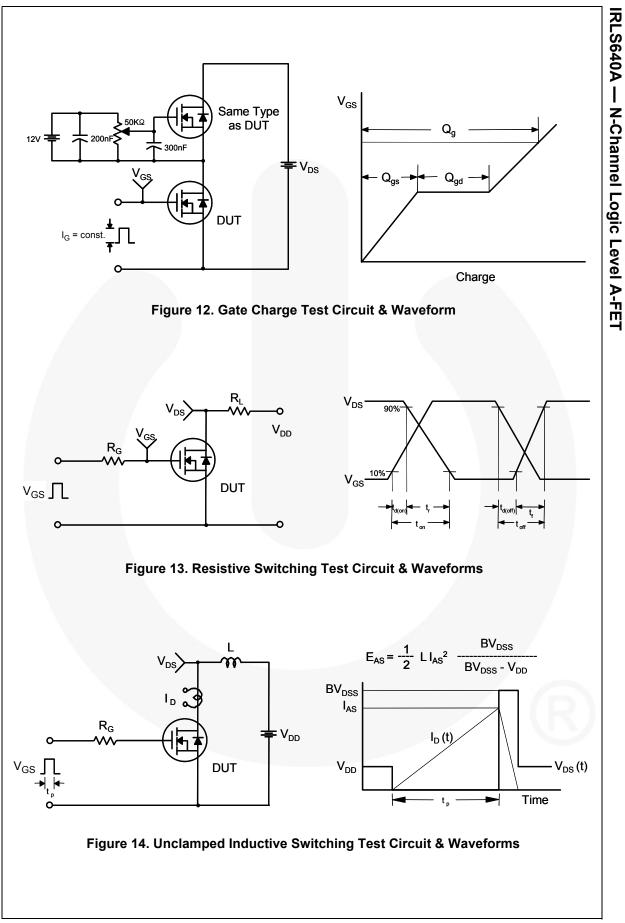
- ① Repetitive Rating : Pulse Width Limited by Maximum Junction Temperature

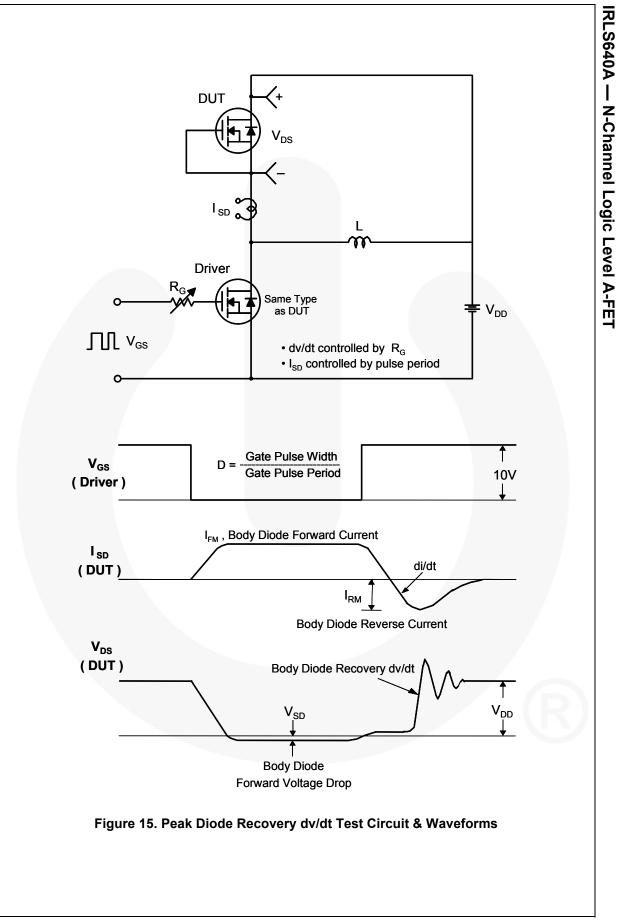
- 5 Essentially Independent of Operating Temperature

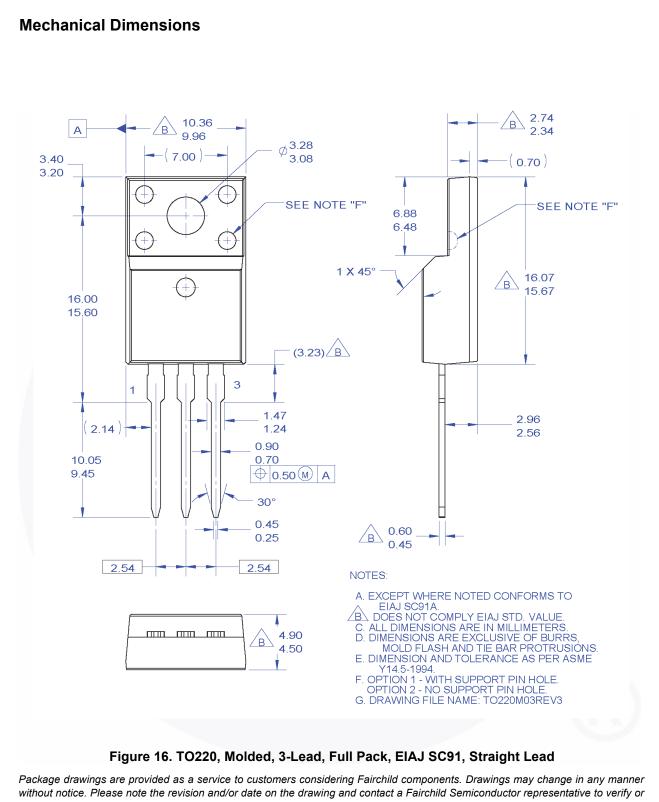


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IRLS640A —

**N-Channel Logic Level A-FET** 



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