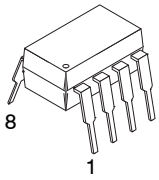
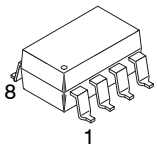
AC/DC to Logic Interface Optocoupler

HCPL3700M



PDIP8 9.655x6.6, 2.54P
CASE 646CQ



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CASE 709AC

Description

The HCPL3700M voltage/current threshold detection optocoupler consists of an AlGaAs LED connected to a threshold sensing input buffer IC which are optically coupled to a high gain darlington output. The input buffer chip is capable of controlling threshold levels over a wide range of input voltages with a single resistor. The output is TTL and CMOS compatible.

Features

- AC or DC Input
- Programmable Sense Voltage
- Logic Level Compatibility
- Threshold Guaranteed Over Temperature (0°C to 70°C)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC_{RMS} for 1 Minute
  - DIN EN/IEC60747−5−5
- These are Pb−Free Devices

Applications

- Low Voltage Detection
- 5 V to 240 V AC/DC Voltage Sensing
- Relay Contact Monitor
- Current Sensing
- Microprocessor Interface
- Industrial Controls

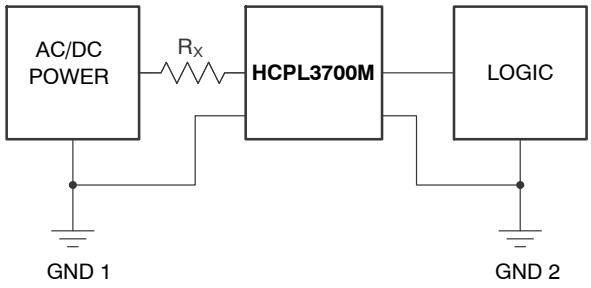
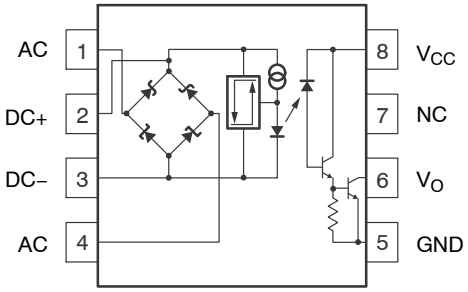


Figure 1. Schematic

ELECTRICAL CONNECTION



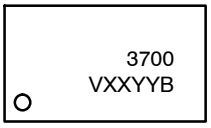
TRUTH TABLE

(Positive Logic)

Input	Output
H	L
L	H

A 0.1 μF bypass capacitor must be connected between pins 8 and 5.

MARKING DIAGRAM



3700	= Device Number
V	= DIN EN/IEC60747−5−5 Option (only appears on component ordered with this option)
XX	= Two−Digit Year Code
YY	= Two−Digit Work Week
B	= Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747−5−5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V_{RMS}	I–IV
	< 300 V_{RMS}	I–IV
	< 450 V_{RMS}	I–III
	< 600 V_{RMS}	I–III
	< 1000 V_{RMS} (Option TV)	I–III
Climatic Classification		40/85/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V_{PR}	Input−to−Output Test Voltage, Method A, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2,262	V_{peak}
	Input−to−Output Test Voltage, Method B, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2,651	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1,414	V_{peak}
V_{IOTM}	Highest Allowable Over−Voltage	6,000	V_{peak}
	External Creepage	≥ 8.0	mm
	External Clearance	≥ 7.4	mm
	External Clearance (for Option TV, 0.4” Lead Spacing)	≥ 10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.5	mm
T_S	Case Temperature (Note 1)	150	°C
$I_{S,INPUT}$	Input Current (Note 1)	25	mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7%) (Note 1)	250	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V (Note 1)	> 10^9	Ω

1. Safety limit value − maximum values allowed in the event of a failure.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter		Value	Units
T_{STG}	Storage Temperature		−40 to +125	°C
T_{OPR}	Operating Temperature		−40 to +85	°C
T_J	Junction Temperature		−40 to +125	°C
T_{SOL}	Lead Solder Temperature		260 for 10 s	°C
P_T	Total Package Power Dissipation (Note 2)		305	mW
EMITTER				
I_{IN}	Input Current	Average	50	mA
		Surge, 3 ms, 120 Hz Pulse Rate	140	
		Transient, 10 μs, 120 Hz Pulse Rate	500	
V_{IN}	Input Voltage (Pins 2−3)		−0.5	V
P_{IN}	Input Power Dissipation (Note 3)		230	mW
DETECTOR				
I_O	Output Current (Average) (Note 4)		30	mA
V_{CC}	Supply Voltage (Pins 8−5)		−0.5 to 20	V
V_O	Output Voltage (Pins 6−5)		−0.5 to 20	V
P_O	Output Power Dissipation (Note 5)		210	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Derate linearly above 70°C free−air temperature at a rate of 2.5 mW/°C.
3. Derate linearly above 70°C free−air temperature at a rate of 1.8 mW/°C.
4. Derate linearly above 70°C free−air temperature at a rate of 0.6 mA/°C.
5. Derate linearly above 70°C free−air temperature at a rate of 1.9 mW/°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	2	18	V
T_A	Ambient Operating Temperature	0	70	°C
f	Operating Frequency	0	4	kHz

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C unless otherwise specified)

Symbol	Parameter		Test Conditions	Min.	Typ.	Max.	Unit
I_{TH+}	Input Threshold Current		$V_{IN} = V_{TH+}$, V_{CC} = 4.5 V	1.96	2.40	3.11	mA
I_{TH-}			V_O = 0.4 V, $I_O \geq$ 4.2 mA (Note 6)	1.00	1.20	1.62	
V_{TH+}	Input Threshold Voltage	DC (Pins 2, 3)	$V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) V_{CC} = 4.5 V, V_O = 0.4 V (Note 6) $I_O \geq$ 4.2 mA	3.35	3.80	4.05	V
V_{TH-}			$V_{IN} = V_2 - V_3$ (Pins 1 & 4 Open) V_{CC} = 4.5 V, V_O = 2.4 V (Note 6) $I_O \geq$ 100 μA	2.01	2.50	2.86	V
V_{TH+}		AC (Pins 1, 4)	$\lvert V_{IN} \rvert = \lvert V_1 - V_4 \rvert$ (Pins 2 & 3 Open) V_{CC} = 4.5 V, V_O = 0.4 V (Note 6) $I_O \geq$ 4.2 mA	4.23	5.00	5.50	V
V_{TH-}			$\lvert V_{IN} \rvert = \lvert V_1 - V_4 \rvert$ (Pins 2 & 3 Open) V_{CC} = 4.5 V, V_O = 2.4 V (Note 6) $I_O \leq$ 100 μA	2.87	3.70	4.20	V
I_{HYS}	Hysteresis		$I_{HYS} = I_{TH+} - I_{TH-}$	–	1.2		mA
V_{HYS}			$V_{HYS} = V_{TH+} - V_{TH-}$	–	1.3		V
V_{IHC1}	Input Clamp Voltage		$V_{IHC1} = V_2 - V_3$, V_3 = GND I_{IN} = 10 mA Pins 1 & 4 Connected to PIN 3	5.4	6.3	6.6	V
V_{IHC2}			$V_{IHC2} = \lvert V_1 - V_4 \rvert$, $\lvert I_{IN} \rvert$ = 10 mA (Pins 2 & 3 Open)	6.1	7.0	7.3	V
V_{IHC3}			$V_{IHC3} = V_2 - V_3$, V_3 = GND I_{IN} = 15 mA (Pins 1 & 4 Open)	–	12.5	13.4	V
V_{ILC}			$V_{ILC} = V_2 - V_3$, V_3 = GND I_{IN} = −10 mA	–	−0.75	–	V
I_{IN}	Input Current		$V_{IN} = V_2 - V_3$ = 5.0 V (Pins 1 & 4 Open)	3.0	3.7	4.4	mA
$V_{D1,2}$	Bridge Diode Forward Voltage		I_{IN} = 3 mA	–	0.65		V
$V_{D3,4}$			I_{IN} = 3 mA	–	0.65		V
V_{OL}	Logic LOW Output Voltage		V_{CC} = 4.5 V, I_{OL} = 4.2 mA (Note 6)	–	0.04	0.4	V
I_{OH}	Logic HIGH Output Current		$V_{OH} = V_{CC}$ = 18 V (Note 6)	–	–	100	μA
I_{CCL}	Logic LOW Supply Current		$V_2 - V_3$ = 5.0 V V_O = Open V_{CC} = 5 V	–	1.0	4	mA
I_{CCH}	Logic HIGH Supply Current		V_{CC} = 18 V, V_O = Open	–	0.01	4	μA
C_{IN}	Input Capacitance		f = 1 mHz, V_{IN} = 0 V (Pins 2 & 3, Pins 1 & 4 Open)	–	50		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Logic LOW output level at pin 6 occurs when $V_{IN} \geq V_{TH+}$ and when $V_{IN} > V_{TH-}$ once V_{IN} exceeds V_{TH+}.
   Logic HIGH output level at pin 6 occurs when $V_{IN} \leq V_{TH-}$ and when $V_{IN} < V_{TH+}$ once decreases below V_{TH-}.

SWITCHING CHARACTERISTICS (T_A = 25°C, V_{CC} = 5 V unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay Time (to Output Low Level)	R_L = 4.7 kΩ, C_L = 30 pF (Note 7)		6.0	15	μs
t_{PLH}	Propagation Delay Time (to Output High Level)	R_L = 4.7 kΩ, C_L = 30 pF (Note 7)		25.0	40	μs
t_R	Output Rise Time (10%−90%)	R_L = 4.7 kΩ, C_L = 30 pF		45		μs
t_F	Output Fall Time (90%−10%)	R_L = 4.7 kΩ, C_L = 30 pF		0.5		μs
$\|CM_H\|$	Common Mode Transient Immunity (at Output High Level)	I_{IN} = 0 mA, R_L = 4.7 kΩ, V_{Omin} = 2.0 V, V_{CM} = 1400 V (Notes 8, 9)		4000		V/μs
$\|CM_L\|$	Common Mode Transient Immunity (at Output Low Level)	I_{IN} = 3.11 mA, R_L = 4.7 kΩ, V_{Omax} = 0.8 V, V_{CM} = 1400 V (Notes 8, 9)		600		V/μs

ISOLATION CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Withstand Isolation Voltage	RH ≤ 50%, I_{I-O} ≤ 10 μA, t = 1 min, f = 50 Hz (Note 10, 11)	5,000	–	–	VAC_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{IO} = 500 V_{DC} (Note 10)	–	10^{12}	–	Ω
C_{I-O}	Capacitance (Input to Output)	f = 1 MHz, V_{IO} = 0 V_{DC}	–	0.6	–	pF

7. T_{PHL} propagation delay is measured from the 2.5 V level of the leading edge of a 5.0 V input pulse (1 μs rise time) to the 1.5 V level on the leading edge of the output pulse. T_{PLH} propagation delay is measured on the trailing edges of the input and output pulse. (Refer to Fig. 10)
8. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V). Refer to Fig. 11.
9. In applications where dV_{cm}/dt may exceed 50,000 V/μs (Such as static discharge), a series resistor, R_{CC}, should be included to protect the detector chip from destructive surge currents. The recommended value for R_{CC} is 240 V per volt of allowable drop in V_{CC} (between pin 8 and V_{CC}) with a minimum value of 240 Ω.
10. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
11. The 5000 VAC_{RMS}/1 min. capability is validated by a 6000 VAC_{RMS}/1 sec. dielectric voltage withstand test.

TYPICAL PERFORMANCE CURVES

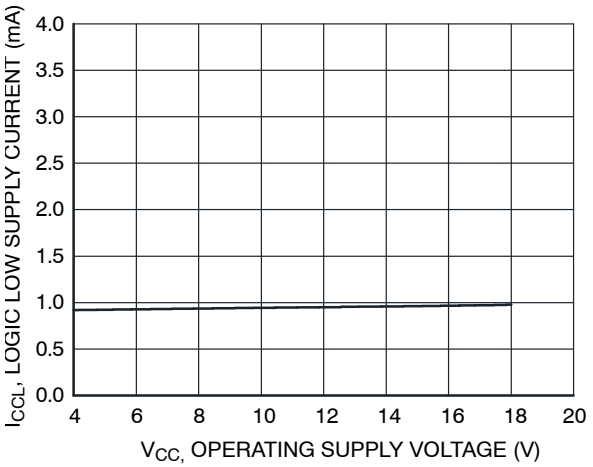


Figure 2. Logic Low Supply Current vs. Operating Supply Voltage

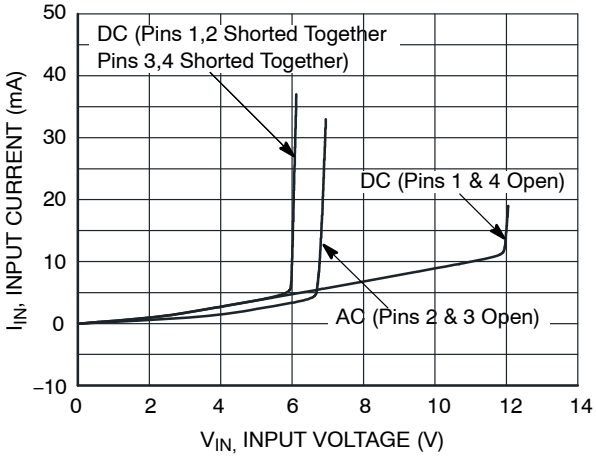


Figure 3. Input Current vs. Input Voltage

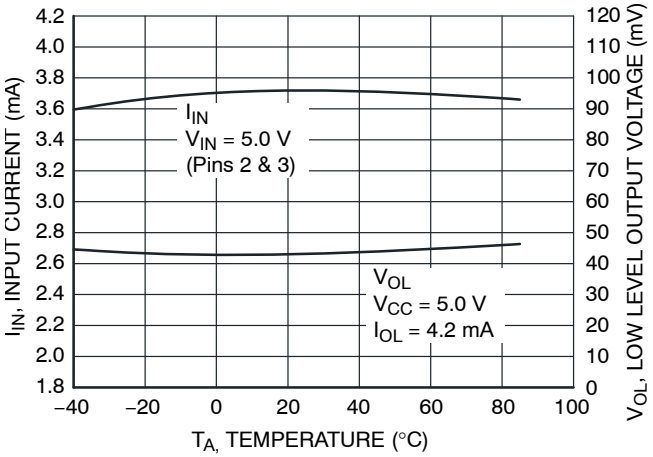


Figure 4. Input Current/Low Level Output Voltage vs. Temperature

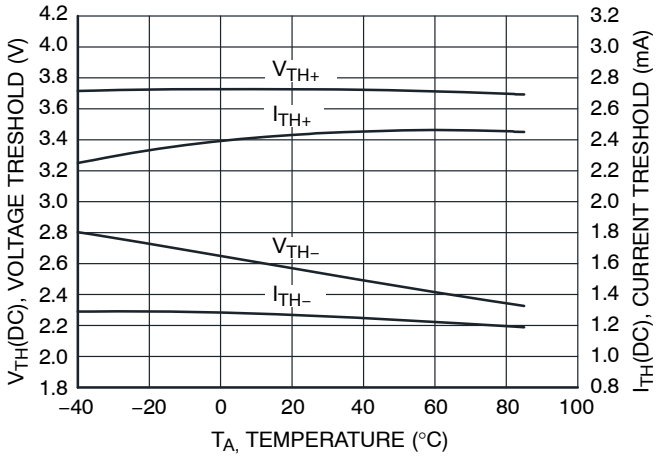


Figure 5. Current Threshold/Voltage Threshold vs. Temperature

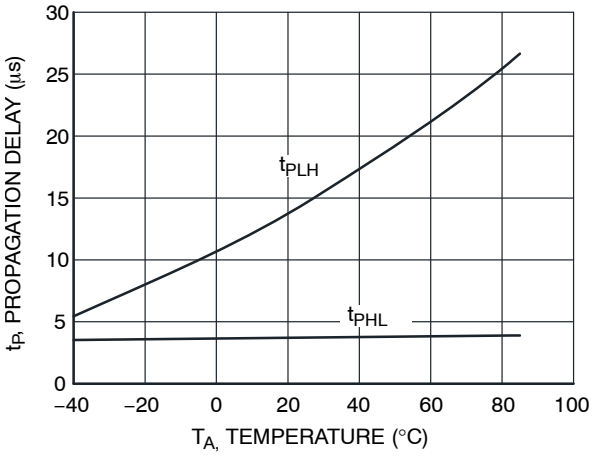


Figure 6. Propagation Delay vs. Temperature

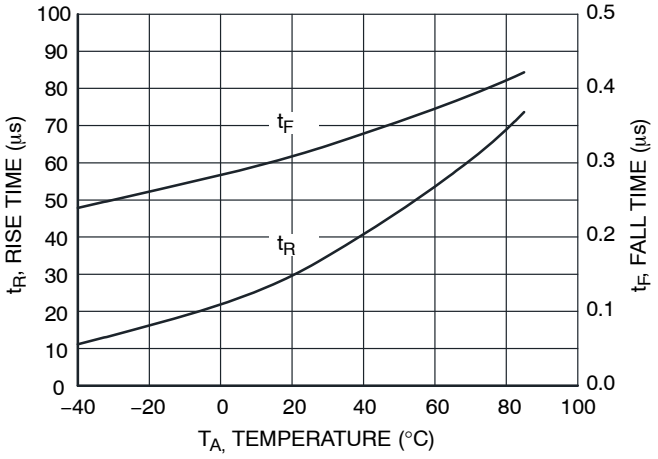


Figure 7. Rise and Fall Time vs. Temperature

TYPICAL PERFORMANCE CURVES (continued)

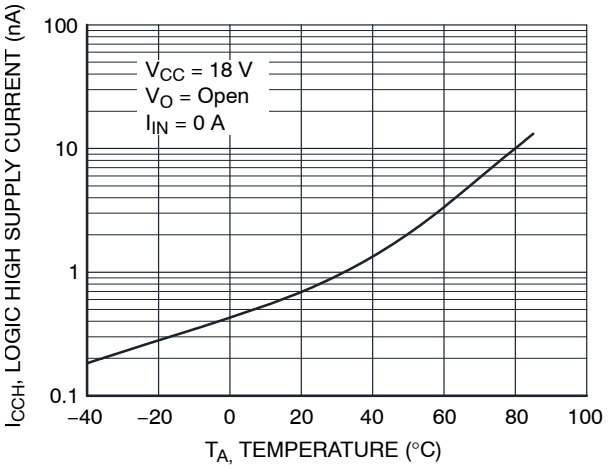


Figure 8. Logic High Supply Current vs. Temperature

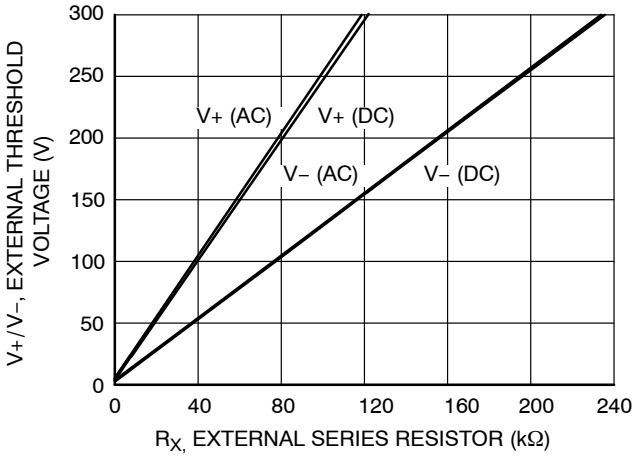


Figure 9. External Threshold Characteristics V+/V− vs. Rx

TEST CIRCUITS

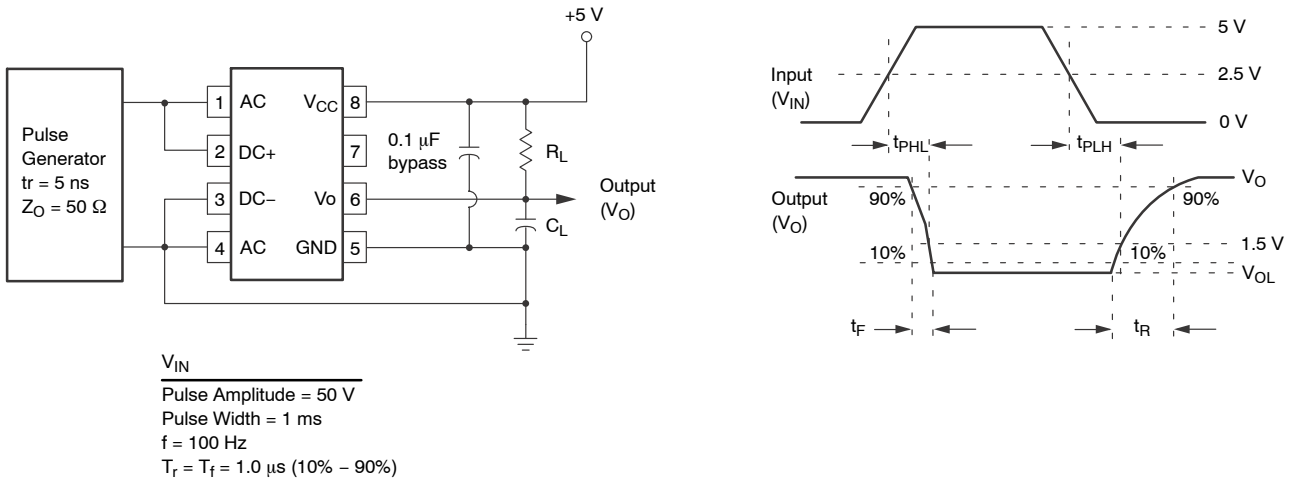


Figure 10. Switching Test Circuit

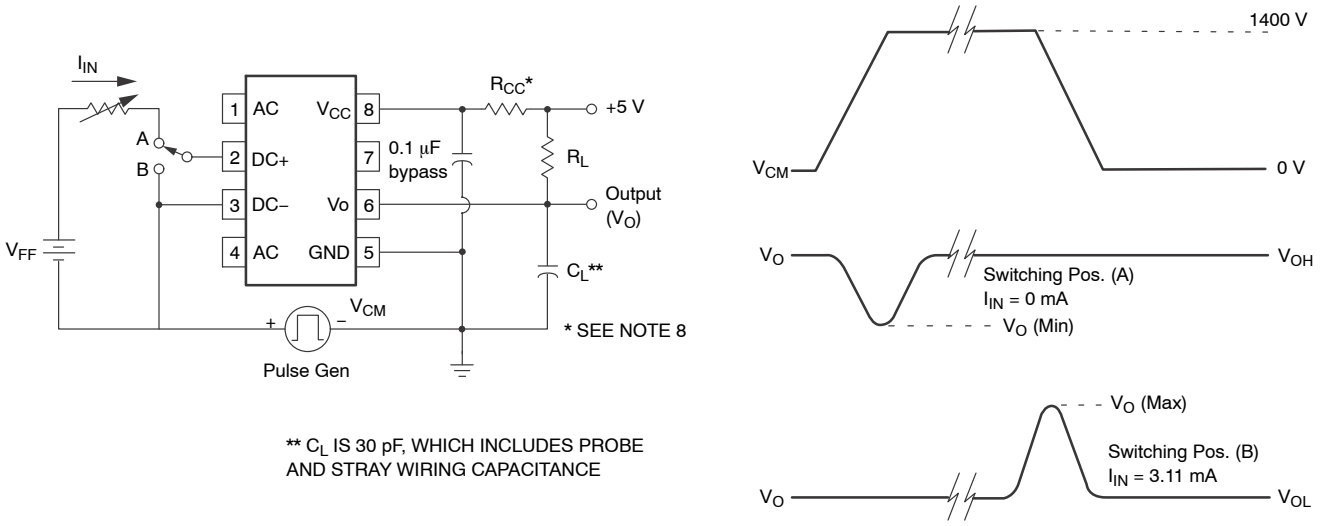
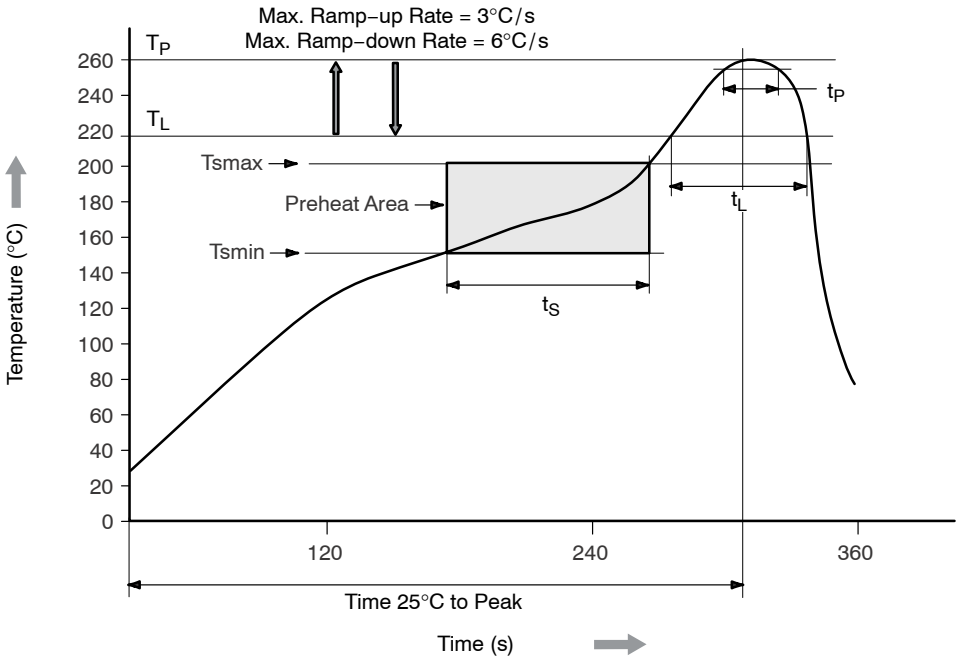


Figure 11. Test Circuit for Common Mode Transient Immunity and Typical Waveforms

REFLOW PROFILE



Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (Tsmin)	150°C
Temperature Maximum (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60 to 120 s
Ramp−up Rate (t_L to t_P)	3°C/s maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 to 150 s
Peak Body Package Temperature	260°C +0°C/−5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp−down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 12. Reflow Profile

ORDERING INFORMATION

Part Number	Package	Packing Method†
HCPL3700M	DIP 8−Pin	50 Units / Tube
HCPL3700SM	SMT 8−Pin (Lead Bend)	50 Units / Tube
HCPL3700SDM	SMT 8−Pin (Lead Bend)	1000 / Tape & Reel
HCPL3700VM	DIP 8−Pin, DIN EN/IEC60747−5−5 option	50 Units / Tube
HCPL3700SVM	SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 option	50 Units / Tube
HCPL3700SDVM	SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 option	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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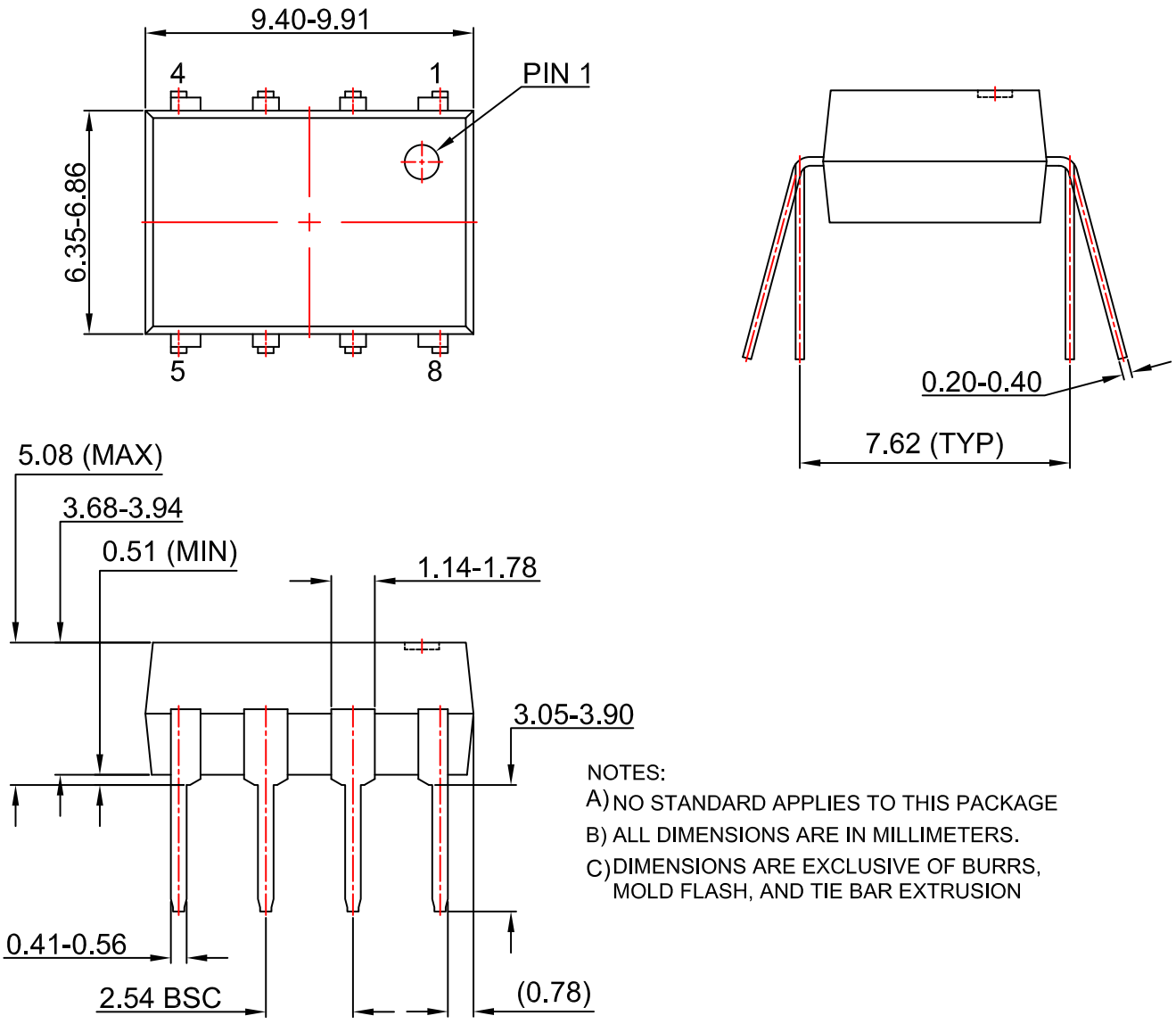
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



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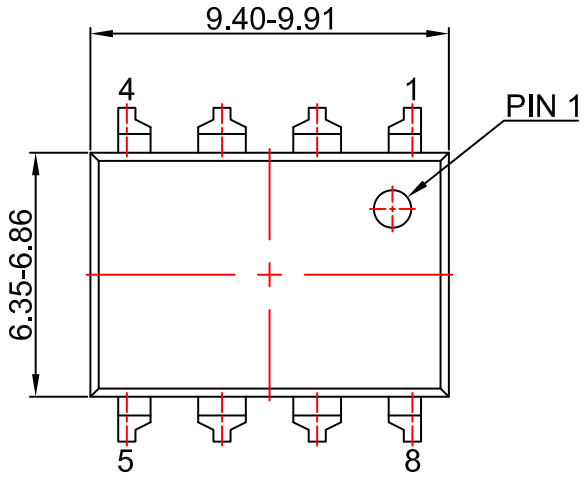
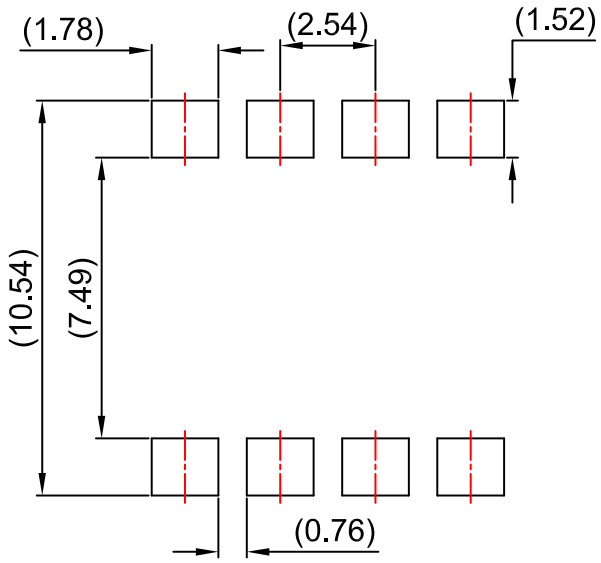
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

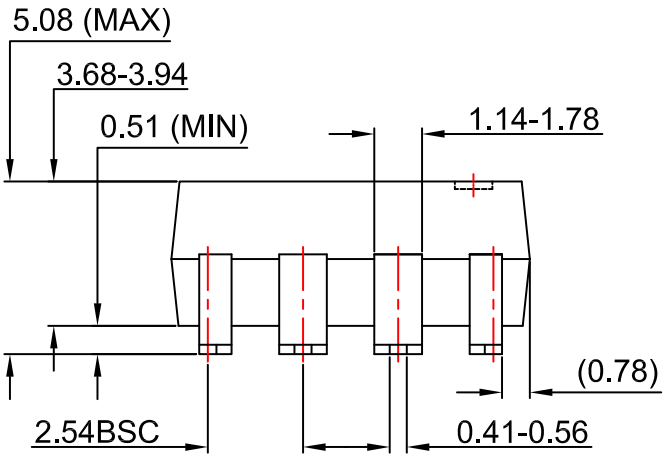
PDIP8 GW
CASE 709AC
ISSUE O

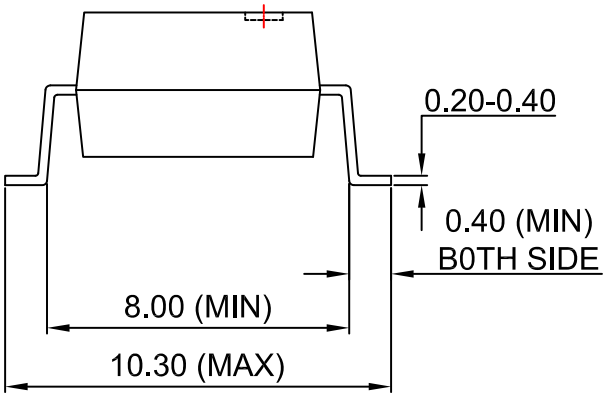
DATE 31 JUL 2016





LAND PATTERN RECOMMENDATION





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