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## FSQ100

### Green Mode Fairchild Power Switch (FPS™)

#### Features

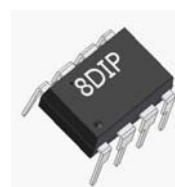
- Internal Avalanche-Rugged SenseFET
- Precision Fixed Operating Frequency: 67KHz
- Burst-Mode Operation
- Internal Startup Circuit
- Pulse-by-Pulse Current Limiting
- Over-Voltage Protection (OVP)
- Overload Protection (OLP)
- Internal Thermal Shutdown Function (TSD)
- Auto-Restart Mode
- Under-Voltage Lockout (UVLO) with Hysteresis
- Built-in Soft-Start
- Secondary-Side Regulation

#### Applications

- Charger & Adapter for Mobile Phone, PDA, MP3
- Auxiliary Power for White Goods, PC, C-TV, Monitor

#### Related Application Notes

- [AN-4137 — Design Guidelines for Off-line Flyback Converters using FPS™](#)
- [AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)
- [AN-4147 — Design Guidelines for RCD Snubber of Flyback](#)
- [AN-4134 — Design Guidelines for Off-line Forward Converters using FPS™](#)
- [AN-4138 — Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch \(FPS™\)](#)



#### Description

The FSQ100 consists of an integrated Pulse Width Modulator (PWM) and SenseFET, specifically designed for high-performance, off-line, Switch-Mode Power Supplies (SMPS) with minimal external components. This device is an integrated high-voltage power switching regulator that combines a VDMOS SenseFET with a voltage mode PWM control block. The integrated PWM controller features include a fixed oscillator, Under-Voltage Lockout (UVLO) protection, Leading Edge Blanking (LEB), an optimized gate turn-on/turn-off driver, Thermal Shutdown (TSD) protection, and temperature-compensated precision-current sources for loop compensation and fault protection circuitry.

When compared to a discrete MOSFET and controller or RCC solution, the FSQ100 device reduces total component count and design size and weight, while increasing efficiency, productivity, and system reliability. This device provides a basic platform well suited for cost-effective flyback converters.

#### Ordering Information

Product Number	Package	Marking Code	BV <sub>DSS</sub>	f <sub>osc</sub>	R <sub>DS(ON)</sub>
FSQ100	8-DIP	Q100	650V	67KHz	16Ω

FPS™ is a trademark of Fairchild Semiconductor Corporation.

## Typical Application

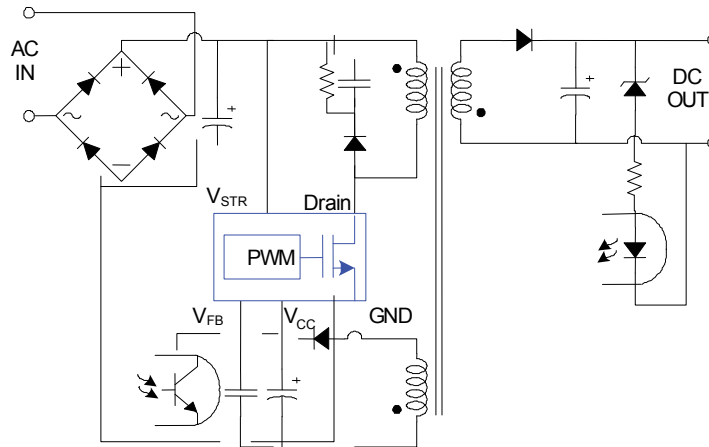


Figure 1. Typical Flyback Application

Table 1. Output Power Table

Product	Open Frame <sup>(1)</sup>	
	230V <sub>AC</sub> ±15% <sup>(2)</sup>	85~265V <sub>AC</sub>
FSQ100	13W	8W

### Notes:

1. Maximum practical continuous power in an open-frame design with sufficient drain pattern as a heat sinker, at 50°C ambient.
2. 230V<sub>AC</sub> or 100/115V<sub>AC</sub> with doubler.

## Internal Block Diagram

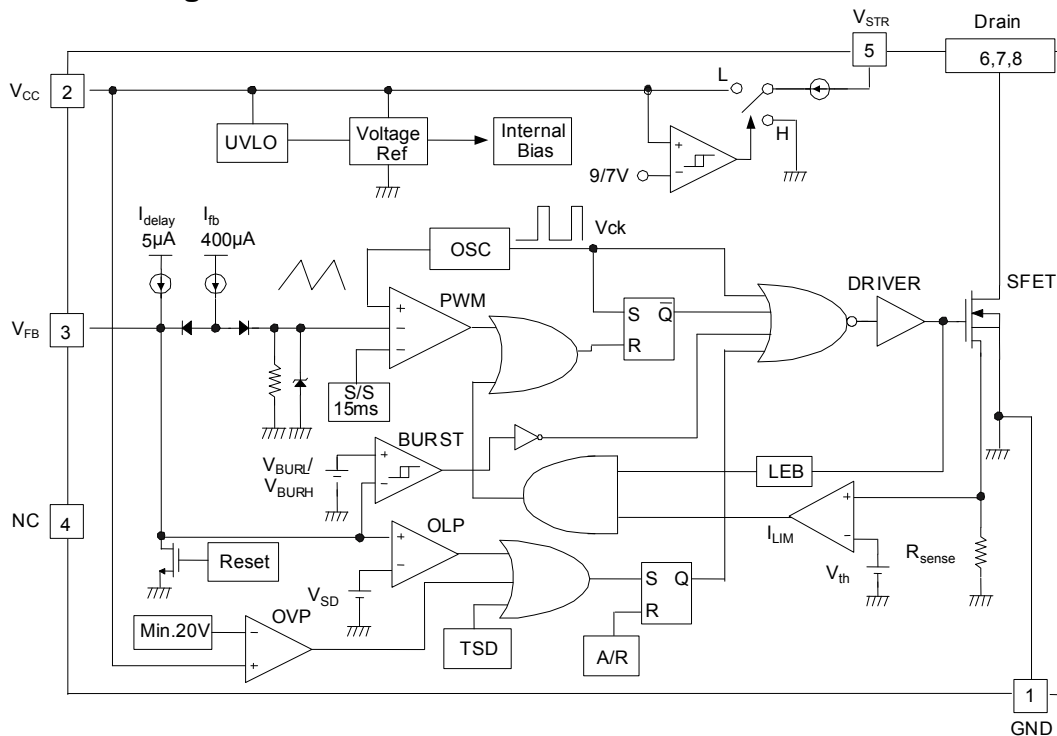


Figure 2. Functional Block Diagram

## Pin Assignments

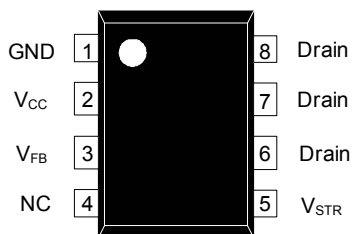


Figure 3. Pin Configuration (Top View)

## Pin Definitions

Pin #	Name	Description
1	GND	<b>Ground.</b> SenseFET source terminal on primary-side and internal control ground.
2	V <sub>CC</sub>	<b>Positive Supply Voltage Input.</b> Although connected to an auxiliary transformer winding, current is supplied from pin 5 (V <sub>STR</sub> ) via an internal switch during startup (see Figure 2). When V <sub>CC</sub> reaches the UVLO upper threshold (9V), the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	V <sub>FB</sub>	<b>Feedback.</b> Inverting input to the PWM comparator with its normal input level lies between 0.5V and 2.5V. It has a 0.4mA current source connected internally, while a capacitor and opto-coupler are typically connected externally. A feedback voltage of 4.5V triggers overload protection (OLP). There is a time delay while charging external capacitor C <sub>fb</sub> from 3V to 4.5V using an internal 5μA current source. This time delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate in true overload conditions.
4	NC	<b>No Connection.</b>
5	V <sub>STR</sub>	<b>Startup.</b> This pin connects directly to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the V <sub>CC</sub> pin and ground. Once the V <sub>CC</sub> reaches 9V, the internal switch stops charging the capacitor.
6,7,8	Drain	<b>SenseFET Drain.</b> The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Value	Unit
$V_{\text{DRAIN}}$	Drain Pin Voltage	650	V
$V_{\text{STR}}$	VSTR Pin Voltage	650	V
$V_{\text{DG}}$	Drain-Gate Voltage	650	V
$V_{\text{GS}}$	Gate-Source Voltage	$\pm 20$	V
$V_{\text{CC}}$	Supply Voltage	20	V
$V_{\text{FB}}$	Feedback Voltage Range	-0.3 to $V_{\text{STOP}}$	V
$P_{\text{D}}$	Total Power Dissipation	1.40	W
$T_{\text{J}}$	Operating Junction Temperature	Internally limited	$^\circ\text{C}$
$T_{\text{A}}$	Operating Ambient Temperature	-25 to +85	$^\circ\text{C}$
$T_{\text{STG}}$	Storage Temperature	-55 to +150	$^\circ\text{C}$

### Notes:

1. Repetitive rating: Pulse width is limited by maximum junction temperature.
2.  $L = 24\text{mH}$ , starting  $T_{\text{J}} = 25^\circ\text{C}$ .

## Thermal Impedance

$T_A = 25^\circ\text{C}$ , unless otherwise specified. All items are tested with the JEDEC standards JESD 51-2 and 51-10 (DIP).

Symbol	Parameter	Value	Unit
$\theta_{\text{JA}}$	Junction-to-Ambient Thermal Impedance <sup>(3)</sup>	88.84	$^\circ\text{C/W}$
$\theta_{\text{JC}}$	Junction-to-Case Thermal Impedance <sup>(4)</sup>	13.94	$^\circ\text{C/W}$

### Notes:

3. Free-standing with no heatsink; without copper clad. Measurement condition; just before junction temperature  $T_{\text{J}}$  enters into OTP.
4. Measured on the DRAIN pin close to plastic interface.

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ , unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
SenseFET Section						
I <sub>DSS</sub>	Zero-Gate-Voltage Drain Current	V <sub>DS</sub> =650V, V <sub>GS</sub> =0V			25	μA
		V <sub>DS</sub> =520V, V <sub>GS</sub> =0V, T <sub>C</sub> =125°C			200	
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance <sup>(5)</sup>	V <sub>GS</sub> =10V, I <sub>D</sub> =0.5A		16	22	Ω
g <sub>fs</sub>	Forward Trans-Conductance	V <sub>DS</sub> =50V, I <sub>D</sub> =0.5A	1.0	1.3		S
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> =0V, V <sub>DS</sub> =25V, f=1MHz		162		pF
C <sub>OSS</sub>	Output Capacitance			18		
C <sub>RSS</sub>	Reverse Transfer Capacitance			3.8		
Control Section						
f <sub>OSC</sub>	Switching Frequency		61	67	73	kHz
Δf <sub>OSC</sub>	Switching Frequency Variation <sup>(6)</sup>	-25°C ≤ T <sub>A</sub> ≤ 85°C		±5	±10	%
D <sub>MAX</sub>	Maximum Duty Cycle		60	67	74	%
V <sub>START</sub>	UVLO Threshold Voltage	V <sub>FB</sub> =GND	8	9	10	V
V <sub>STOP</sub>		V <sub>FB</sub> =GND	6	7	8	V
I <sub>FB</sub>	Feedback Source Current	0V ≤ V <sub>FB</sub> ≤ 3V	0.35	0.40	0.45	mA
t <sub>S/S</sub>	Internal Soft Start Time		10	15	20	ms
Burst Mode Section						
V <sub>BURH</sub>	Burst Mode Voltage	T <sub>J</sub> =25°C	0.6	0.7	0.8	V
V <sub>BURL</sub>			0.45	0.55	0.65	V
V <sub>BUR(HYS)</sub>		Hysteresis		150		mV
Protection Section						
I <sub>LIM</sub>	Peak Current Limit		0.475	0.550	0.650	A
T <sub>SD</sub>	Thermal Shutdown Temperature <sup>(7)</sup>		125	145		°C
V <sub>SD</sub>	Shutdown Feedback Voltage		4.0	4.5	5.0	V
V <sub>OVP</sub>	Over-Voltage Protection		20			V
I <sub>DELAY</sub>	Shutdown Delay Current	3V ≤ V <sub>FB</sub> ≤ V <sub>SD</sub>	4	5	6	μA
Total Device Section						
I <sub>OP</sub>	Operating Supply Current <sup>(8)</sup>	V <sub>CC</sub> ≤ 16V		1.5	3.0	mA
I <sub>CH</sub>	Startup Charging Current	V <sub>CC</sub> =0V , V <sub>STR</sub> =50V	450	550	650	μA

### Notes:

- Pulse test: Pulse width  $\leq 300\mu\text{s}$ , duty  $\leq 2\%$ .
- These parameters, although guaranteed, are tested in EDS (wafer test) process.
- These parameters, although guaranteed, are not 100% tested in production.
- Control part only.

## Typical Performance Characteristics

These characteristic graphs are normalized at  $T_A = 25^\circ\text{C}$ .

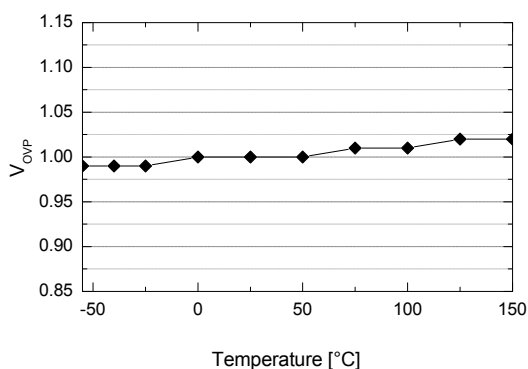


Figure 4. Over-Voltage Protection ( $V_{OVP}$ ) vs.  $T_A$

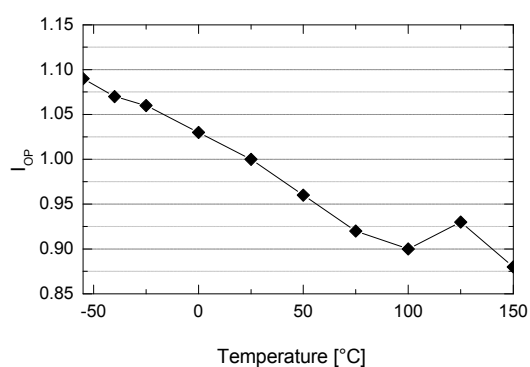


Figure 5. Operating Supply Current ( $I_{OP}$ ) vs.  $T_A$

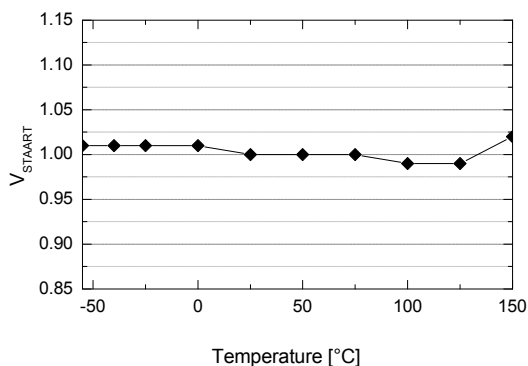


Figure 6. Start Threshold Voltage ( $V_{START}$ ) vs.  $T_A$

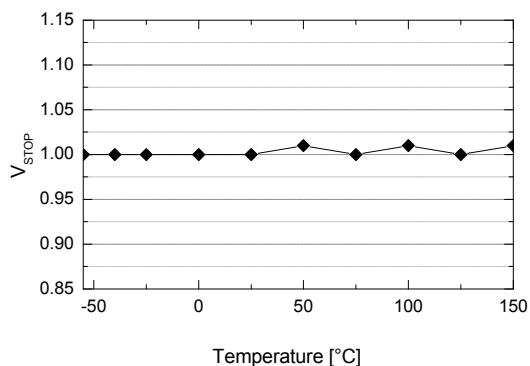


Figure 7. Stop Threshold Voltage ( $V_{STOP}$ ) vs.  $T_A$

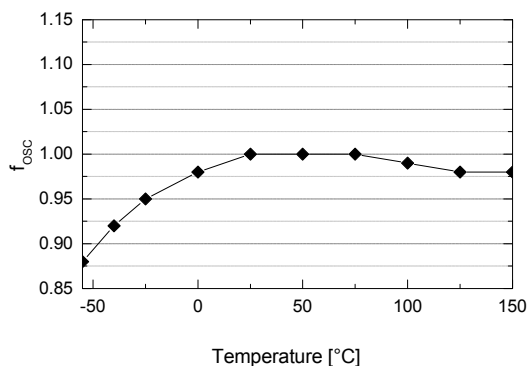


Figure 8. Operating Frequency ( $f_{osc}$ ) vs.  $T_A$

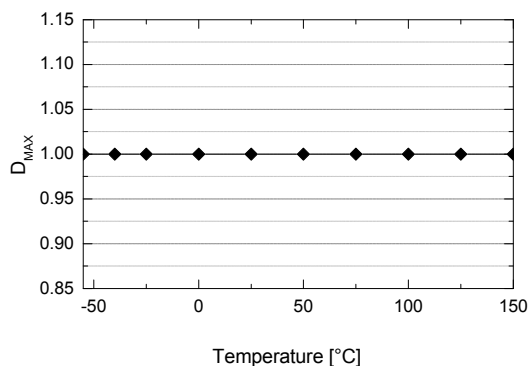
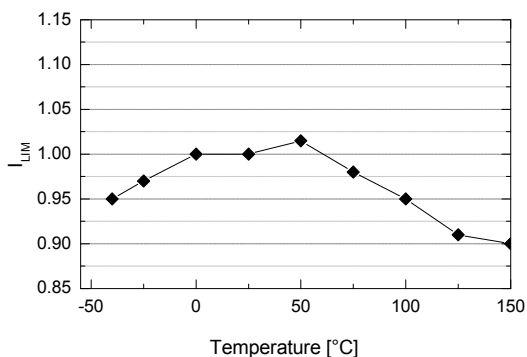


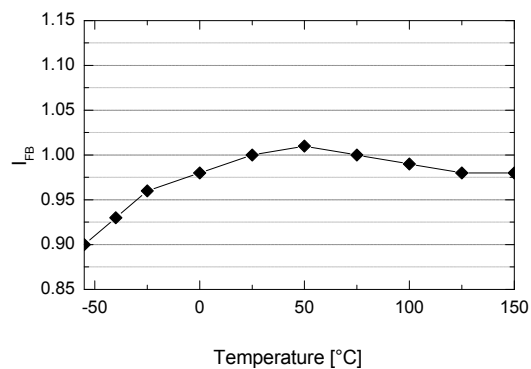
Figure 9. Maximum Duty Cycle ( $D_{MAX}$ ) vs.  $T_A$

## Typical Performance Characteristics (Continued)

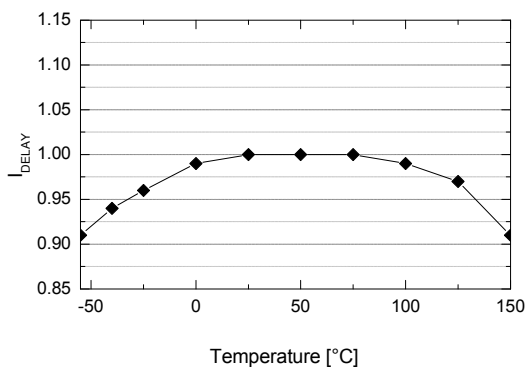
These characteristic graphs are normalized at  $T_A = 25^\circ\text{C}$ .



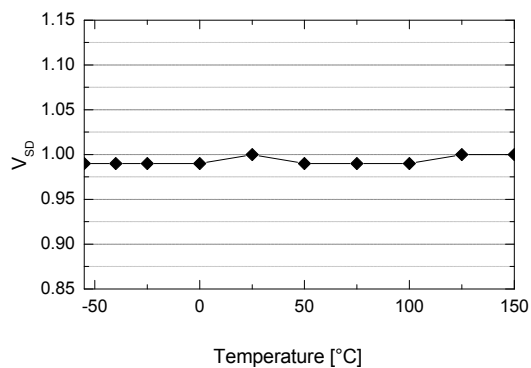
**Figure 10. Peak Current Limit ( $I_{\text{LIM}}$ ) vs.  $T_A$**



**Figure 11. Feedback Source Current ( $I_{\text{FB}}$ ) vs.  $T_A$**



**Figure 12. Shutdown Delay Current ( $I_{\text{DELAY}}$ ) vs.  $T_A$**



**Figure 13. Shutdown Feedback Voltage ( $V_{\text{SD}}$ ) vs.  $T_A$**



## Functional Description

**1. Startup:** At startup, the internal high-voltage current source supplies the internal bias and charges the external  $V_{CC}$  capacitor, as shown in Figure 14. When  $V_{CC}$  reaches 9V, the device starts switching and the internal high-voltage current source stops charging the capacitor. The device is in normal operation provided  $V_{CC}$  does not drop below 7V. After startup, the bias is supplied from the auxiliary transformer winding.

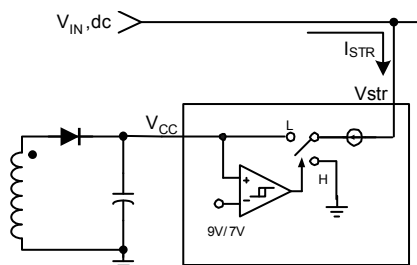


Figure 14. Internal Startup Circuit

Calculating the  $V_{CC}$  capacitor is an important step to design with the FSQ100. At initial startup, the maximum value of start operating current  $I_{START}$  is about 100 $\mu$ A, which supplies current to UVLO and  $V_{REF}$  blocks. The charging current  $I_{VCC}$  of the  $V_{CC}$  capacitor is equal to  $I_{STR} - 100\mu A$ . After  $V_{CC}$  reaches the UVLO start voltage, only the bias winding supplies  $V_{CC}$  current to the device. When the bias winding voltage is not sufficient, the  $V_{CC}$  level decreases to the UVLO stop voltage and the internal current source is activated again to charge the  $V_{CC}$  capacitor. To prevent this  $V_{CC}$  fluctuation (charging/discharging), the  $V_{CC}$  capacitor should be chosen to have a value between 10 $\mu$ F and 47 $\mu$ F.

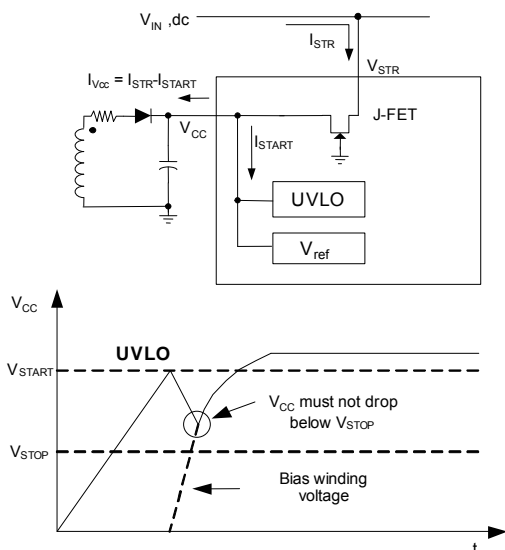


Figure 15. Charging  $V_{CC}$  Capacitor through  $V_{str}$

**2. Feedback Control:** The FSQ100 is a voltage mode controlled device, as shown in Figure 16. Usually, an opto-coupler and shunt regulator, like KA431 are used to implement the feedback network. The feedback voltage is compared with an internally generated sawtooth waveform. This directly controls the duty cycle.

When the shunt regulator reference pin voltage exceeds the internal reference voltage of 2.5V, the opto-coupler LED current increases, the feedback voltage  $V_{FB}$  is pulled down, and it reduces the duty cycle. This happens when the input voltage increases or the output load decreases.

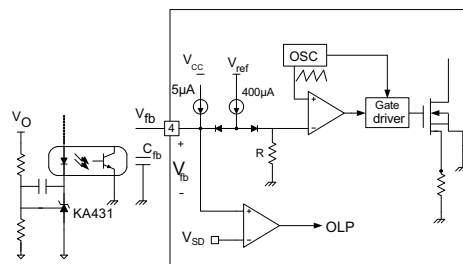


Figure 16. PWM and Feedback Circuit

**3. Leading Edge Blanking (LEB):** At the instant the internal SenseFET is turned on, the primary-side capacitance and secondary-side rectifier diode reverse recovery typically causes a high-current spike through the SenseFET. Excessive voltage across the  $R_{SENSE}$  resistor lead to incorrect pulse-by-pulse current limit protection. To avoid this, a leading edge blanking (LEB) circuit disables pulse-by-pulse current-limit protection block for a fixed time ( $t_{LEB}$ ) after the SenseFET turns on.

**4. Protection Circuit:** The FSQ100 has protective functions, such as overload protection (OLP), over voltage protection (OVP), under-voltage lockout (UVLO), and thermal shutdown (TSD). Because these protection circuits are fully integrated inside the IC without external components, reliability is improved without increasing costs. Once a fault condition occurs, switching is terminated and the SenseFET remains off. This causes  $V_{CC}$  to fall. When  $V_{CC}$  reaches the UVLO stop voltage  $V_{STOP}$  (7V), the protection is reset and the internal high-voltage current source charges the  $V_{CC}$  capacitor via the  $V_{STR}$  pin. When  $V_{CC}$  reaches the UVLO start voltage  $V_{START}$  (9V), the device resumes normal operation. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated.

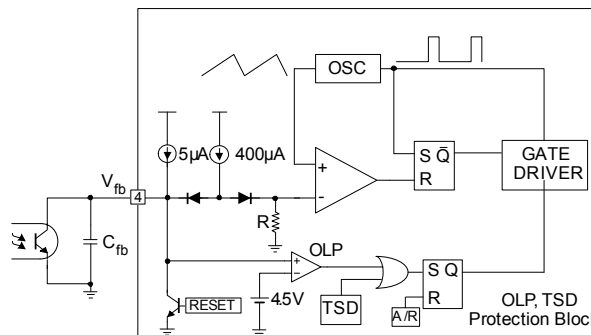


Figure 17. Protection Block



## Application Tips

### 1. Methods of Reducing Audible Noise

Switching mode power converters have electronic and magnetic components that generate audible noise when the operating frequency is in the range of 20~20,000Hz. Even though they operate above 20kHz, they can make noise, depending on the load condition. Designers can employ several methods to reduce noise.

#### Glue or Varnish

The most common method involves using glue or varnish to tighten magnetic components. The motion of core, bobbin and coil, and the chattering or magnetostriction of core can cause the transformer to produce audible noise. The use of rigid glue and varnish helps reduce the transformer noise, but can crack the core. This is because sudden changes in the ambient temperature cause the core and the glue to expand or shrink in a different ratio.

#### Ceramic Capacitor

Using a film capacitor instead of a ceramic capacitor as a snubber capacitor is another noise-reduction solution. Some dielectric materials show a piezoelectric effect, depending on the electric field intensity. Hence, a snubber capacitor becomes one of the most significant sources of audible noise. It is possible to use a Zener clamp circuit instead of an RCD snubber for higher efficiency as and lower audible noise.

#### Adjusting Sound Frequency

Moving the fundamental frequency of noise out of 2~4kHz range is the third method. Generally, humans are more sensitive to noise in the range of 2~4kHz. When the fundamental frequency of noise is located in this range, the noise is perceived as louder, although the noise intensity level is identical (refer to Figure 22 Equal Loudness Curves).

When FPS acts in burst mode and the burst operation is suspected to be a source of noise, this method may be helpful. If the frequency of burst-mode operation lies in the range of 2~4 kHz, adjusting the feedback loop can shift the burst operation frequency. To reduce the burst operation frequency, increase a feedback gain capacitor ( $C_F$ ), opto-coupler supply resistor ( $R_D$ ), and feedback capacitor ( $C_B$ ); and decrease a feedback gain resistor ( $R_F$ ), as shown in Figure 23.

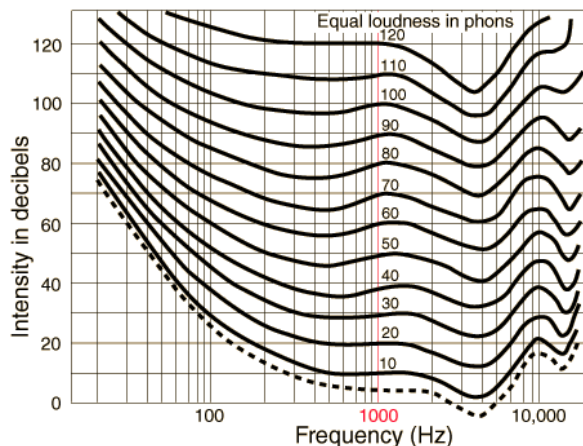


Figure 22. Equal Loudness Curves

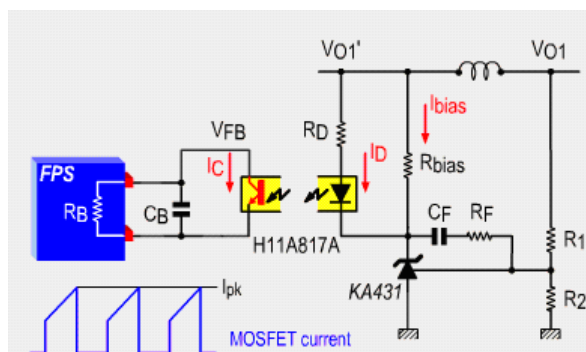


Figure 23. Typical Feedback Network of FPS™

### 2. Reference Materials

[AN-4134 — Design Guidelines for Off-line Forward Converters using FPS™](#)

[AN-4137 — Design Guidelines for Off-line Flyback Converters using FPS™](#)

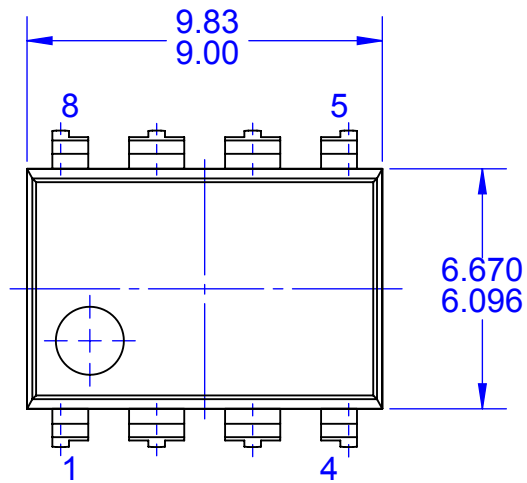
[AN-4138 — Design Considerations for Battery Charger Using Green Mode Fairchild Power Switch \(FPS™\)](#)

[AN-4140 — Transformer Design Consideration for Off-line Flyback Converters Using Fairchild Power Switch \(FPS™\)](#)

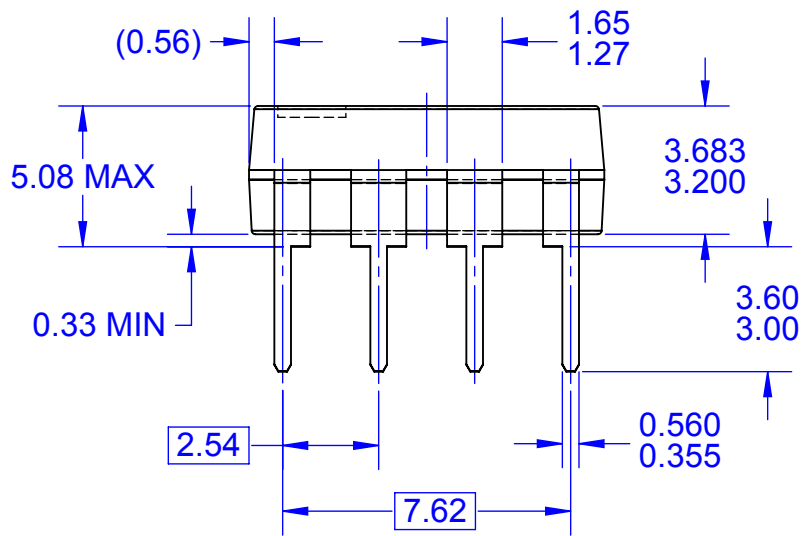
[AN-4141 — Troubleshooting and Design Tips for Fairchild Power Switch \(FPS™\) Flyback Applications](#)

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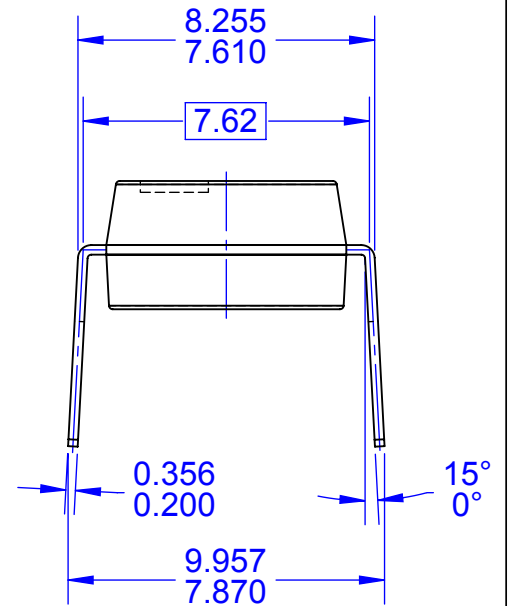
[AN-4148 — Audible Noise Reduction Techniques for FPS™ Applications](#)



TOP VIEW



FRONT VIEW



SIDE VIEW

NOTES:

- CONFORMS TO JEDEC MS-001, VARIATION BA
- ALL DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
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