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ON Semiconductor®

## FQU2N50B

# N-Channel QFET® MOSFET

500 V, 1.6 A, 5.3 Ω

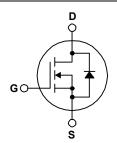
### Description

This N-Channel enhancement mode power MOSFET is produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

#### **Features**

- 1.6 A, 500 V,  $R_{DS(on)}$  = 5.3  $\Omega$  (Max.) @  $V_{GS}$  = 10 V,  $I_{D}$  = 0.8 A
- Low Gate Charge (Typ. 6.0 nC)
- Low Crss (Typ. 4.3 pF)
- · Fast Switching
- · 100% Avalanche Tested
- · Improved dv/dt Capability





## Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQU2N50BTU-WS	Units
V <sub>DSS</sub>	Drain-Source Voltage		500	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		1.6	А
	- Continuous (T <sub>C</sub> = 100°C	C)	1.0	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	6.4	А
V <sub>GSS</sub>	Gate-Source Voltage		± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	1.6	А
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	3.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>A</sub> = 25°C) *		2.5	W
	Power Dissipation (T <sub>C</sub> = 25°C)		30	W
	- Derate above 25°C		0.24	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	Э	-55 to +150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering 1/8" from Case for 5 Seconds	,	300	°C

#### **Thermal Characteristics**

Symbol	Parameter	FQU2N50BTU_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.17	
В	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	50	

Package Marking and Ordering Information	Package	Marking	and	<b>Orderina</b>	Information
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Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU2N50BTU-WS	FQU2N50B	I-PAK	Tube	N/A	N/A	75 units

## Electrical Characteristics T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Cha	racteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
$\Delta BV_{DSS}$ / $\Delta T_{J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		0.48		V/°C
I <sub>DSS</sub>	Zoro Coto Voltogo Droin Current	V <sub>DS</sub> = 500 V, V <sub>GS</sub> = 0 V			1	μΑ
	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C			10	μА
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -30 V, V <sub>DS</sub> = 0 V			-100	nA

#### On Characteristics

V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	2.3	3.0	3.7	V
		$V_{DS} = V_{GS}$ , $I_D = 250 \text{ mA}$	3.6	4.3	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.8 A		4.2	5.3	Ω
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 50 \text{ V}, I_{D} = 0.8 \text{ A}$		1.3		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,	 180	230	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz	 30	40	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		 4	6	pF

#### **Switching Characteristics**

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 250 V, I <sub>D</sub> = 2.1 A,	 6	20	ns
t <sub>r</sub>	Turn-On Rise Time	$R_G = 25 \Omega$	 25	60	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	11.6	 10	30	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)	 20	50	ns
$Q_g$	Total Gate Charge	$V_{DS} = 400 \text{ V}, I_{D} = 2.1 \text{ A},$	 6.0	8.0	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V	 1.3		nC
Q <sub>gd</sub>	Gate-Drain Charge	(Note 4)	 3.0		nC

#### **Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current		 	1.6	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		 	6.4	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.6 A	 	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0 \text{ V, } I_{S} = 2.1 \text{ A,}$	 195		ns
Q <sub>rr</sub>	Reverse Recovery Charge	$dI_F / dt = 100 A/\mu s$	 0.69		μС

- Notes: 
  1. Repetitive rating : pulse-width limited by maximum junction temperature. 
  2. L = 85 mH,  $I_{AS}$  = 1.6 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C. 
  3.  $I_{SD}$  ≤ 2.1 A, di/dt ≤ 200 A/ $\mu$ s,  $V_{DD}$  ≤ BV $_{DSS}$ , starting  $T_{J}$  = 25°C. 
  4. Essentially independent of operating temperature.

## **Typical Characteristics**

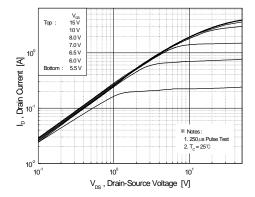


Figure 1. On-Region Characteristics

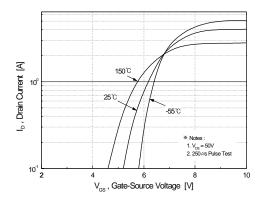


Figure 2. Transfer Characteristics

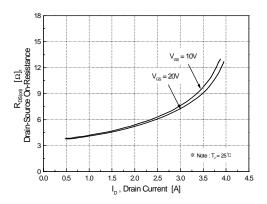


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

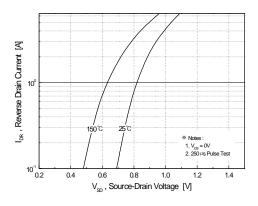


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

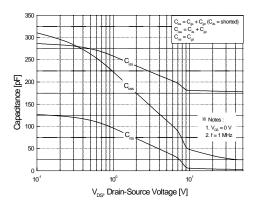


Figure 5. Capacitance Characteristics

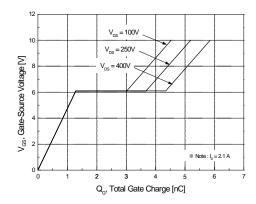


Figure 6. Gate Charge Characteristics

## Typical Characteristics (Continued)

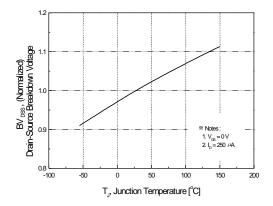


Figure 7. Breakdown Voltage Variation vs. Temperature

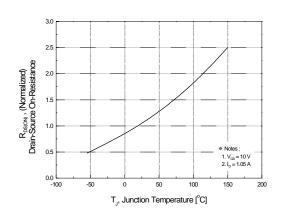


Figure 8. On-Resistance Variation vs. Temperature

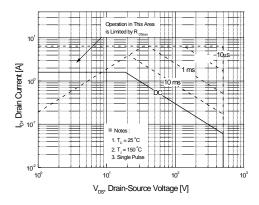


Figure 9. Maximum Safe Operating Area

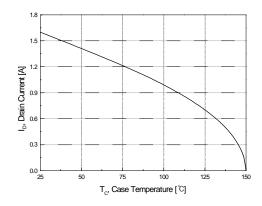


Figure 10. Maximum Drain Current vs. Case Temperature

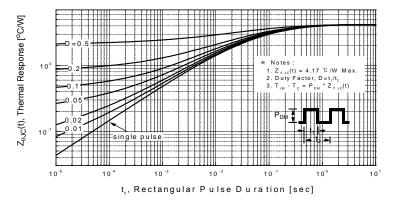


Figure 11. Transient Thermal Response Curve

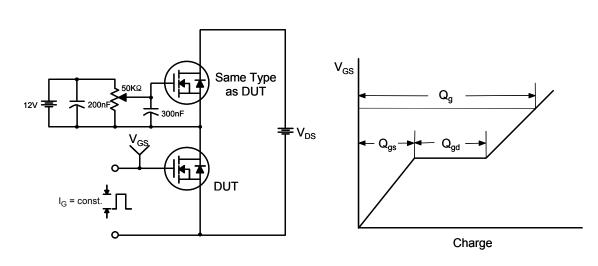


Figure 12. Gate Charge Test Circuit & Waveform

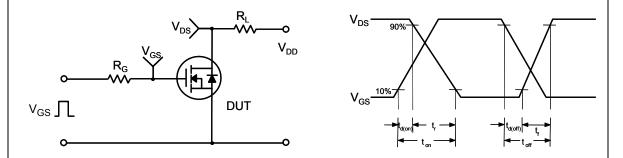


Figure 13. Resistive Switching Test Circuit & Waveforms

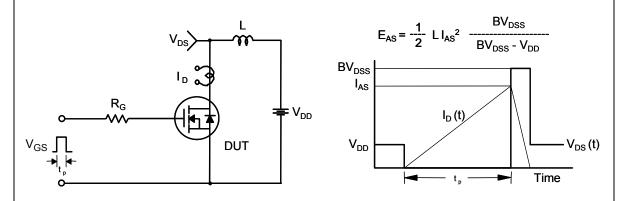
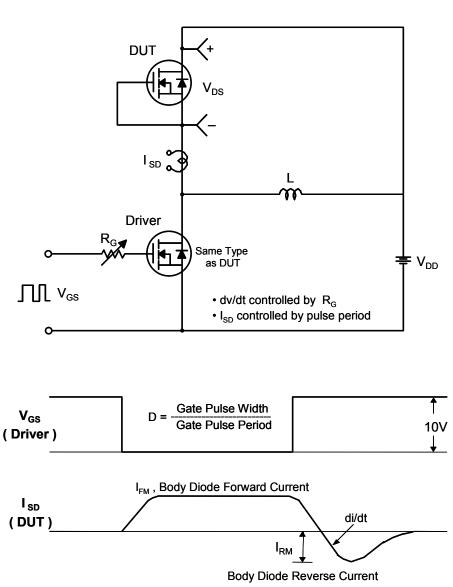


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



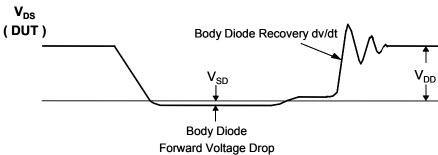
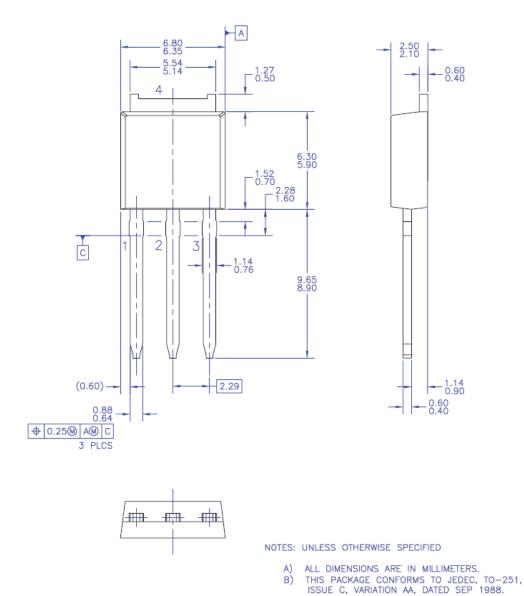


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

#### **Mechanical Dimensions**



- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

Figure 16. TO-251 (I-PAK), Molded, 3-Lead, Option AA

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