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# FQT2P25

## P-Channel QFET® MOSFET

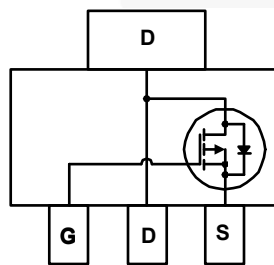
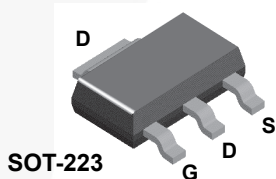
-250 V, -0.55 A, 4.0  $\Omega$

### Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

### Features

- -0.55 A, -250 V,  $R_{DS(on)} = 4.0 \Omega$  (Max.) @  $V_{GS} = -10$  V,  $I_D = -0.275$  A
- Low Gate Charge (Typ. 6.5 nC)
- Low  $C_{rss}$  (Typ. 6.5 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQT2P25TF	Unit
$V_{DSS}$	Drain-Source Voltage	-250	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	-0.55	A
		-0.35	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-2.2	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	120	mJ
$I_{AR}$	Avalanche Current (Note 1)	-0.55	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	0.25	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	-5.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate above $25^\circ\text{C}$	2.5	W
		0.02	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQT2P25TF	Unit
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	50	$^\circ\text{C}/\text{W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQT2P25TF	FQT2P25	SOT-223	Tape and Reel	13 "	12 mm	4000 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-250	--	--	V
$\Delta B_{VDSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.2	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -250\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -200\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -0.275\text{ A}$	--	3.15	4.0	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -0.275\text{ A}$	--	0.6	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	190	250	pF
$C_{oss}$	Output Capacitance		--	40	55	pF
$C_{rss}$	Reverse Transfer Capacitance		--	6.5	8.5	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -125\text{ V}, I_D = -2.3\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4)	--	8.5	25	ns
$t_r$	Turn-On Rise Time		--	40	90	ns
$t_{d(off)}$	Turn-Off Delay Time		--	12	35	ns
$t_f$	Turn-Off Fall Time		--	25	60	ns
$Q_g$	Total Gate Charge	$V_{DS} = -200\text{ V}, I_D = -2.3\text{ A},$ $V_{GS} = -10\text{ V}$  (Note 4)	--	6.5	8.5	nC
$Q_{gs}$	Gate-Source Charge		--	1.8	--	nC
$Q_{gd}$	Gate-Drain Charge		--	3.0	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	-0.55	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-2.2	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.55 A	--	--	-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.3 A,	--	110	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs	--	0.4	--	μC

#### Notes:

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 635\text{ mH}$ ,  $I_{AS} = -0.55\text{ A}$ ,  $V_{DD} = -50\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -2.3\text{ A}$ ,  $di/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

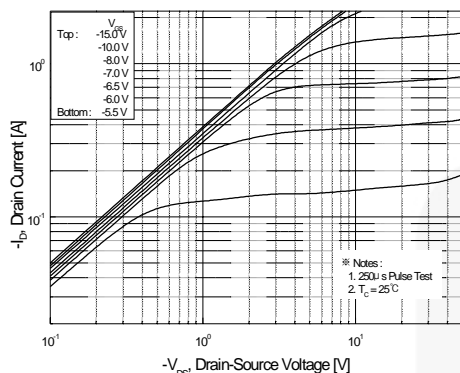


Figure 1. On-Region Characteristics

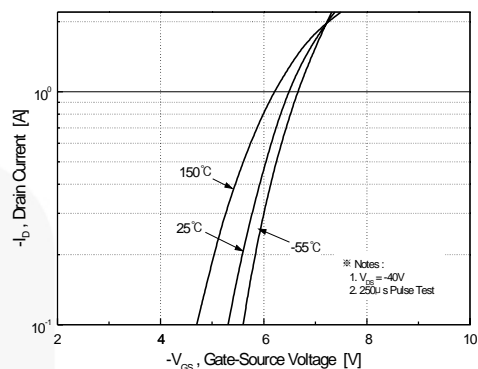


Figure 2. Transfer Characteristics

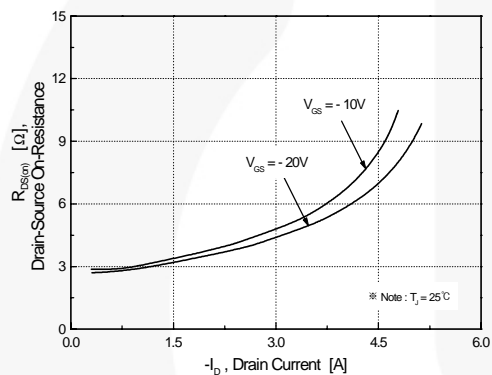


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

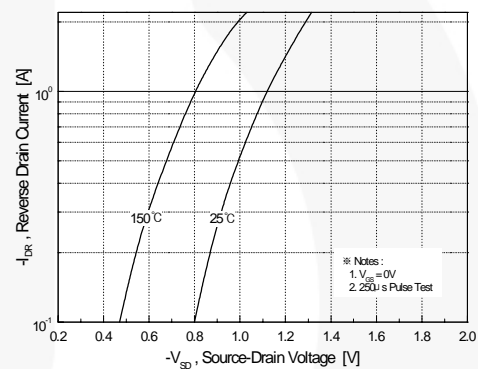


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

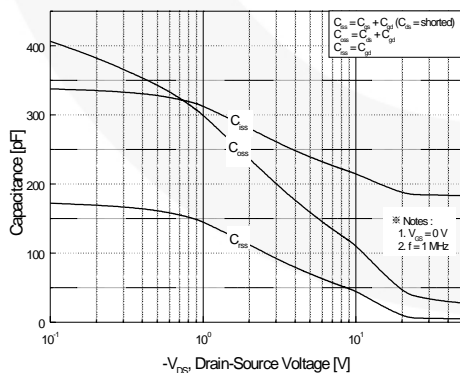


Figure 5. Capacitance Characteristics

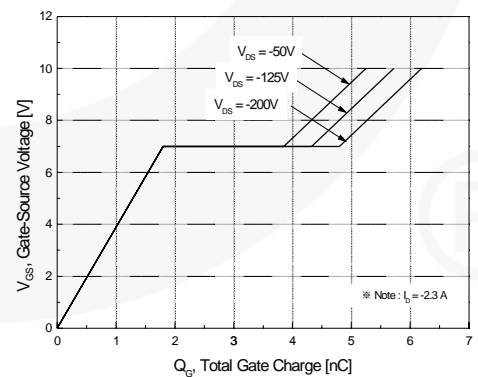


Figure 6. Gate Charge Characteristics

## Typical Characteristics (Continued)

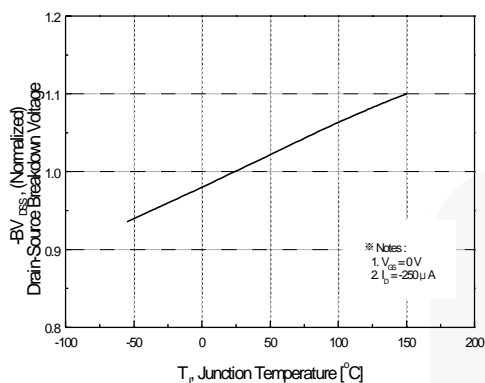


Figure 7. Breakdown Voltage Variation vs. Temperature

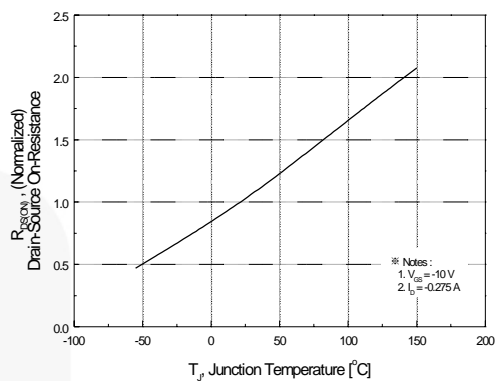


Figure 8. On-Resistance Variation vs. Temperature

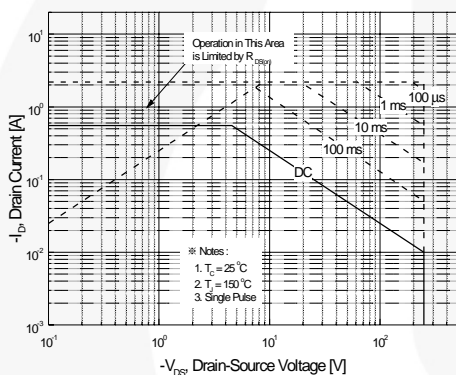


Figure 9. Maximum Safe Operating Area

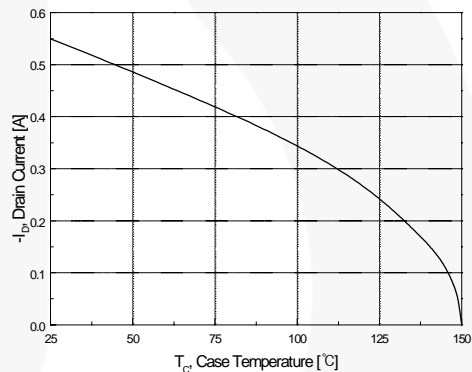


Figure 10. Maximum Drain Current vs. Case Temperature

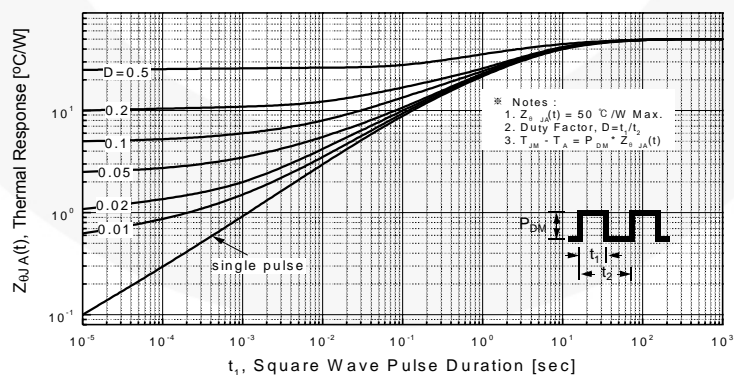


Figure 11. Transient Thermal Response Curve

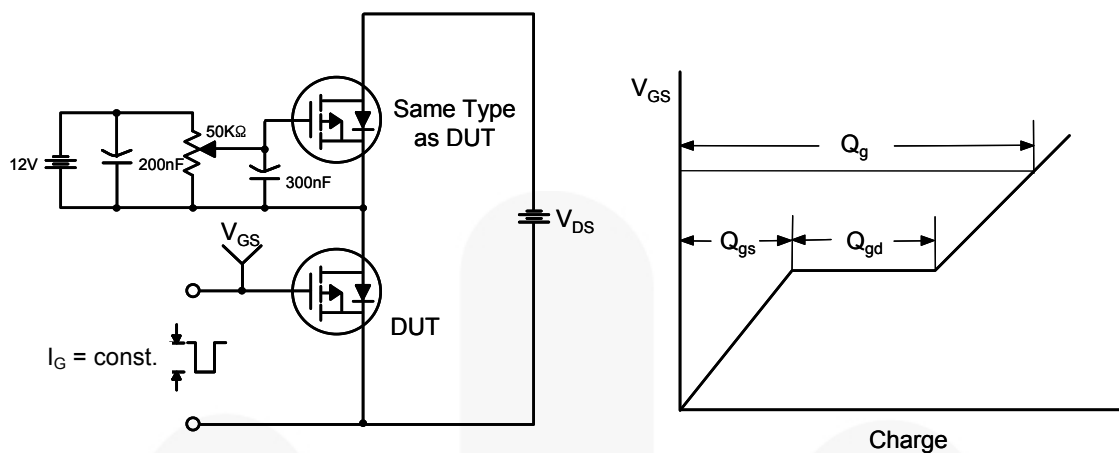


Figure 12. Gate Charge Test Circuit & Waveform

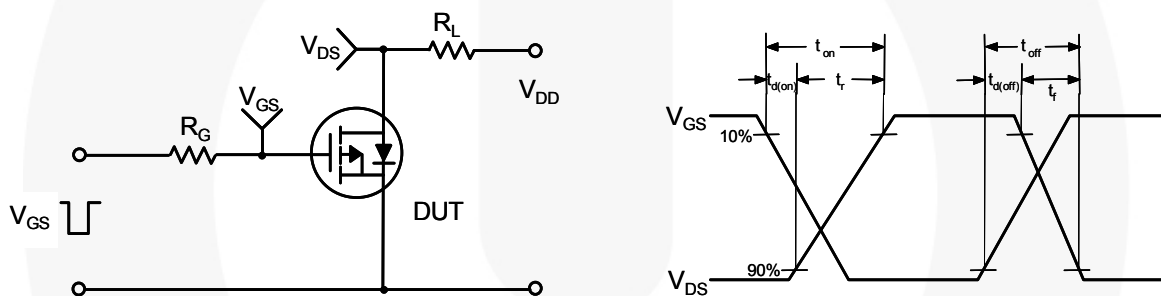


Figure 13. Resistive Switching Test Circuit & Waveforms

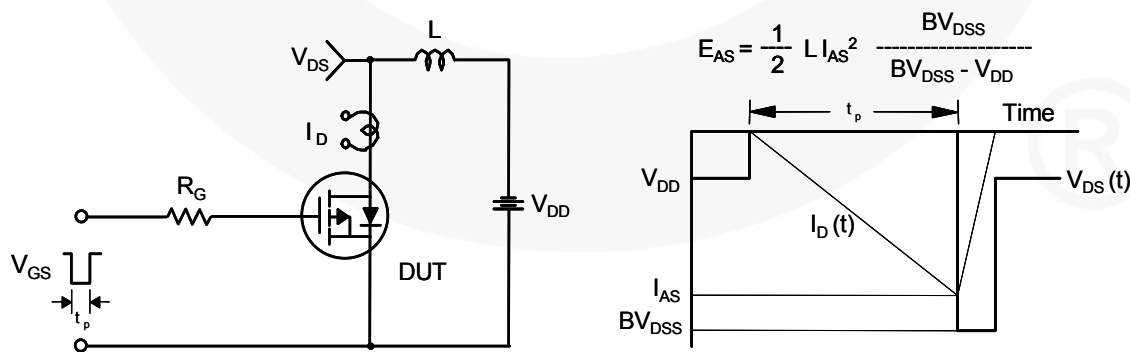


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

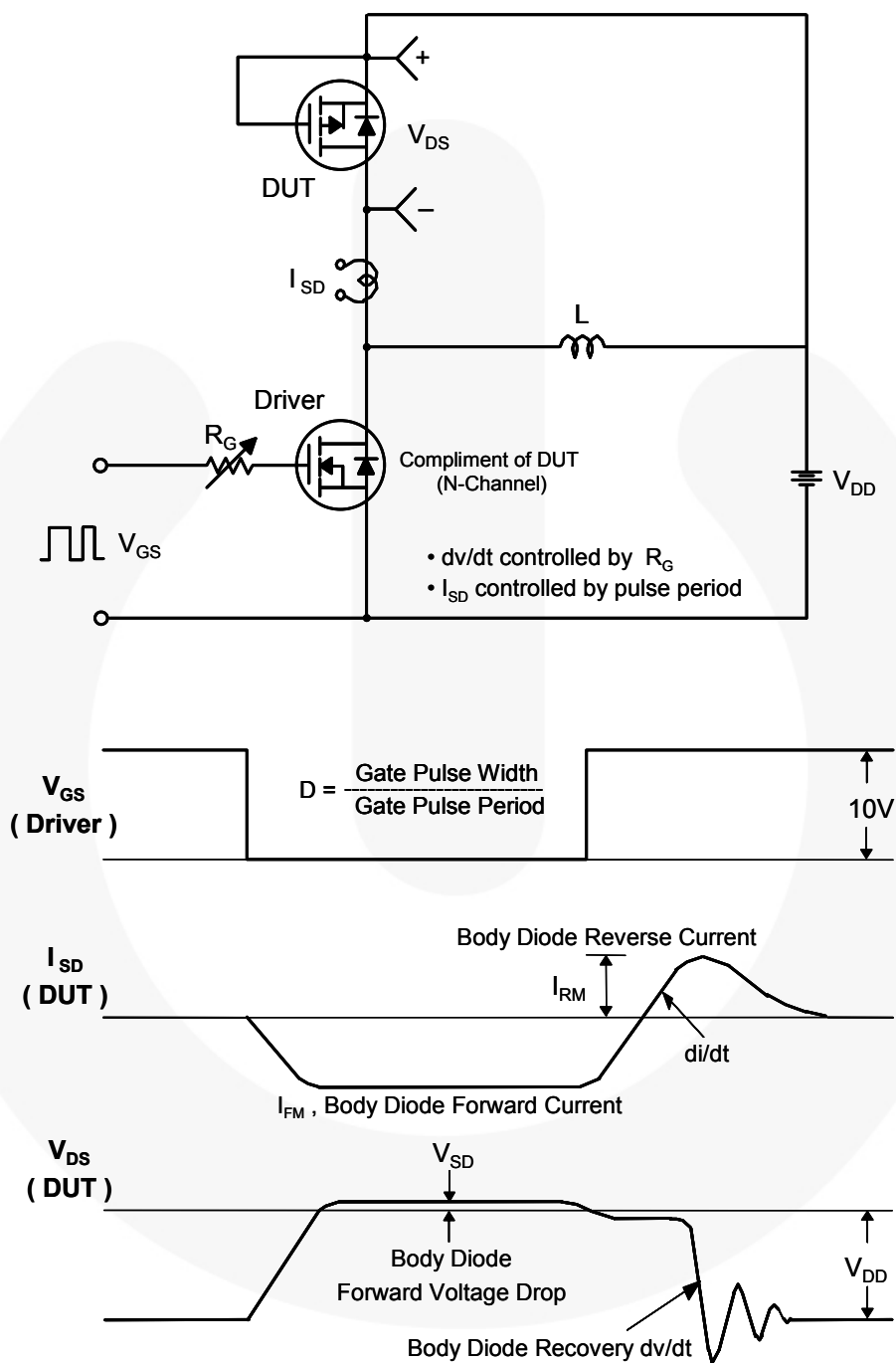
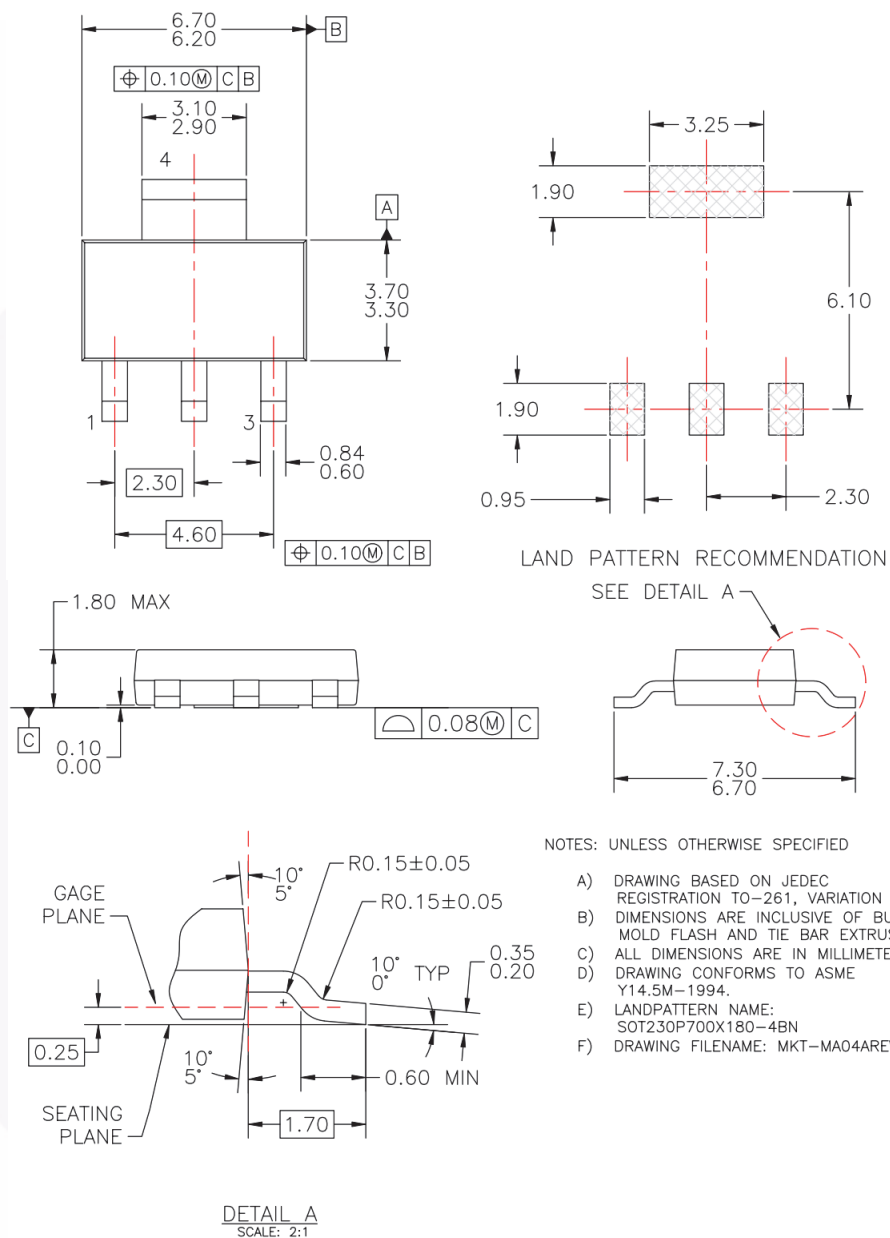


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. SOT-223, Molded, 4-Lead**

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