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August 2000

QFET™

# FQS4900

## Dual N & P-Channel, Logic Level MOSFET

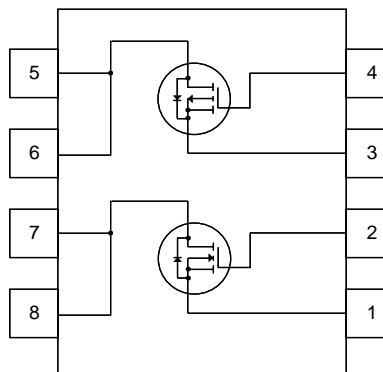
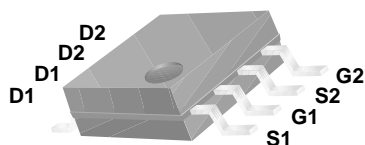
### General Description

These dual N and P-channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. This device is well suited for high interface in telephone sets.

### Features

- N-Channel 1.3A, 60V,  $R_{DS(on)} = 0.55 \Omega @ V_{GS} = 10 V$   
 $R_{DS(on)} = 0.65 \Omega @ V_{GS} = 5 V$   
 P-Channel -0.3A, -300V,  $R_{DS(on)} = 15.5 \Omega @ V_{GS} = -10 V$   
 $R_{DS(on)} = 16 \Omega @ V_{GS} = -5 V$
- Low gate charge ( typical N-Channel 1.6 nC)  
 ( typical P-Channel 3.6 nC)
- Fast switching
- Improved dv/dt capability



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
$V_{DSS}$	Drain-Source Voltage	60	-300	V
$I_D$	Drain Current - Continuous ( $T_A = 25^\circ\text{C}$ )	1.3	-0.3	A
	- Continuous ( $T_A = 70^\circ\text{C}$ )	0.82	-0.19	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	5.2	-1.2	A
$V_{GSS}$	Gate-Source Voltage	$\pm 20$		V
dv/dt	Peak Diode Recovery dv/dt (Note 2)	7.0	4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ )	2.0		W
	( $T_A = 70^\circ\text{C}$ )	1.3		W
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	62.5	$^\circ\text{C/W}$

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	N-Ch	60	--	--	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	P-Ch	-300	--	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 60 V, V <sub>GS</sub> = 0 V	N-Ch	--	--	1	μA
		V <sub>DS</sub> = 48 V, T <sub>C</sub> = 55°C		--	--	10	μA
		V <sub>DS</sub> = -300 V, V <sub>GS</sub> = 0 V	P-Ch	--	--	-1	μA
		V <sub>DS</sub> = -240 V, T <sub>C</sub> = 55°C		--	--	-10	μA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	V <sub>GS</sub> = 20 V, V <sub>DS</sub> = 0 V	All	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	V <sub>GS</sub> = -20 V, V <sub>DS</sub> = 0 V	All	--	--	-100	nA
On Characteristics							
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = 4V, I <sub>D</sub> = 20 mA	N-Ch	1.0	--	1.95	V
		V <sub>DS</sub> = 4V, I <sub>D</sub> = -20 mA	P-Ch	-1.0	--	-1.95	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 0.65 A	N-Ch	--	0.39	0.55	Ω
		V <sub>GS</sub> = 5 V, I <sub>D</sub> = 0.65 A		--	0.46	0.65	Ω
		V <sub>GS</sub> = -10 V, I <sub>D</sub> = -0.15 A	P-CH	--	11.2	15.5	Ω
		V <sub>GS</sub> = -5 V, I <sub>D</sub> = -0.15 A		--	11.4	16	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 0.65 A	N-CH	--	1.7	--	S
		V <sub>DS</sub> = -10 V, I <sub>D</sub> = -0.15 A	P-CH	--	0.6	--	S
Switching Characteristics							
t <sub>d(on)</sub>	Turn-On Delay Time	N-Channel V <sub>DD</sub> = 30 V, I <sub>D</sub> = 1.3 A, R <sub>G</sub> = 25 Ω	N-Ch	--	5.7	21	ns
t <sub>r</sub>	Turn-On Rise Time		P-Ch	--	10	30	ns
			N-Ch	--	21	50	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		P-Ch	--	25	60	ns
		N-Ch	--	11	32	ns	
t <sub>f</sub>	Turn-Off Fall Time	P-Channel V <sub>DD</sub> = -150 V, I <sub>D</sub> = -0.3 A, R <sub>G</sub> = 25 Ω	P-Ch	--	35	80	ns
			N-Ch	--	17	45	ns
Q <sub>g</sub>	Total Gate Charge		P-Ch	--	47	105	ns
			N-Ch	--	1.6	2.1	nC
Q <sub>gs</sub>	Gate-Source Charge	N-Channel V <sub>DS</sub> = 48 V, I <sub>D</sub> = 1.3 A, V <sub>GS</sub> = 5 V	P-Ch	--	3.6	4.7	nC
			N-Ch	--	0.28	--	nC
Q <sub>gd</sub>	Gate-Drain Charge	P-Channel V <sub>DS</sub> = -240 V, I <sub>D</sub> = -0.3 A, V <sub>GS</sub> = -5 V	P-Ch	--	0.42	--	nC
			N-Ch	--	0.82	--	nC
			P-Ch	--	2.1	--	nC
Drain-Source Diode Characteristics and Maximum Ratings							
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		N-Ch	--	--	1.3	A
			P-Ch	--	--	-0.3	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 1.3 A	N-Ch	--	--	1.5	V
		V <sub>GS</sub> = 0 V, I <sub>S</sub> = -0.3 A	P-Ch	--	--	-4.0	V

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
3. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
4. Essentially independent of operating temperature

# Typical Characteristics : N-Channel

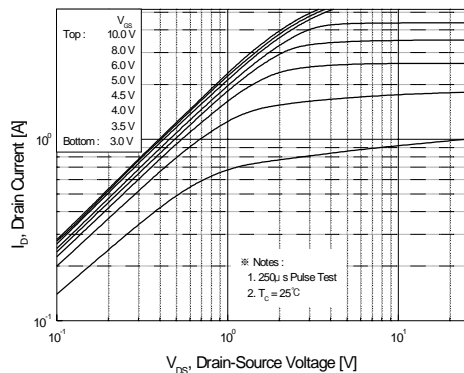


Figure 1. On-Region Characteristics

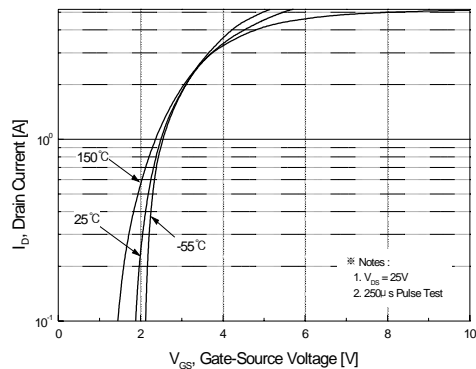


Figure 2. Transfer Characteristics

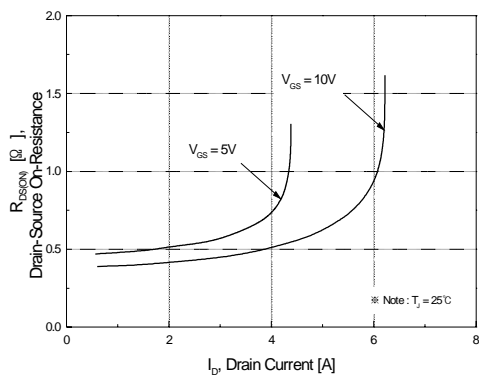


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

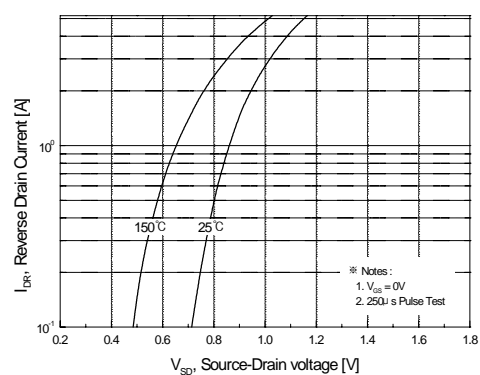


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

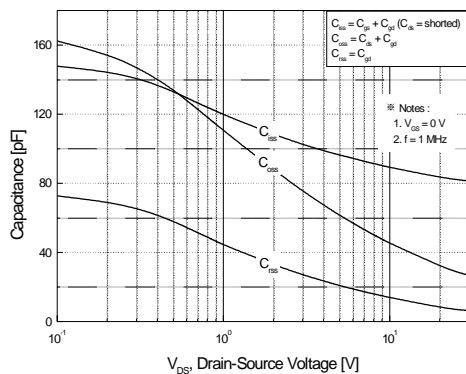


Figure 5. Capacitance Characteristics

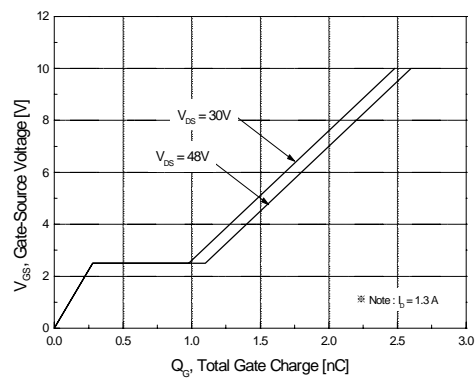


Figure 6. Gate Charge Characteristics

# Typical Characteristics : N-Channel (Continued)

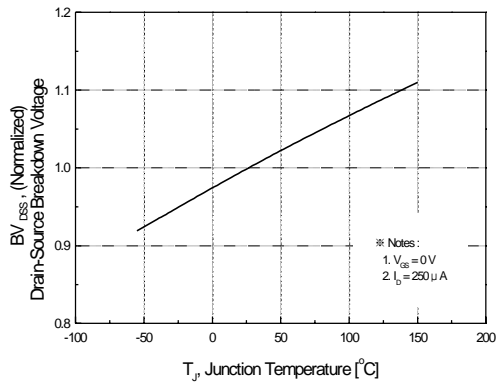


Figure 7. Breakdown Voltage Variation vs. Temperature

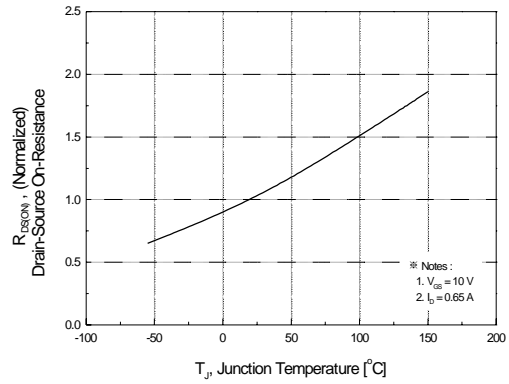


Figure 8. On-Resistance Variation vs. Temperature

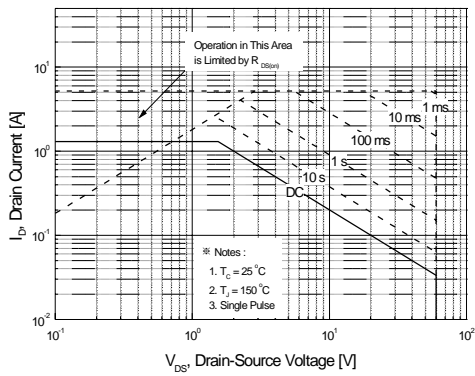


Figure 9. Maximum Safe Operating Area

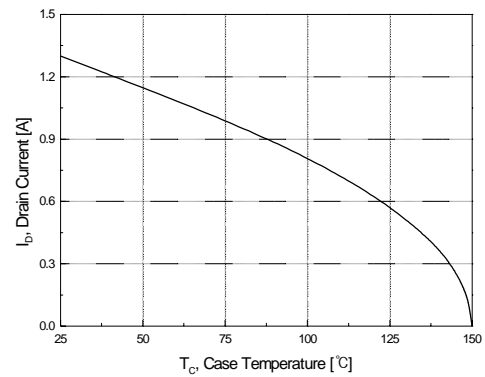


Figure 10. Maximum Drain Current vs. Case Temperature

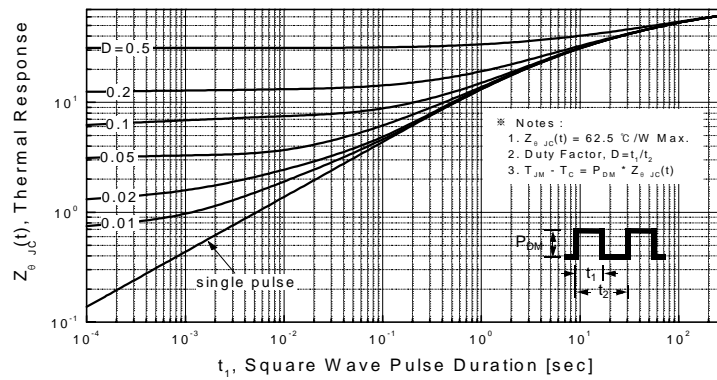


Figure 11. Transient Thermal Response Curve

# Typical Characteristics : P-Channel (Continued)

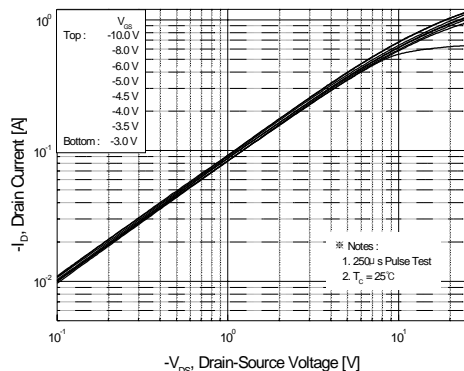


Figure 1. On-Region Characteristics

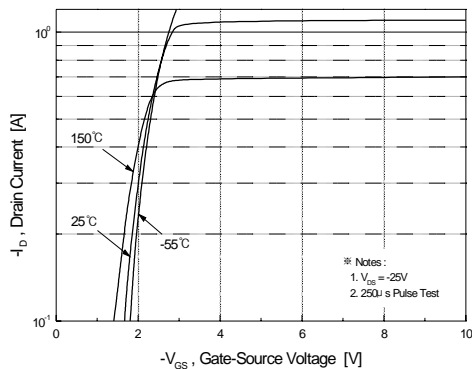


Figure 2. Transfer Characteristics

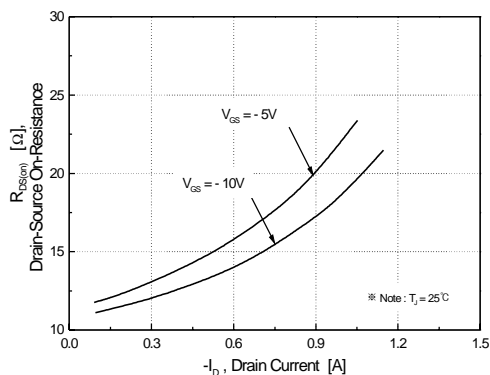


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

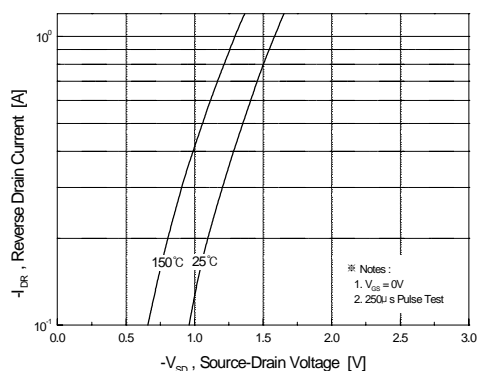


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

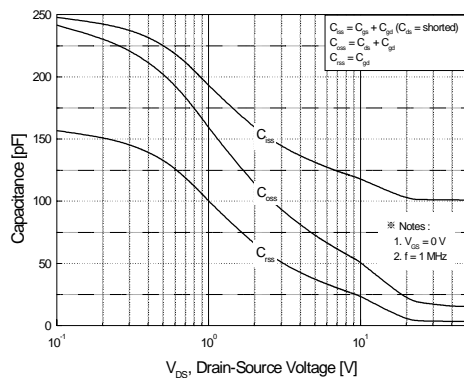


Figure 5. Capacitance Characteristics

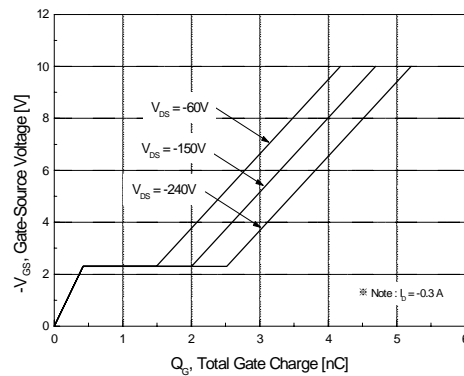


Figure 6. Gate Charge Characteristics

# Typical Characteristics : P-Channel (Continued)

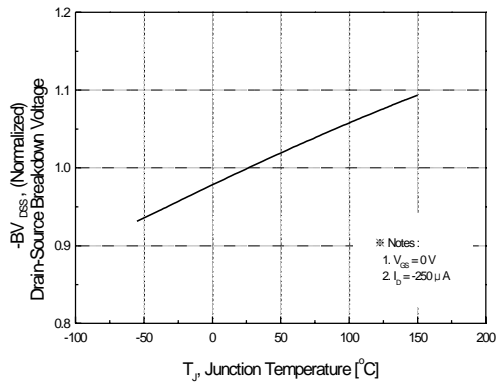


Figure 7. Breakdown Voltage Variation vs. Temperature

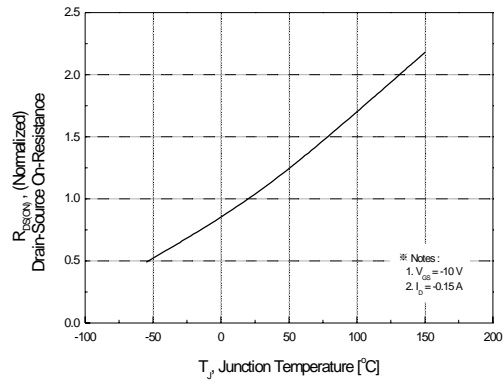


Figure 8. On-Resistance Variation vs. Temperature

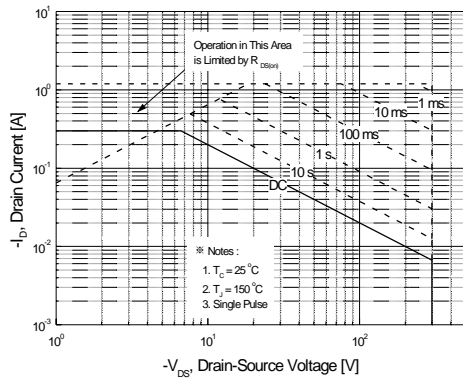


Figure 9. Maximum Safe Operating Area

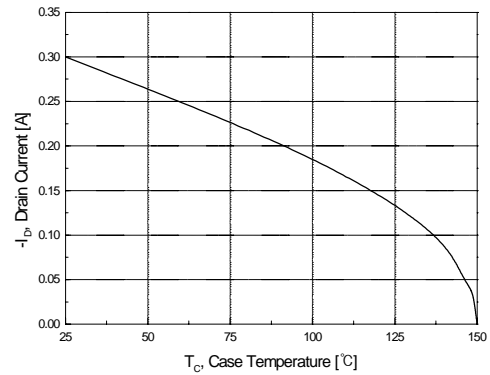


Figure 10. Maximum Drain Current vs. Case Temperature

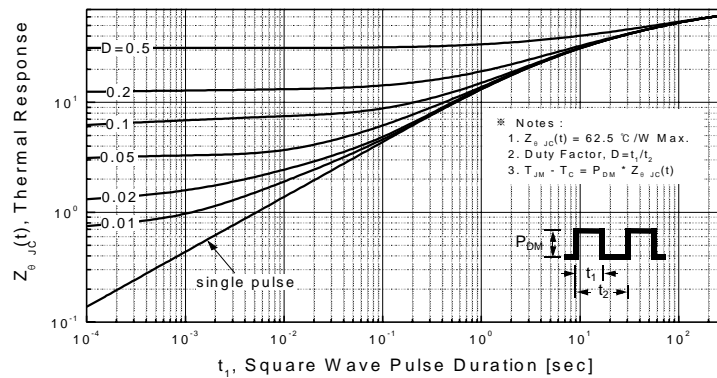
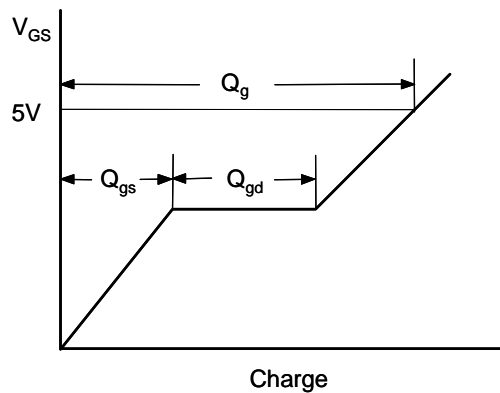
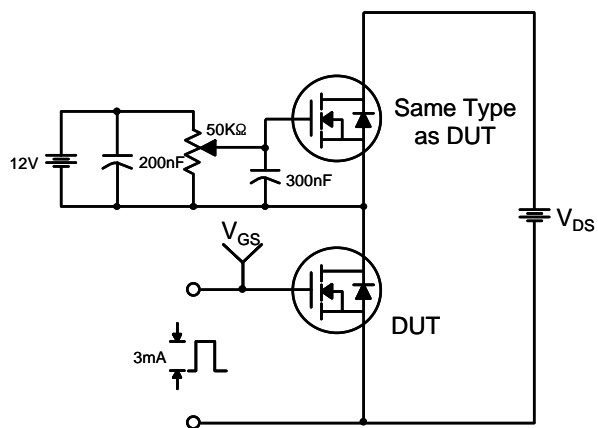
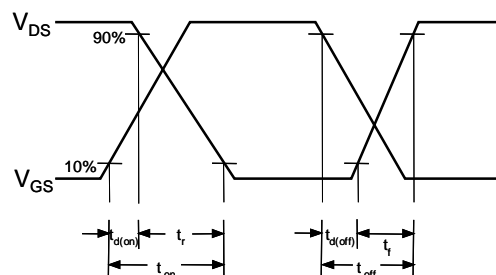
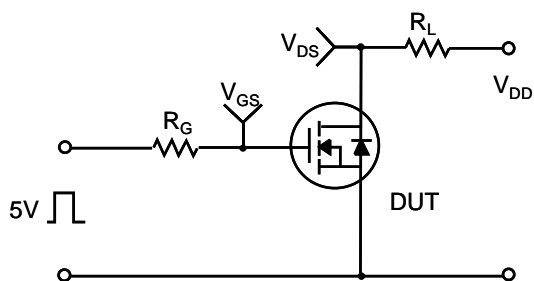


Figure 11. Transient Thermal Response Curve

## Gate Charge Test Circuit &amp; Waveform



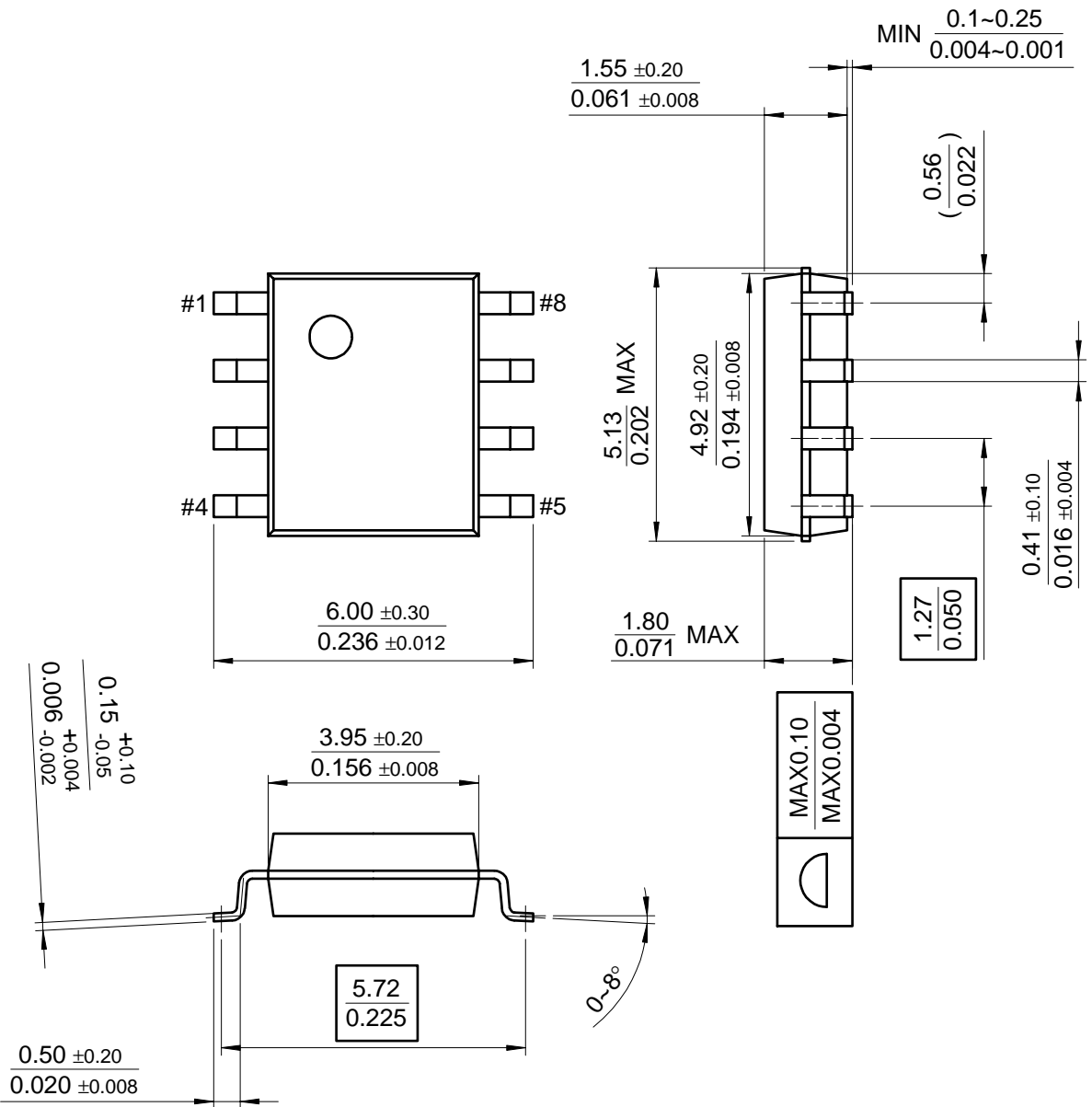
## Resistive Switching Test Circuit &amp; Waveforms





Package Dimensions

8-SOP



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