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ON Semiconductor®

# FQD3P50TM-F085

## 500V P-Channel MOSFET

### General Description

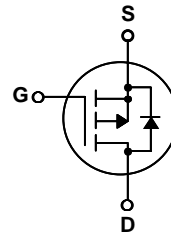
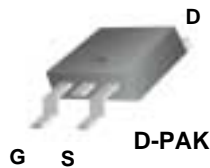
These P-Channel enhancement mode power field effect transistors are produced using ON Semiconductor's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for electronic lamp ballast based on complimentary half bridge.

### Features

- -2.1A, -500V,  $R_{DS(on)} = 4.9\Omega$  @  $V_{GS} = -10$  V
- Low gate charge ( typical 18 nC)
- Low  $C_{rss}$  ( typical 9.5 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Qualified to AEC Q101
- RoHS Compliant



FQD3P50TM-F085 500V P-Channel MOSFET



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQD3P50TM-F085	Units
$V_{DSS}$	Drain-Source Voltage	-500	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	-2.1	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	-1.33	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-8.4	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	250	mJ
$I_{AR}$	Avalanche Current (Note 1)	-2.1	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-4.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	2.5	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	50	W
	- Derate above $25^\circ\text{C}$	0.4	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	$^\circ\text{C/W}$

\* When mounted on the minimum pad size recommended (PCB Mount)

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.42	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -500\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -400\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -1.05\text{ A}$	--	3.9	4.9	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -50\text{ V}, I_D = -1.05\text{ A}$ (Note 4)	--	2.1	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	510	660	pF
$C_{oss}$	Output Capacitance		--	70	90	pF
$C_{rss}$	Reverse Transfer Capacitance		--	9.5	12	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -250\text{ V}, I_D = -2.7\text{ A},$ $R_G = 25\text{ }\Omega$  (Note 4, 5)	--	12	35	ns
$t_r$	Turn-On Rise Time		--	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
$t_f$	Turn-Off Fall Time		--	45	100	ns
$Q_g$	Total Gate Charge	$V_{DS} = -400\text{ V}, I_D = -2.7\text{ A},$ $V_{GS} = -10\text{ V}$  (Note 4, 5)	--	18	23	nC
$Q_{gs}$	Gate-Source Charge		--	3.6	--	nC
$Q_{gd}$	Gate-Drain Charge		--	9.2	--	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	-2.1	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-8.4	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.1 A	--	--	-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -2.7 A, dI <sub>F</sub> / dt = 100 A/μs (Note 4)	--	270	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.5	--	μC

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 102\text{ mH}$ ,  $I_{AS} = -2.1\text{ A}$ ,  $V_{DD} = -50\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq -2.7\text{ A}$ ,  $dI/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

## Typical Characteristics

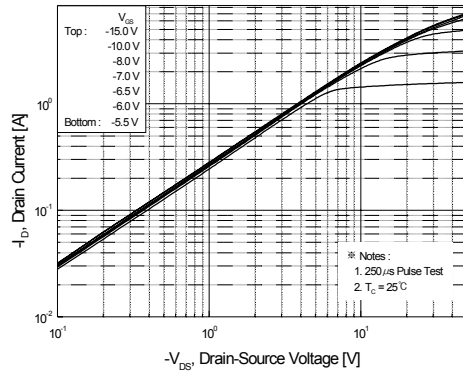


Figure 1. On-Region Characteristics

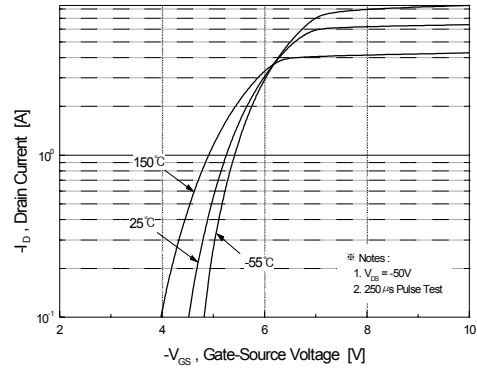


Figure 2. Transfer Characteristics

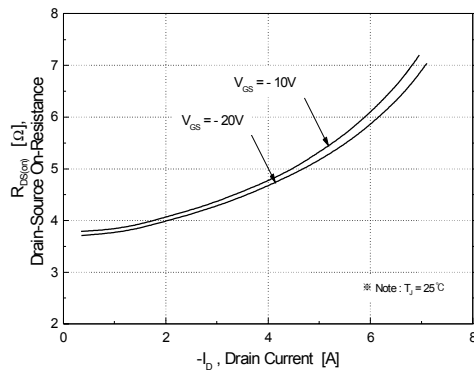


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

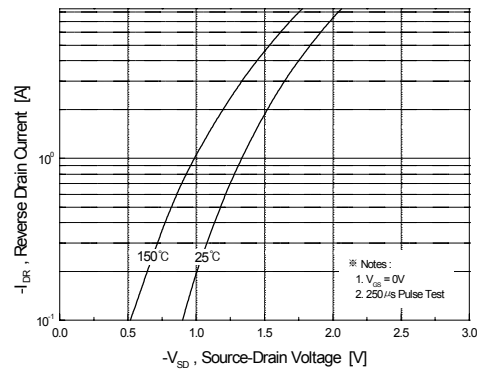


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

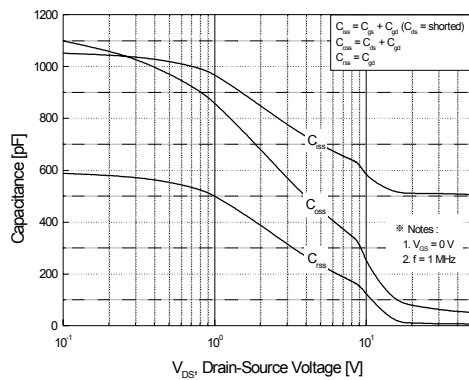


Figure 5. Capacitance Characteristics

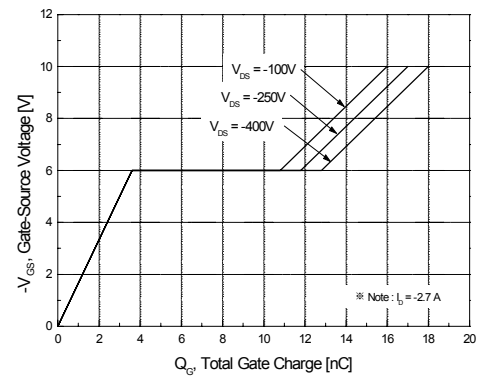
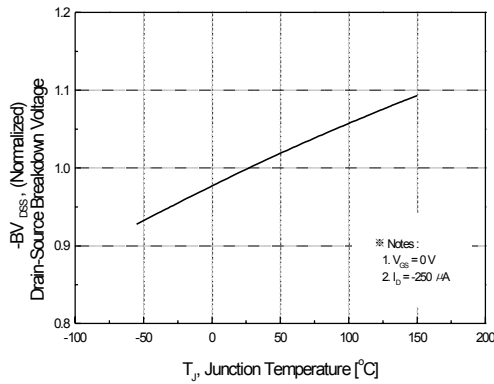
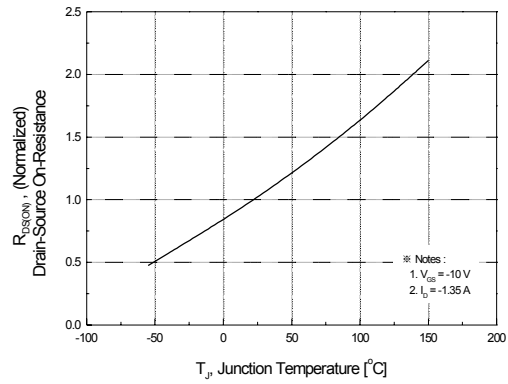


Figure 6. Gate Charge Characteristics

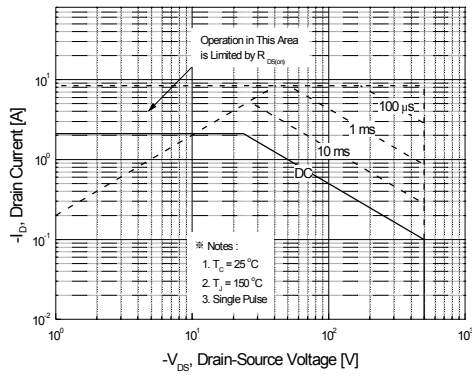
## Typical Characteristics (Continued)



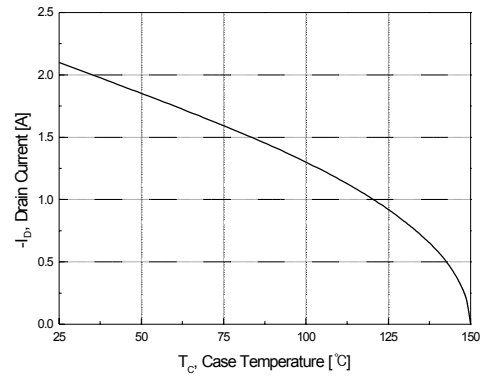
**Figure 7. Breakdown Voltage Variation vs. Temperature**



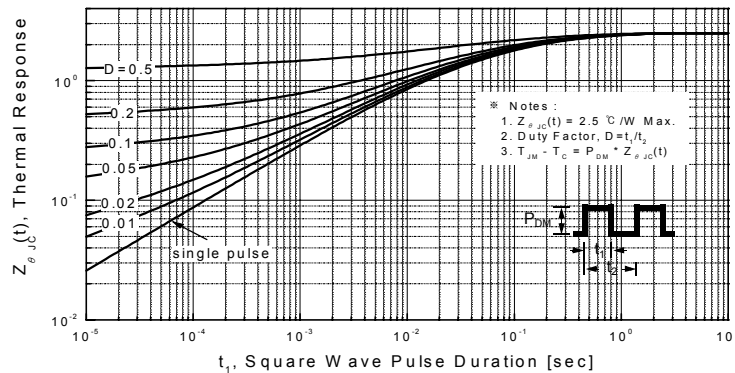
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**

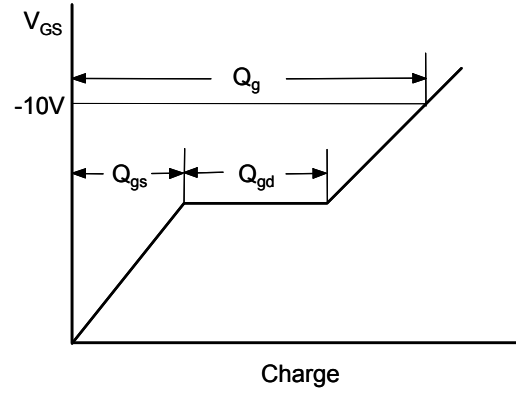
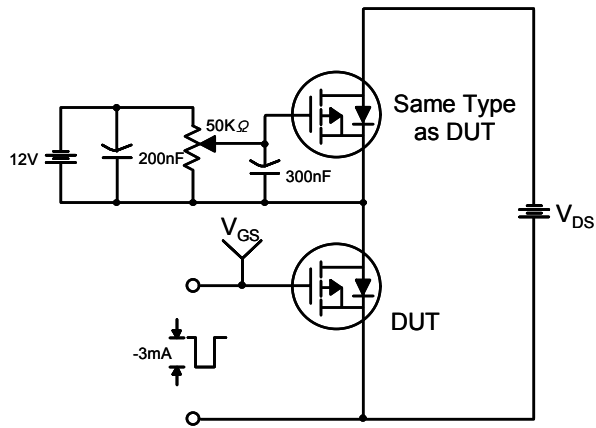


**Figure 10. Maximum Drain Current vs. Case Temperature**

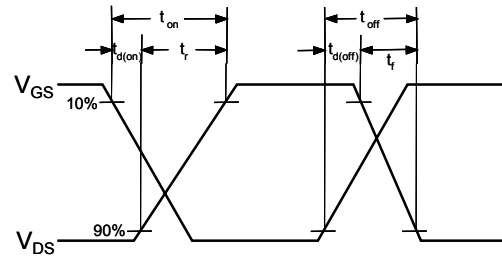
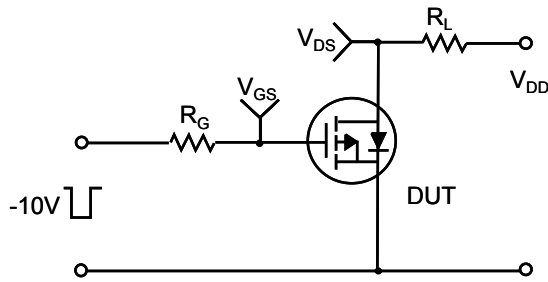


**Figure 11. Transient Thermal Response Curve**

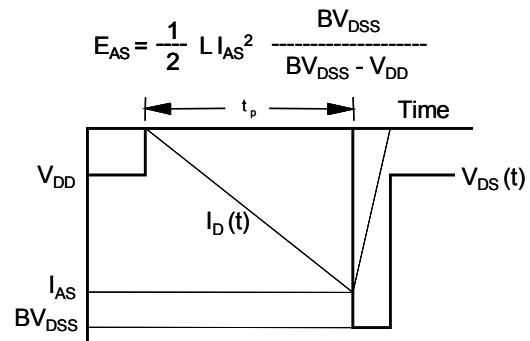
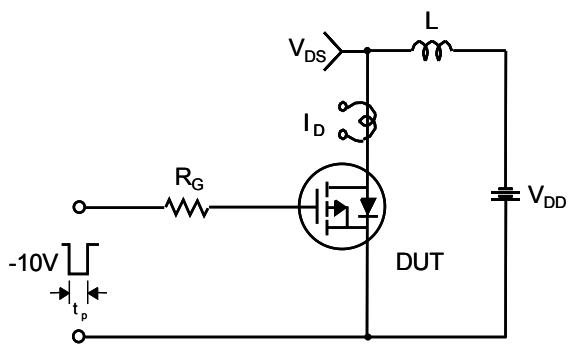
### Gate Charge Test Circuit & Waveform



### Resistive Switching Test Circuit & Waveforms



### Unclamped Inductive Switching Test Circuit & Waveforms



### Peak Diode Recovery dv/dt Test Circuit & Waveforms

The diagram illustrates a test circuit and its corresponding waveforms for measuring the peak diode recovery dv/dt.

**Circuit Diagram:**

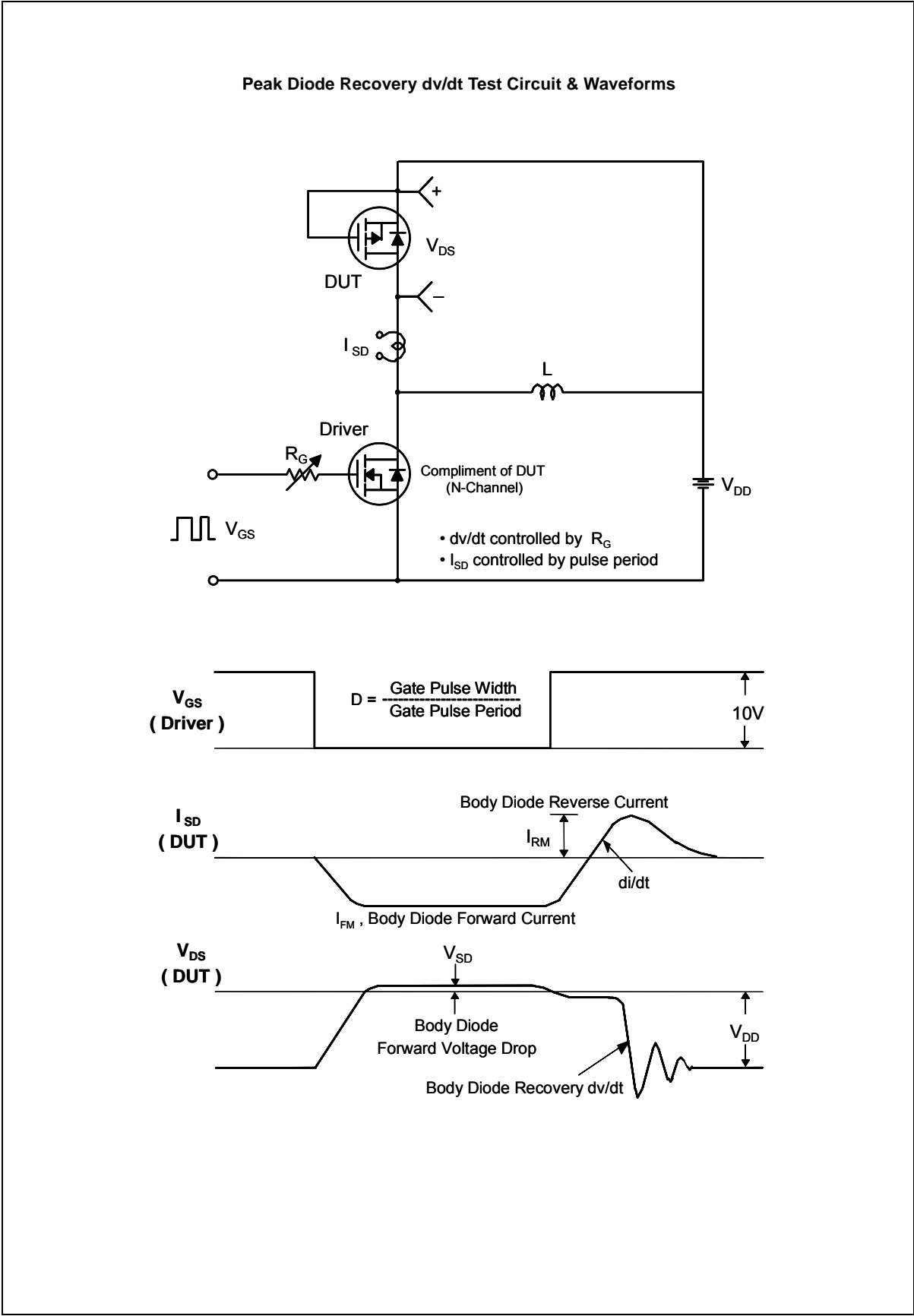
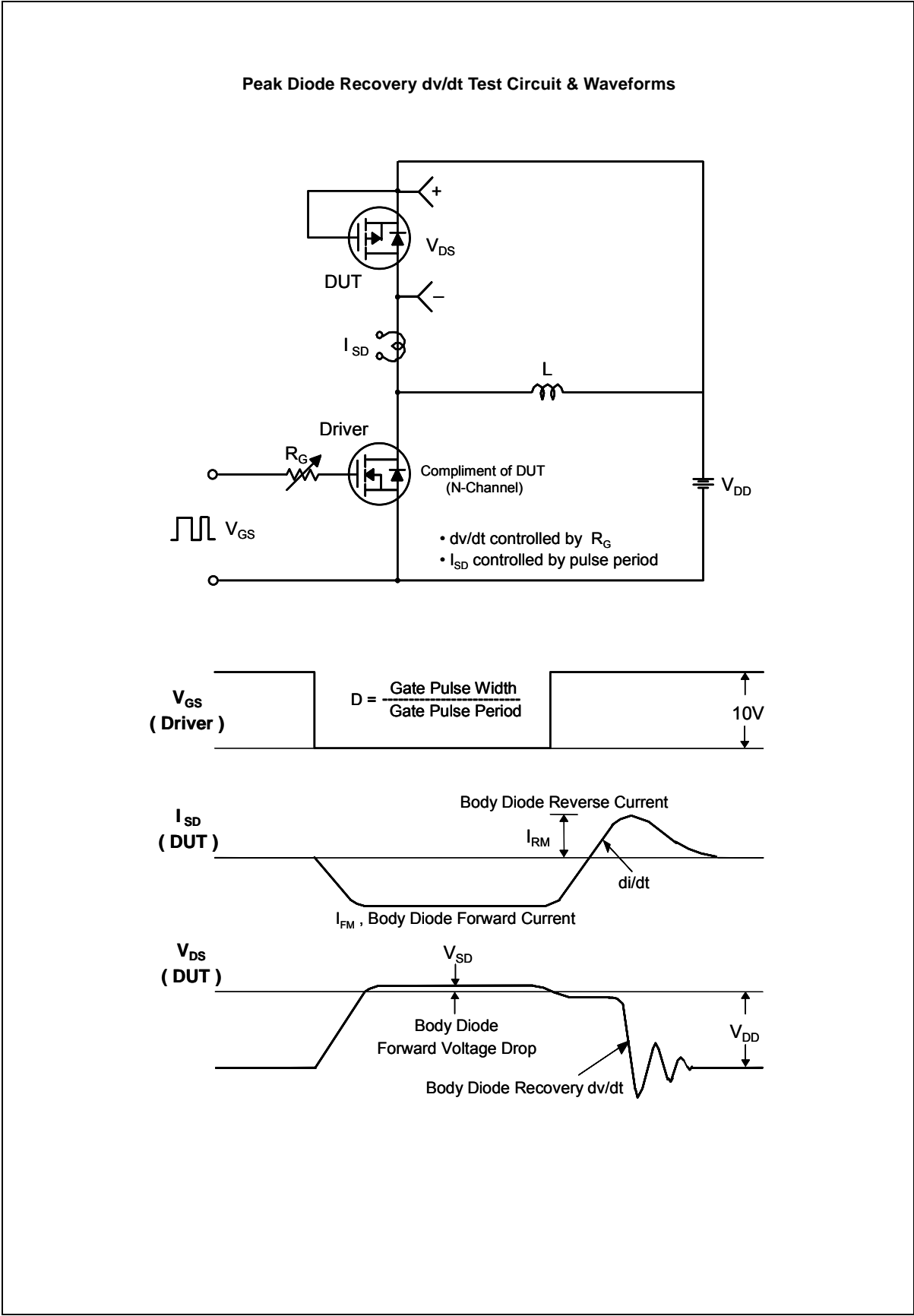
- The circuit features a Driver (N-Channel MOSFET) and a DUT (Diode Under Test).
- The Driver's gate is driven by a square wave  $V_{GS}$  through a gate resistor  $R_G$ .
- The Driver's source is connected to ground, and its drain is connected to the DUT's anode.
- The DUT's cathode is connected to a load inductor  $L$ , which is then connected to a supply voltage  $V_{DD}$ .
- The DUT's reverse current is labeled  $I_{SD}$ .
- The DUT's forward voltage drop is labeled  $V_{DS}$ .
- The DUT's forward current is labeled  $I_{FM}$ .
- The DUT's reverse recovery current is labeled  $I_{RM}$ .
- The DUT's reverse recovery time is labeled  $t_{rr}$ .
- The DUT's reverse recovery charge is labeled  $Q_{rr}$ .
- The DUT's reverse recovery energy is labeled  $E_{rr}$ .

**Waveforms:**

- The  $V_{GS}$  (Driver) waveform is a square wave with a pulse width  $D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$  and a peak voltage of 10V.
- The  $I_{SD}$  (DUT) waveform shows the Body Diode Reverse Current, which is zero during the forward conduction phase and rises during the reverse recovery phase. The peak reverse current is  $I_{RM}$ , and the reverse recovery time is  $t_{rr}$ .
- The  $V_{DS}$  (DUT) waveform shows the Body Diode Forward Voltage Drop, which is zero during the forward conduction phase and rises during the reverse recovery phase. The peak reverse voltage is  $V_{DD}$ , and the reverse recovery time is  $t_{rr}$ .

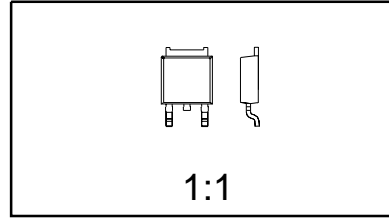
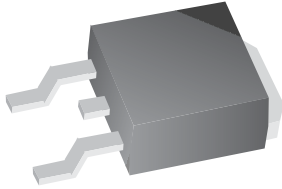
**Key Parameters:**

- $dV/dt$  controlled by  $R_G$
- $I_{SD}$  controlled by pulse period



## Mechanical Dimensions

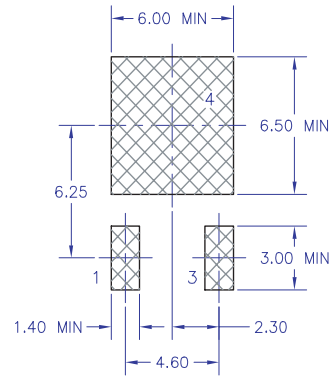
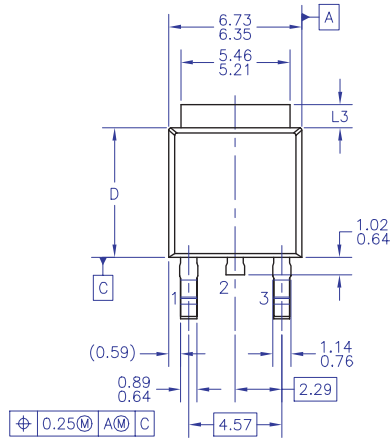
### TO-252 (DPAK) (FS PKG Code 36)



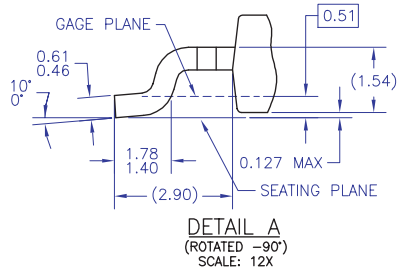
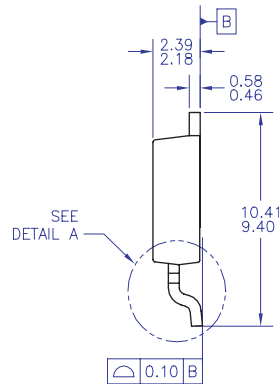
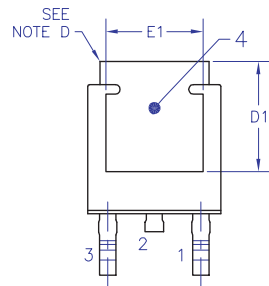
Scale 1:1 on letter size paper

Dimensions shown below are in:  
millimeters

Part Weight per unit (gram): 0.33



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA & AB, DATED NOV. 1999.
- C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
- D) HEAT SINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E) DIMENSIONS L3,D,E1&D1 TABLE:

	OPTION AA	OPTION AB
L3	0.89-1.27	1.52-2.03
D	5.97-6.22	5.33-5.59
E1	4.32 MIN	3.81 MIN
D1	5.21 MIN	4.57 MIN



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