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# FQB9P25

## P-Channel QFET® MOSFET

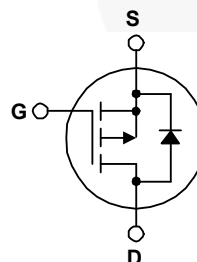
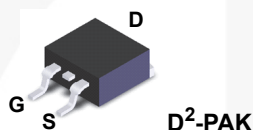
-250 V, -9.4 A, 620 mΩ

### Description

These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for high efficiency switching DC/DC converters.

### Features

- -9.4 A, -250 V,  $R_{DS(on)} = 620 \text{ m}\Omega$  (Max.) @  $V_{GS} = -10 \text{ V}$ ,  $I_D = -4.7 \text{ A}$
- Low Gate Charge (Typ. 29 nC)
- Low  $C_{rss}$  (Typ. 27 pF)
- 100% Avalanche Tested



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FQB9P25TM	Unit
$V_{DSS}$	Drain-Source Voltage	-250	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	-9.4	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	-5.9	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-37.6	A
$V_{GSS}$	Gate-Source Voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	650	mJ
$I_{AR}$	Avalanche Current (Note 1)	-9.4	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	12	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	-5.5	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.13	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	120	W
	- Derate above $25^\circ\text{C}$	0.96	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FQB9P25TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.04	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB9P25TM	FQB9P25	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-250	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\text{ }\mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.2	--	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -250\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -200\text{ V}, T_C = 125^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -4.7\text{ A}$	--	0.48	0.62	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -4.7\text{ A}$	--	5.7	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	910	1180	pF
$C_{oss}$	Output Capacitance		--	170	220	pF
$C_{rss}$	Reverse Transfer Capacitance		--	27	35	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -125\text{ V}, I_D = -9.4\text{ A},$ $R_G = 25\text{ }\Omega$	--	20	50	ns
$t_r$	Turn-On Rise Time		--	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		--	45	100	ns
$t_f$	Turn-Off Fall Time	(Note 4)	--	65	140	ns
$Q_g$	Total Gate Charge	$V_{DS} = -200\text{ V}, I_D = -9.4\text{ A},$ $V_{GS} = -10\text{ V}$	--	29	38	nC
$Q_{gs}$	Gate-Source Charge		--	7.6	--	nC
$Q_{gd}$	Gate-Drain Charge	(Note 4)	--	14	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current	--	--	-9.4	A	
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-37.6	A	
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -9.4 A	--	--	-5.0	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = -9.4 A, dI <sub>F</sub> / dt = 100 A/μs	--	190	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	1.45	--	μC

#### Notes:

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $L = 11.8\text{ mH}$ ,  $I_{AS} = -9.4\text{ A}$ ,  $V_{DD} = -50\text{ V}$ ,  $R_G = 25\text{ }\Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -9.4\text{ A}$ ,  $dI/dt \leq 300\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.

## Typical Characteristics

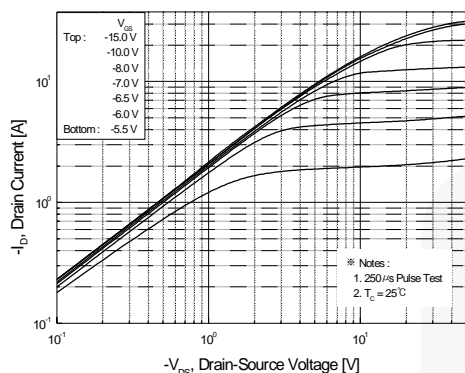


Figure 1. On-Region Characteristics

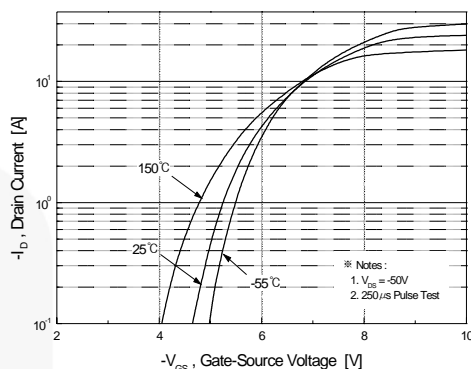


Figure 2. Transfer Characteristics

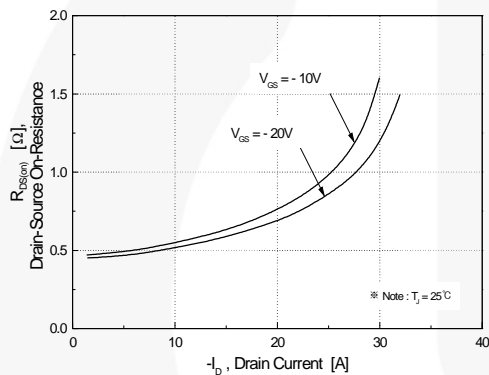


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

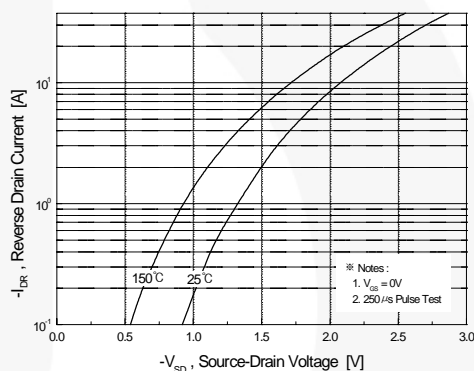


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

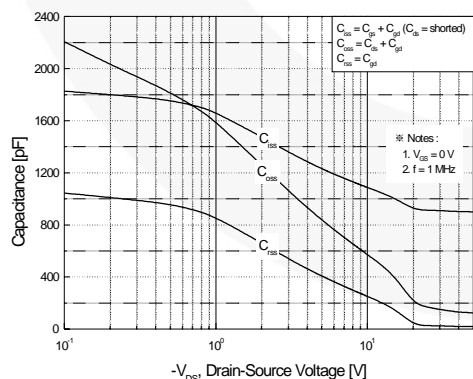


Figure 5. Capacitance Characteristics

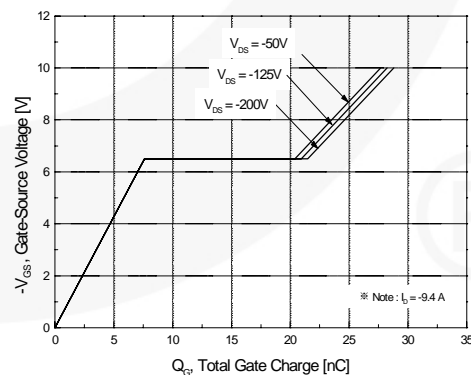
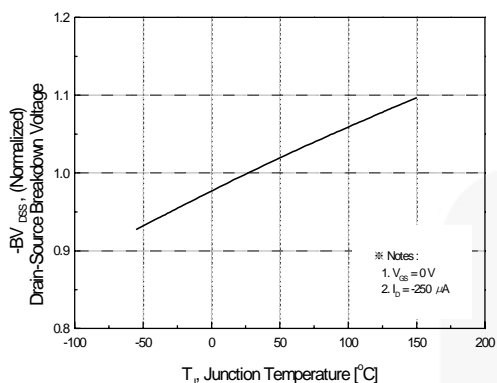
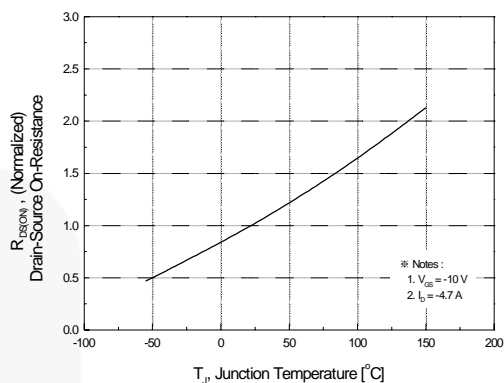


Figure 6. Gate Charge Characteristics

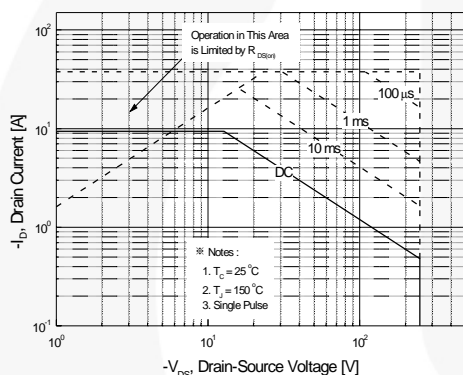
## Typical Characteristics (Continued)



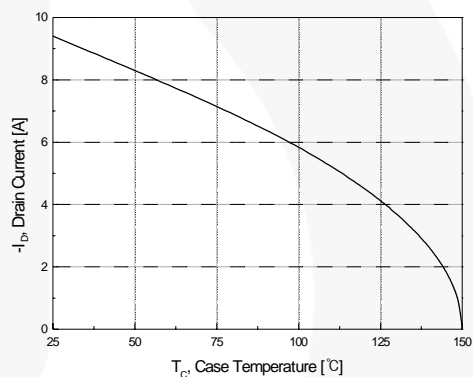
**Figure 7. Breakdown Voltage Variation vs. Temperature**



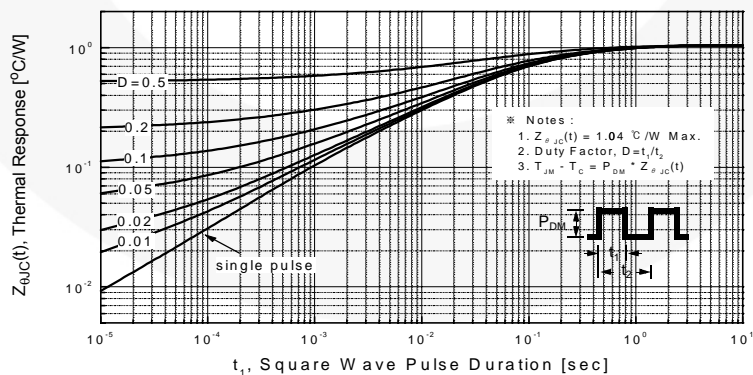
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

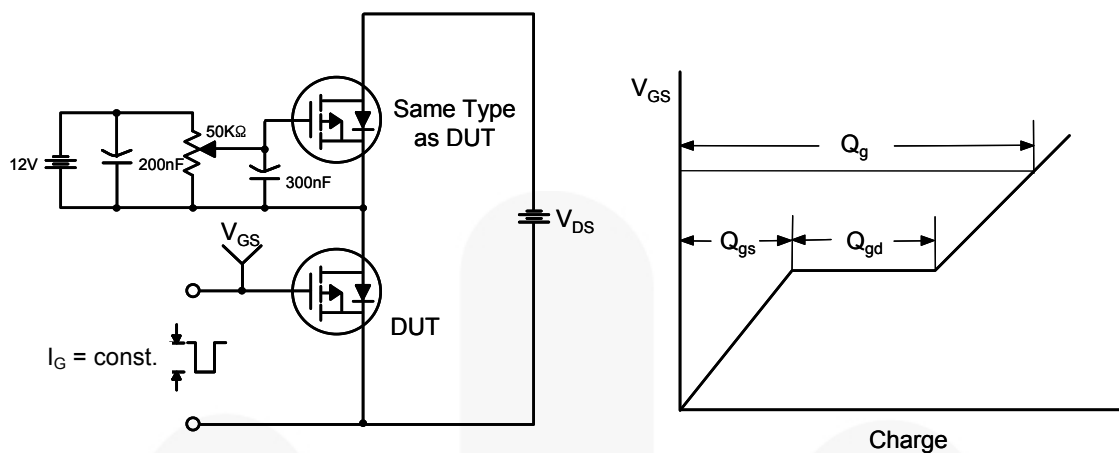


Figure 12. Gate Charge Test Circuit & Waveform

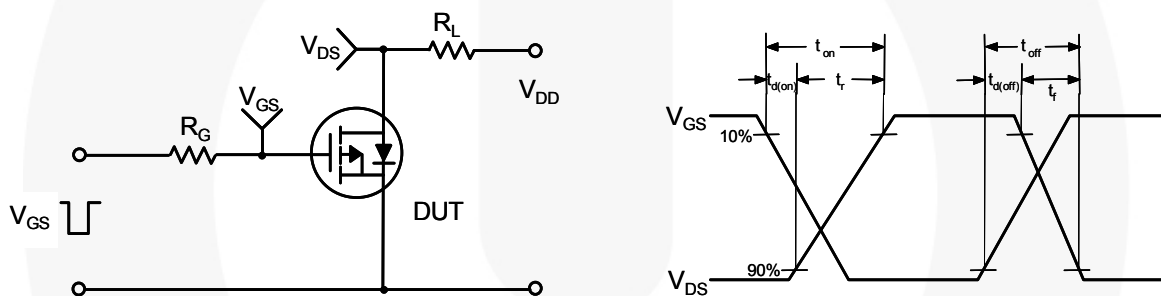


Figure 13. Resistive Switching Test Circuit & Waveforms

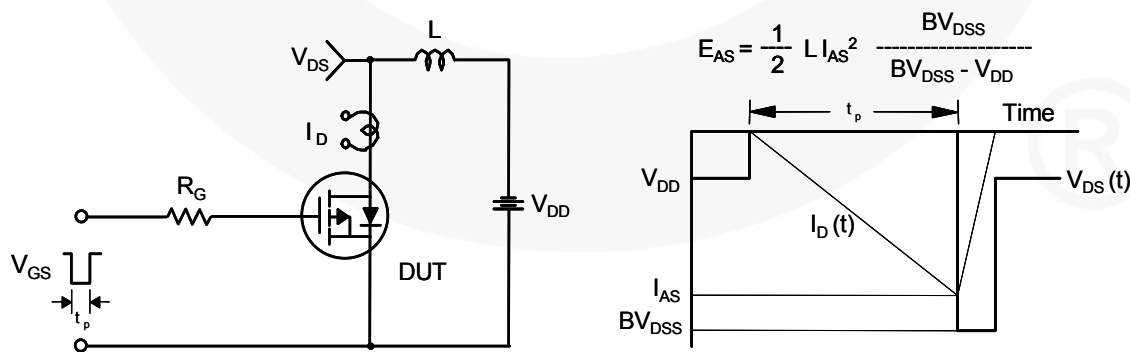


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

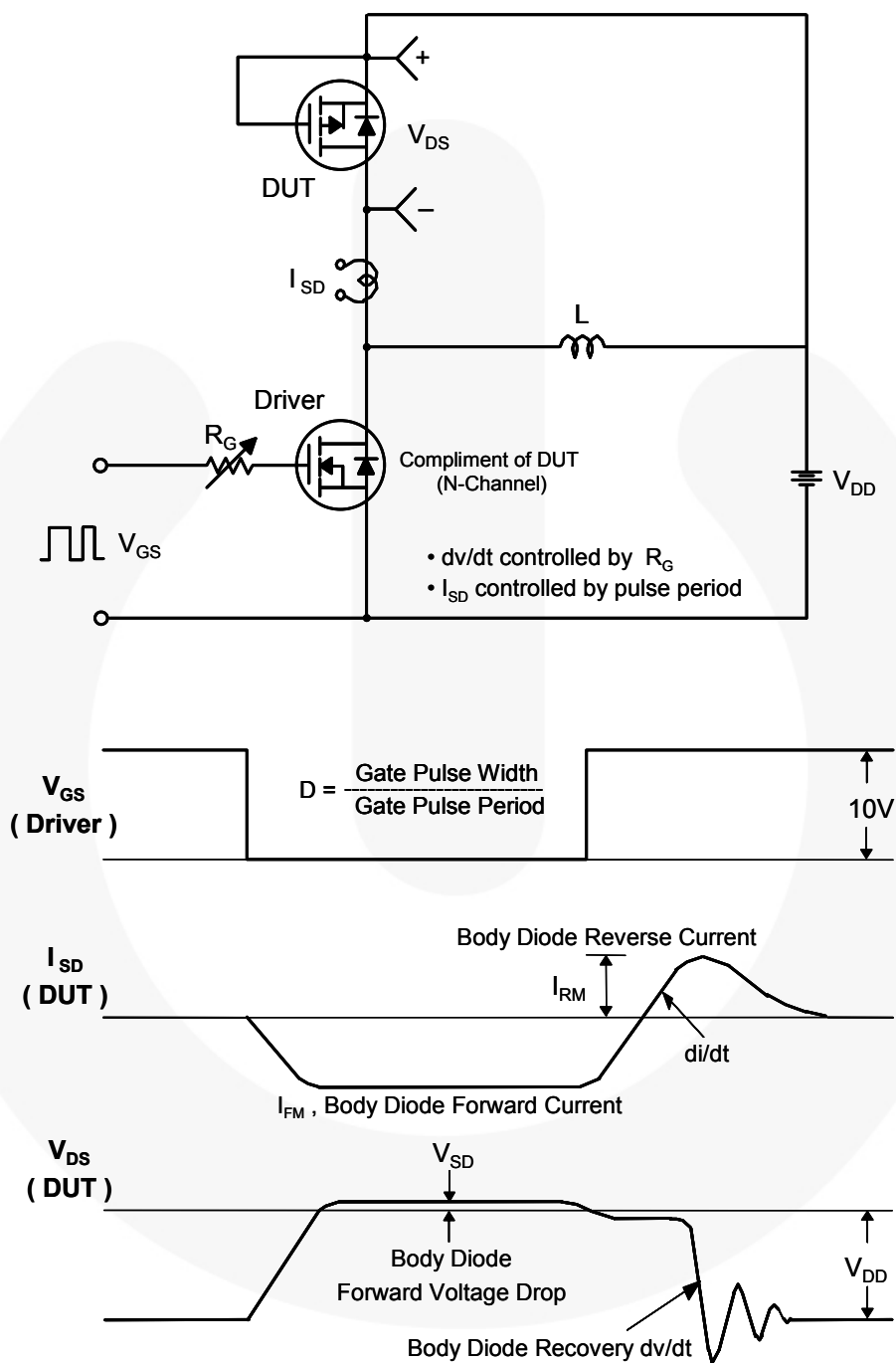
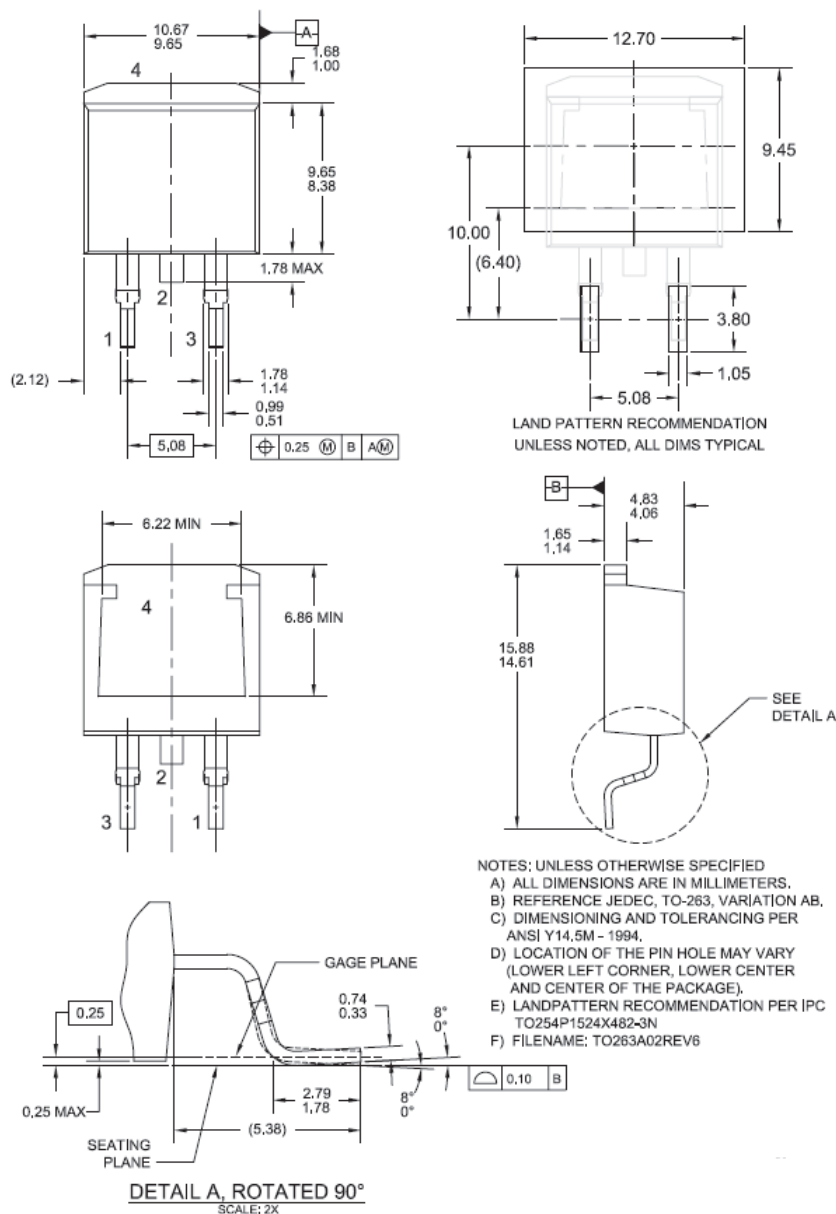


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms

## Mechanical Dimensions



**Figure 16. TO263 (D<sup>2</sup>PAK), Molded, 2-Lead, Surface Mount**

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