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December 2013

FQB8N90C

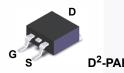
N-Channel QFET[®] MOSFET 900 V, 6.3 A, 1.9 Ω

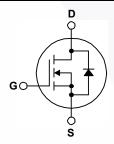
Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Features

- 6.3 A, 900 V, $R_{DS(on)}$ = 1.9 Ω (Max.) @ V_{GS} = 10 V
- Low Gate Charge (Typ. 35 nC)
- Low C_{rss} (Typ. 12 pF)
- · Fast Switching
- · 100% Avalanche Tested
- · Improved dv/dt Capability





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter	FQB8N90CTM	Unit
V _{DSS}	Drain-Source Voltage	900	V
I _D	Drain Current - Continuous (T _C = 25°C)	6.3	Α
	- Continuous (T _C = 100°C)	3.8	Α
I _{DM}	Drain Current - Pulsed (Note 1)	25	Α
V_{GSS}	Gate-Source Voltage	± 30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	850	mJ
I _{AR}	Avalanche Current (Note 1)	6.3	Α
E _{AR}	Repetitive Avalanche Energy (Note 1)	17.1	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_{D}	Power Dissipation (T _C = 25°C)	171	W
	- Derate Above 25°C	1.37	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
TL	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	°C

Thermal Characteristics

Symbol	Parameter	FQB8N90CTM	Unit	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.73	°C/W	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. 40		C/VV	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB8N90CTM	FQB8N90C	D ² -PAK	Tape and Reel	330 mm	24 mm	800 untis

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Uni
Off Cha	racteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA				V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.95		V/°C
I _{DSS}	Zana Cata Valta da Dunin Cumant	V _{DS} = 900 V, V _{GS} = 0 V			10	μА
Z	Zero Gate Voltage Drain Current	V _{DS} = 720 V, T _C = 125°C			100	μА
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V		-	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V		-	-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	3.0		5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 3.15 A		1.6	1.9	Ω
g _{FS}	Forward Transconductance	V _{DS} = 50 V, I _D = 3.15 A		5.5		S
Dvnami	ic Characteristics				•	
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V,		1600	2080	pF
C _{oss}	Output Capacitance	f = 1.0 MHz		130	170	pF
C _{rss}	Reverse Transfer Capacitance			12	15	pF
Cwitchi	ing Characteristics					
	ng Characteristics Turn-On Delay Time			40	90	ns
t _{d(on)}	Turn-On Rise Time	$V_{DD} = 450 \text{ V}, I_D = 8 \text{ A},$		110	230	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_G = 25 Ω		70	150	ns
t _f	Turn-Off Fall Time	(Note 4)		70	150	ns
Q _g	Total Gate Charge	V _{DS} = 720 V, I _D = 8 A, V _{GS} = 10 V		35	45	nC
Q _{gs}	Gate-Source Charge			10		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		14		nC
					•	1
Drain-S	Source Diode Characteristics and Ma Maximum Continuous Drain-Source Diode For				6.3	Α
I _{SM}	Maximum Pulsed Drain-Source Diode Forward				25	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 6.3 A			1.4	V
t _{rr}	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_S = 8 \text{ A},$		530		ns

Notes:

^{1.} Repetitive rating : pulse-width limited by maximum junction temperature.

^{2.} L = 40 mH, I $_{AS}$ = 6.3 A, V $_{DD}$ = 50 V, R $_{G}$ = 25 Ω , starting T $_{J}$ = 25°C.

^{3.} $I_{SD} \le 8$ A, di/dt ≤ 200 A/ μ s, $V_{DD} \le BV_{DSS}$, starting $T_J = 25^{\circ}C$.

^{4.} Essentially independent of operating temperature.

Typical Characteristics

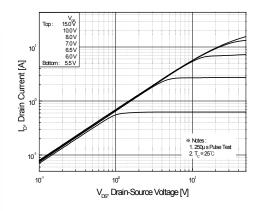


Figure 1. On-Region Characteristics

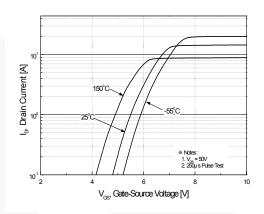


Figure 2. Transfer Characteristics

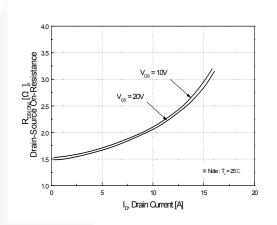


Figure 3. On-Resistance Variation vs
Drain Current and Gate Voltage

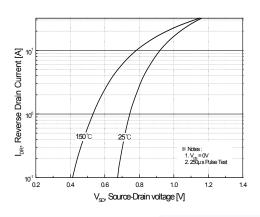


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

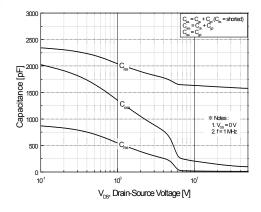


Figure 5. Capacitance Characteristics

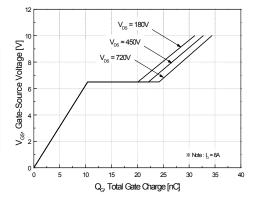


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

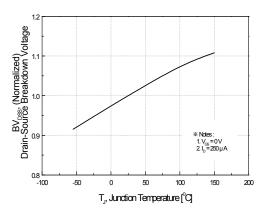


Figure 7. Breakdown Voltage Variation vs Temperature

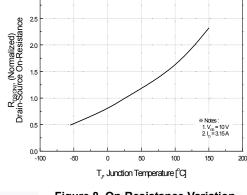


Figure 8. On-Resistance Variation vs Temperature

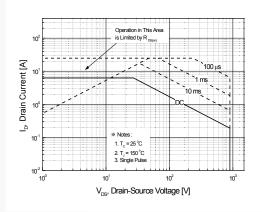


Figure 9. Maximum Safe Operating Area

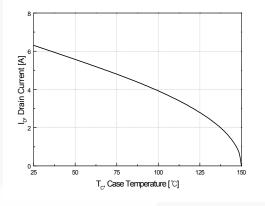


Figure 10. Maximum Drain Current vs Case Temperature

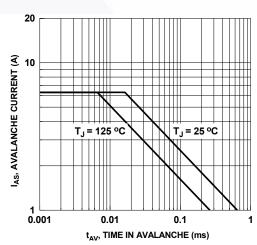


Figure 11. Unclamped Inductive Switching Capability

Typical Characteristics (Continued)

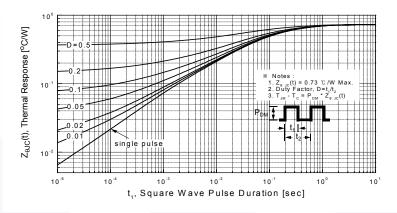


Figure 12. Transient Thermal Response Curve

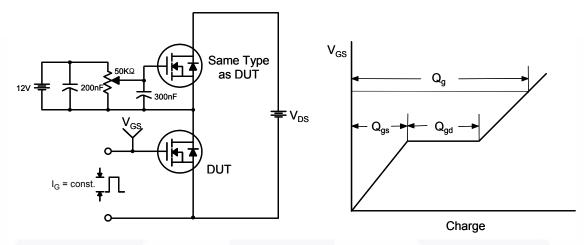


Figure 13. Gate Charge Test Circuit & Waveform

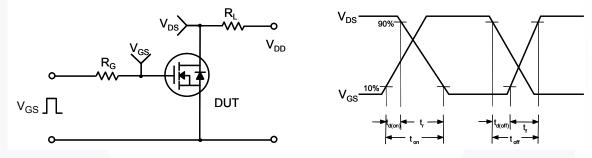


Figure 14. Resistive Switching Test Circuit & Waveforms

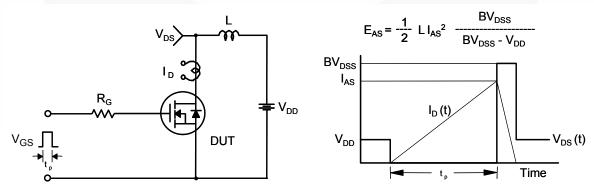


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

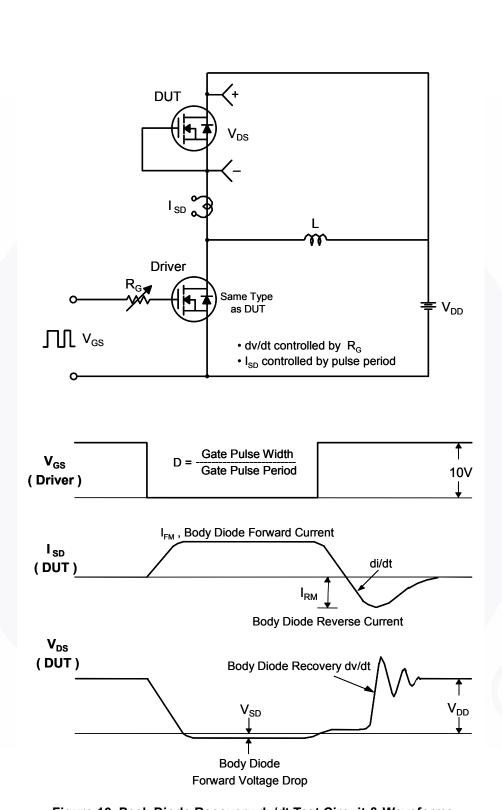


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

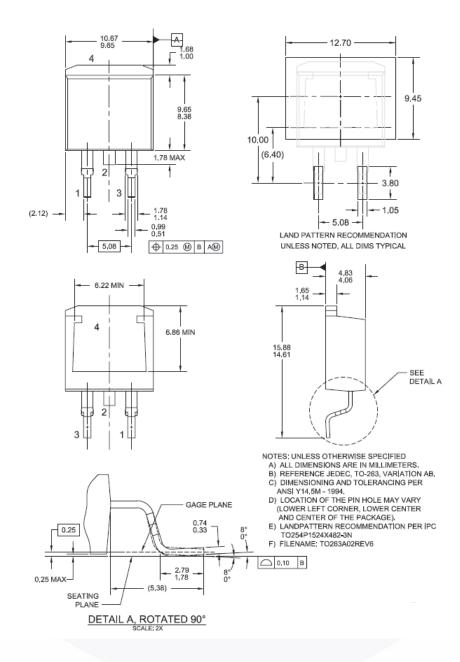


Figure 17. TO263 (D²PAK), Molded, 2-Lead, Surface Mount

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