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FQB33N10L

N-Channel QFET® MOSFET

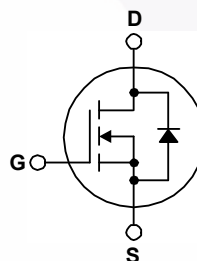
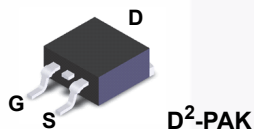
100 V, 33 A, 52 mΩ

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 33 A, 100 V, $R_{DS(on)} = 52 \text{ m}\Omega$ (Max) @ $V_{GS} = 10 \text{ V}$, $I_D = 16.5 \text{ A}$
- Low Gate Charge (Typ. 30 nC)
- Low C_{rss} (Typ. 70 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQB33N10LTM	Unit
V_{DSS}	Drain-Source Voltage	100	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	33	A
	- Continuous ($T_C = 100^\circ\text{C}$)	23	A
I_{DM}	Drain Current - Pulsed (Note 1)	132	A
V_{GSS}	Gate-Source Voltage	± 20	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	430	mJ
I_{AR}	Avalanche Current (Note 1)	33	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	12.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P_D	Power Dissipation ($T_A = 25^\circ\text{C}$) *	3.75	W
	Power Dissipation ($T_C = 25^\circ\text{C}$)	127	W
	- Derate above 25°C	0.85	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	FQB33N10LTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	1.18	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (minimum pad of 2 oz copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (* 1 in ² pad of 2 oz copper), Max.	40	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FQB33N10L	FQB33N10LTM	D2-PAK	330mm	24mm	800

Electrical Characteristics

$T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	--	0.09	--	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 80\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0	--	2.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 16.5\text{ A}$	--	0.039	0.052	Ω
		$V_{GS} = 5\text{ V}, I_D = 16.5\text{ A}$	--	0.043	0.055	
g_{FS}	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 16.5\text{ A}$	--	27	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1250	1630	pF
C_{oss}	Output Capacitance		--	305	400	pF
C_{rss}	Reverse Transfer Capacitance		--	70	90	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}, I_D = 33\text{ A},$ $R_G = 25\ \Omega$	--	17	45	ns
t_r	Turn-On Rise Time		--	470	950	ns
$t_{d(off)}$	Turn-Off Delay Time		--	70	150	ns
t_f	Turn-Off Fall Time		(Note 4)	--	120	250
Q_g	Total Gate Charge	$V_{DS} = 80\text{ V}, I_D = 33\text{ A},$ $V_{GS} = 5\text{ V}$	--	30	40	nC
Q_{gs}	Gate-Source Charge		--	4.7	--	nC
Q_{gd}	Gate-Drain Charge		(Note 4)	--	16	--

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current	--	--	33	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	132	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 33\text{ A}$	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 33\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	90	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.26	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 0.59\text{ mH}, I_{AS} = 33\text{ A}, V_{DD} = 25\text{ V}, R_G = 25\ \Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 33\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially independent of operating temperature

Typical Characteristics

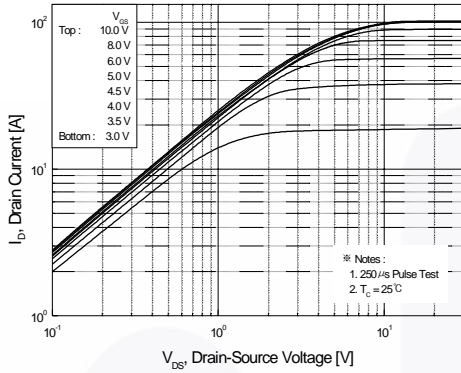


Figure 1. On-Region Characteristics

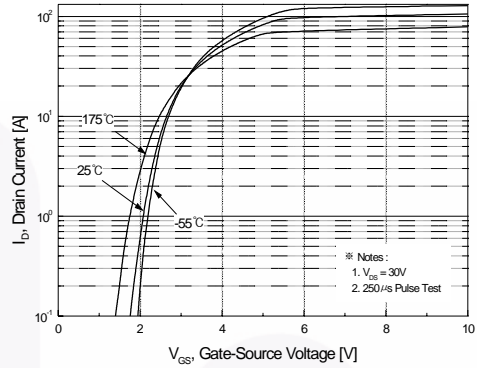


Figure 2. Transfer Characteristics

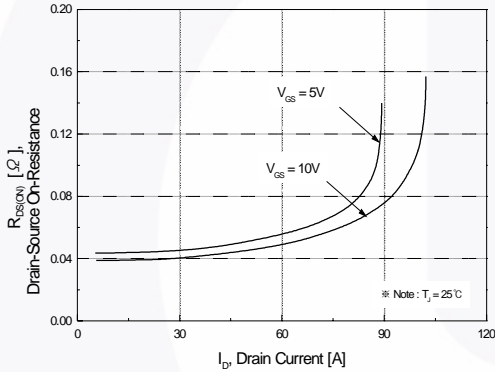


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

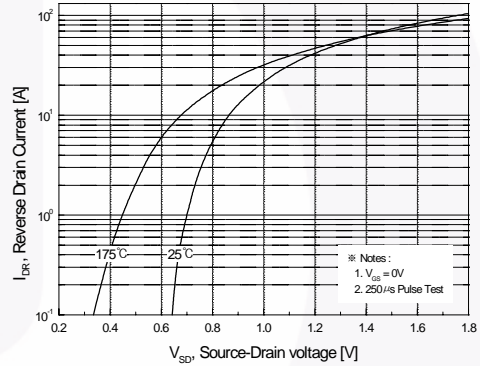


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

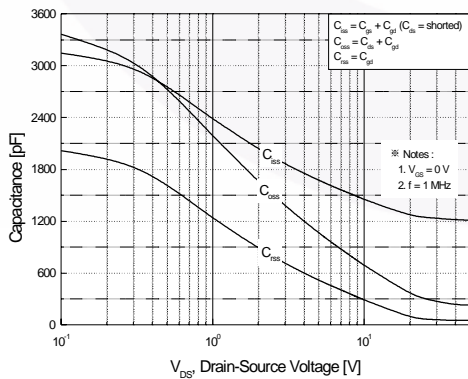


Figure 5. Capacitance Characteristics

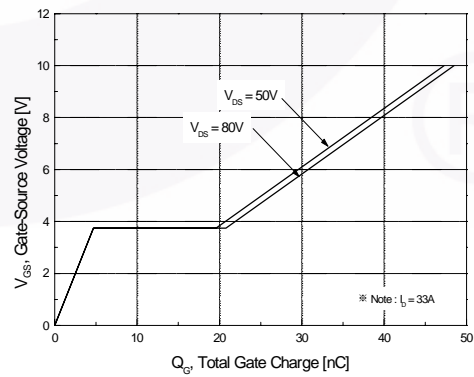


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

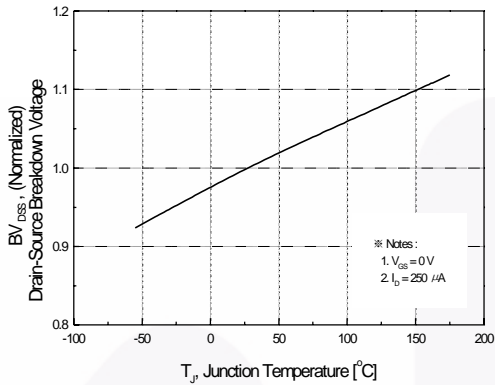


Figure 7. Breakdown Voltage Variation vs. Temperature

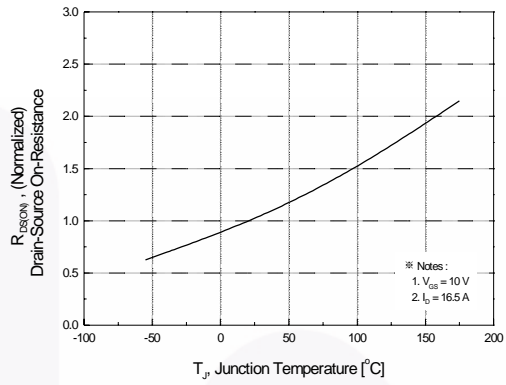


Figure 8. On-Resistance Variation vs. Temperature

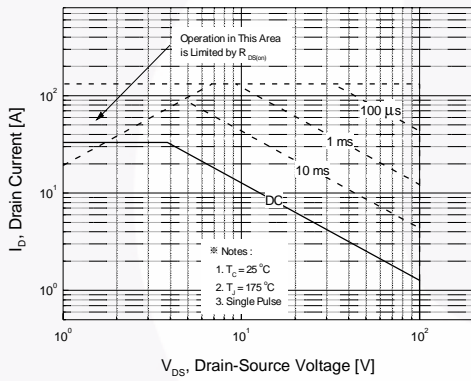


Figure 9. Maximum Safe Operating Area

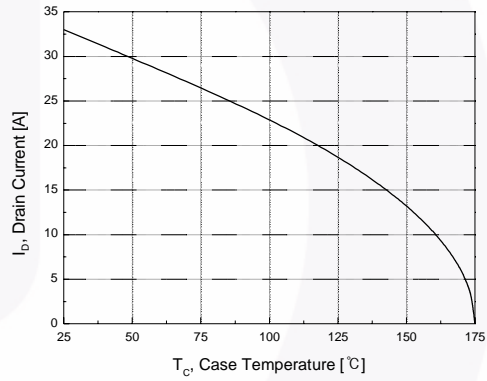


Figure 10. Maximum Drain Current vs. Case Temperature

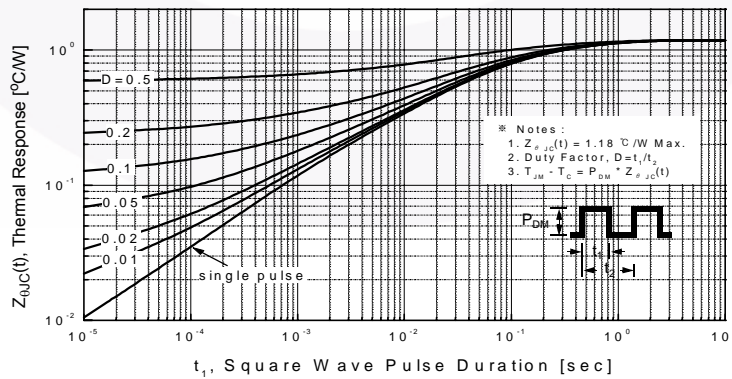


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

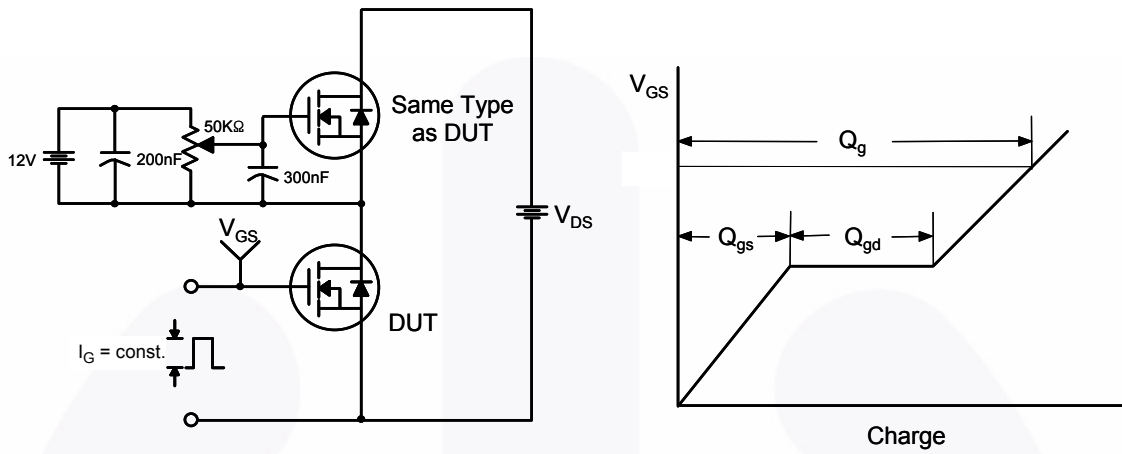


Figure 13. Resistive Switching Test Circuit & Waveforms

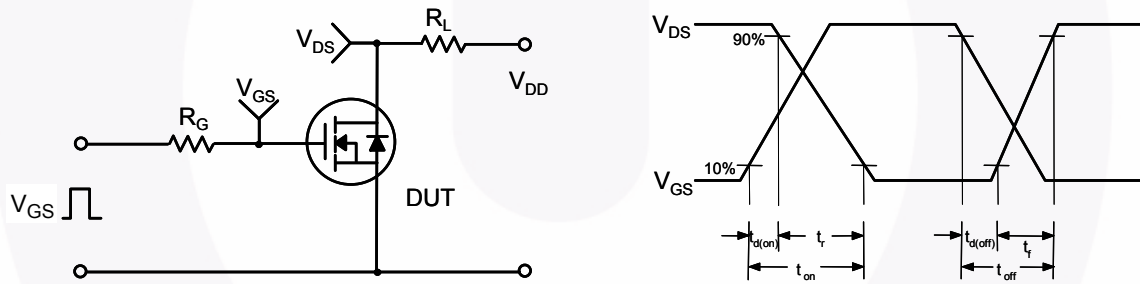


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

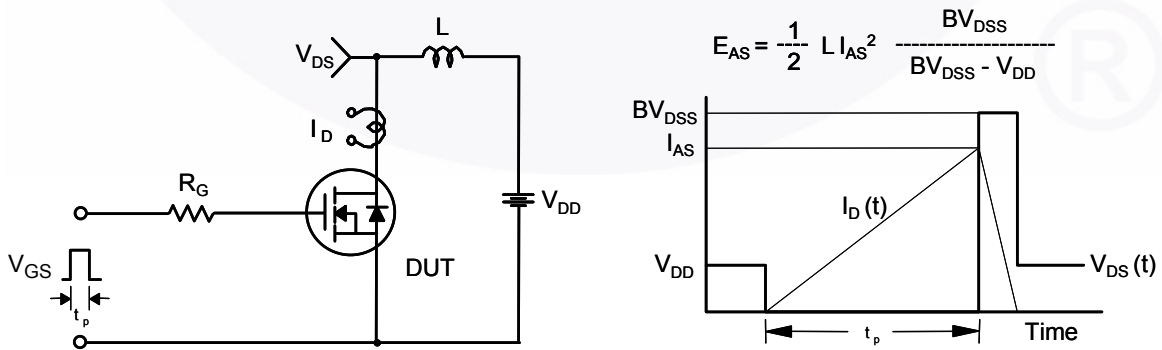
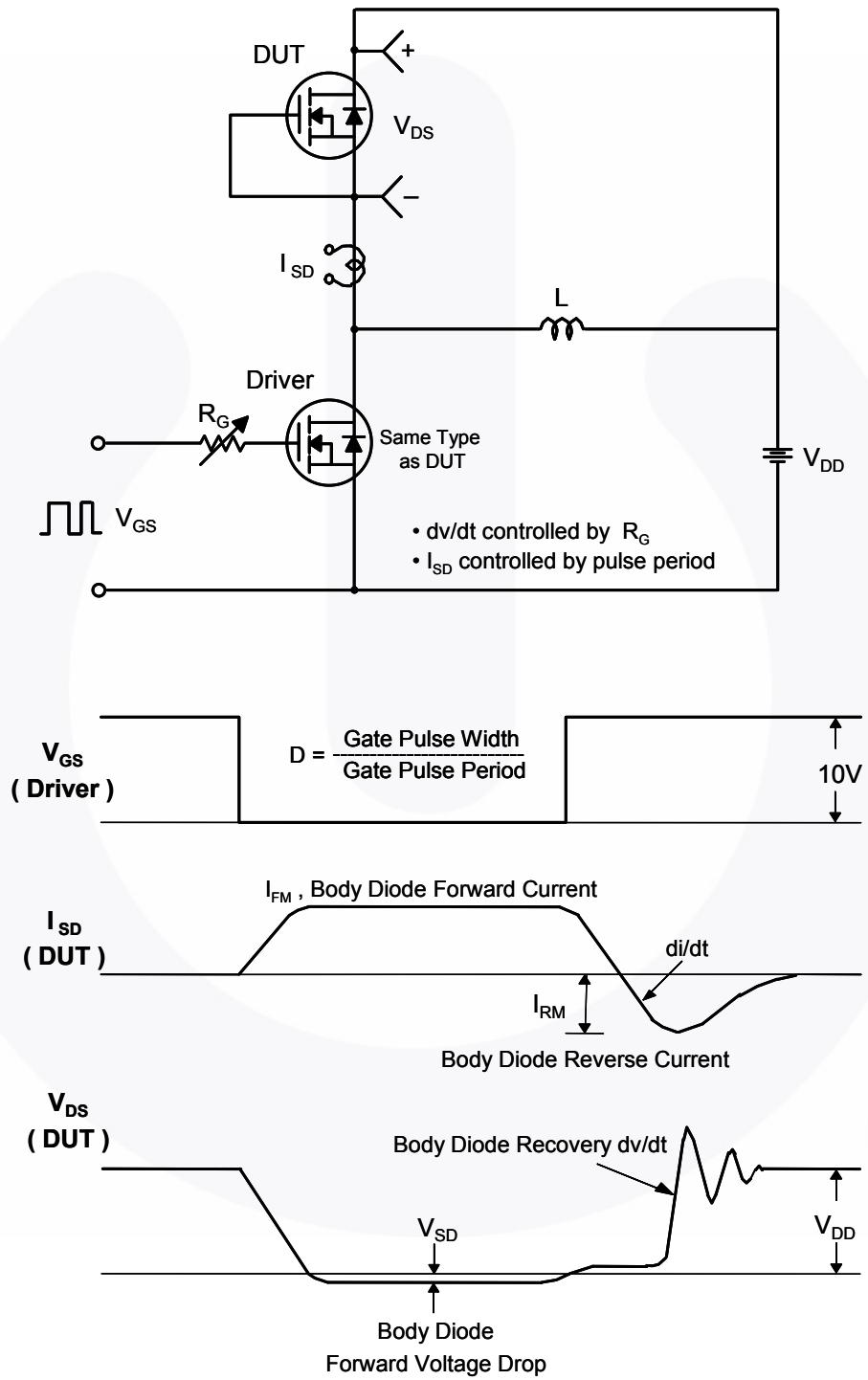


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-263 2L (D²PAK)

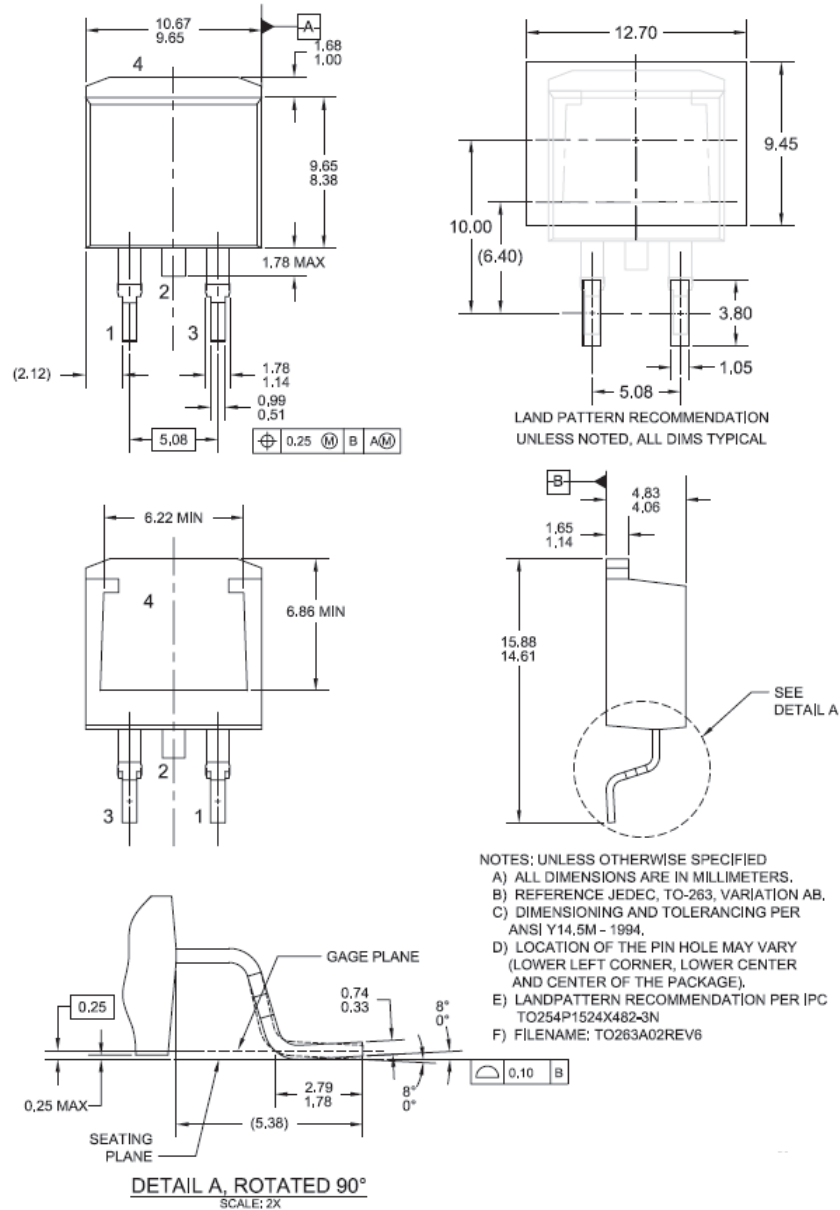


Figure 16. 2LD, TO263, Surface Mount

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Dimension in Millimeters



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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