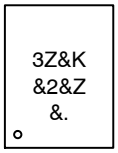
Surge and Over-Voltage Protection Switch for VBUS, CCx and SBUx

FPF3188A

WLCSP56
CASE 567XJ

MARKING DIAGRAM



3Z	= Specific Device Code
&K	= 2−Digits Lot Run Traceability Code
&2	= 2−Digit Date Code Format
&Z	= Assembly Plant Code
&.	= Pin One Dot

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

Description

The FPF3188A features a surge and over voltage protection switch for power and signal paths based on USB type C/PD application.

The FPF3188A has Single Input Dual Output (SIDO) power paths. Channel one (V_{BUS} to V_{OUT}) is an active−low, 28 V/5.5 A rated, power MOSFET switch with an internal clamp supporting surge protection, selectable OVP at 13.9 V or 21.9 V by GPIO. Channel two (V_{BUS} to SYS) is an active−high, 6 V/6 A rated, power MOSFET, fixed OVP at 5.25 V (±250 mV) and Reverse Current Blocking (RCB) during its OFF State.

The FPF3188A has negative 6 V block capability which can withstand unexpected reverse polarity power cable connection.

POK is paired with always ON LDO to power downstream devices when VBUS is greater than 2.7 V, regardless of OVLO, EN0, EN1 and EN2 State. This provides system power supply without battery.

FPF3188A has active discharge path at VBUS which can meet USB type C w/ PD compliance.

FPF3188A has CC1/2 and SBU1/2 signal paths, which offer ±22 V surge protection and over voltage protection to protect system side.

CC1/2 has 26 V/1.5 A rated 150 mΩ switch with typ 5.65 V of OVP and integrated dead battery resistor at CC1/2_C under unpowered or VPWR_SIG < UVLO.

SBU1/2 has 26 V/50 mA rated 1 Ω switch with typ 4.9 V OVP and ultra low leakage current of typ 2 nA.

The FPF3188A is available in a 56−bump, 3.11 mm x 3.41 mm Wafer−Level Chip−Scale Package (WL−CSP) with 0.4 mm pitch.

Features

- OVP Protection Switch for Power and Signal Paths with integrated TVS
- SIDO Power Paths (VBUS to VOUT/SYS)
- ±200 V Surge Protection at V_{BUS}
- −6VDC Block at V_{BUS}
- Low ON−Resistance
  - VOUT Path: typ 27 mΩ
  - SYS Path: typ 33 mΩ
- Selectable OVP Trip Level by GPIO
- Ultra fast OV Response Time: Typ 50 ns
- Always ON LDO Output, POK
- Active Discharge Path at V_{BUS}
- Type−C Signal Paths (CC1/2 and SBU1/2)
- Dedicated VPWR_SIG with UVLO
- ±22 V Surge Protection at CCx_C and SBUx_C
- Low ON−Resistance
  - CC1/2 Path: typ 150 mΩ
  - SBU1/2 Path: typ 1 Ω
- Fixed OVP Trip Level
- Integrated Dead Battery Resistor at CCx_C
- Open Drain OVP FLAGB for Power and Signal Paths
- Over−Temperature Protection (OTP)

Applications

- Mobile Handsets and Tablets

APPLICATION DIAGRAM

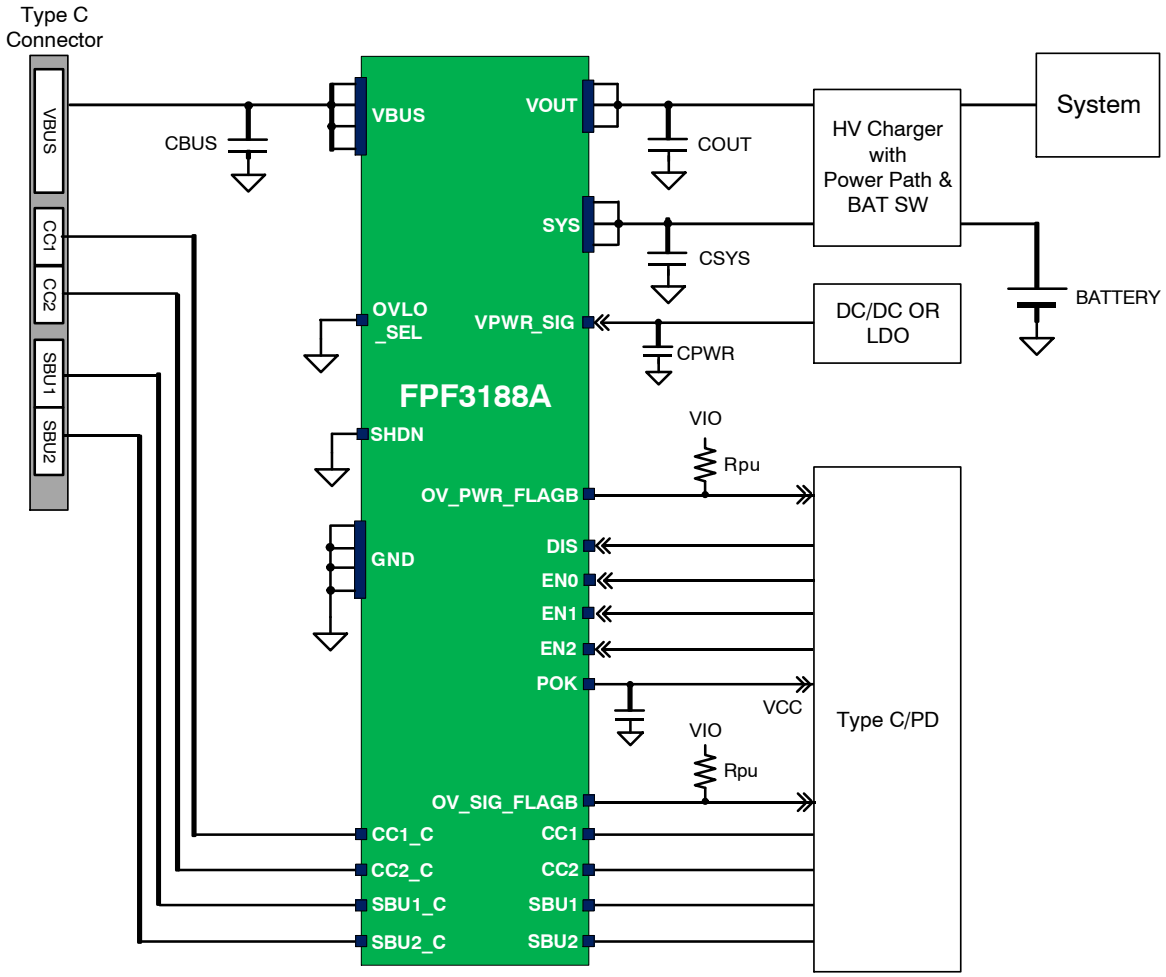


Figure 1. Typical Application

BLOCK DIAGRAM

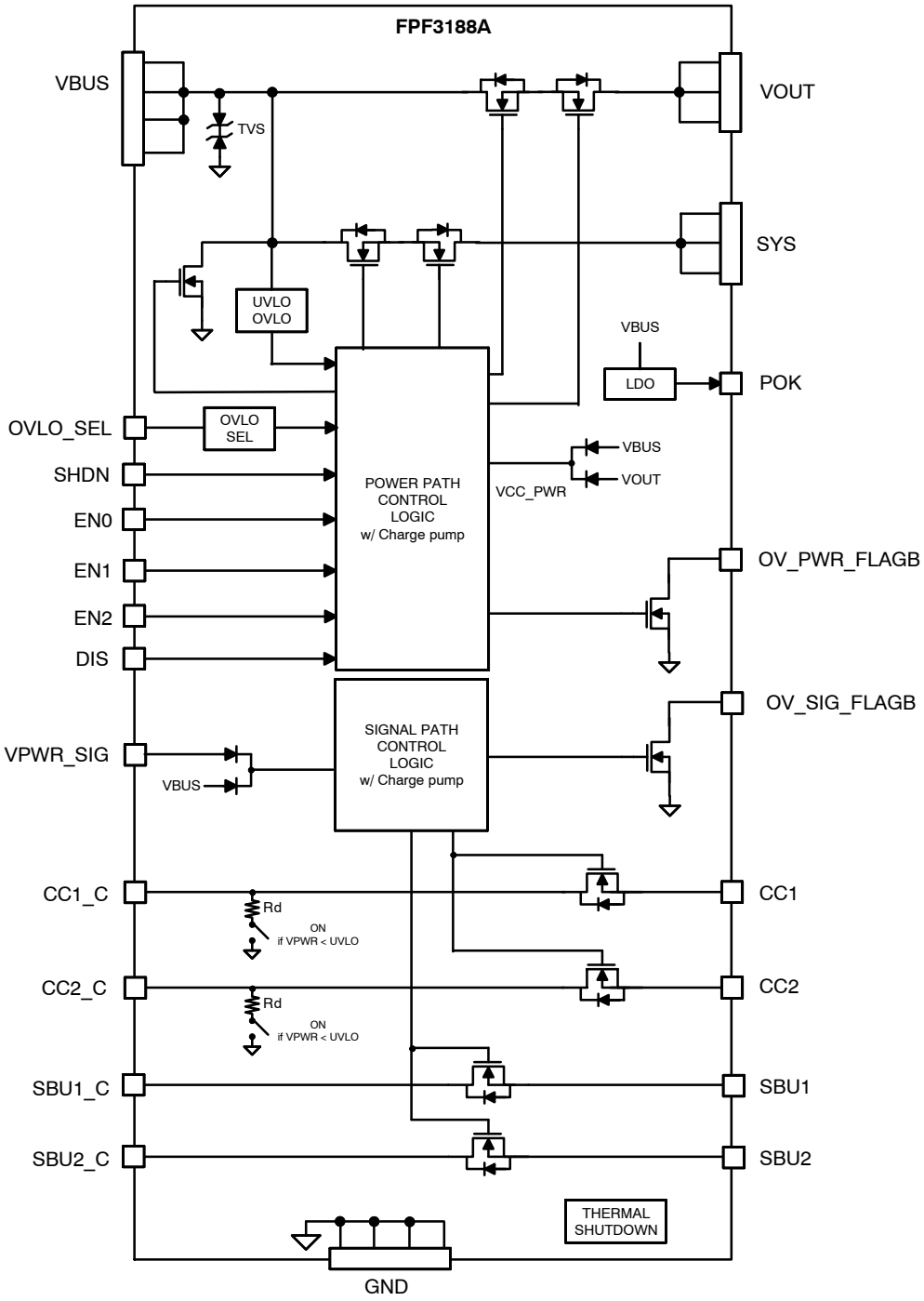


Figure 2. Functional Block Diagram

PIN CONFIGURATION

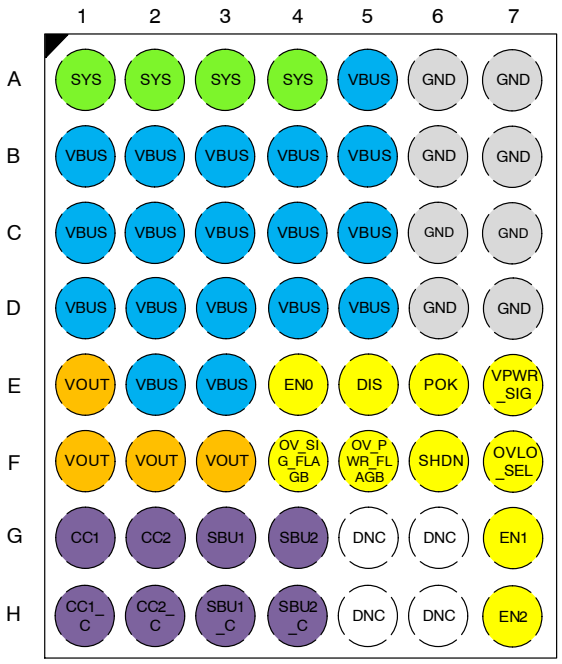


Figure 3. Pin Configuration (Top View)

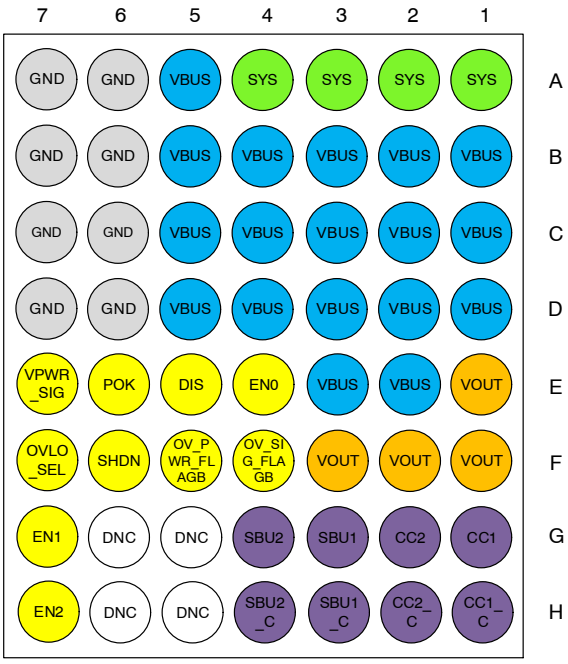


Figure 4. Pin Configuration (Bottom View)

PIN DEFINITIONS

Name	Bump	Type	Description
VBUS	A5, B1~B2, C1~C5, D1~D5, E2, E3	Input/Supply	Switch Input/Output and Power Paths Block Power Supply
VOUT	E1, F1~F3	Output/Supply	Switch Output/Input to Load
SYS	A1~A4	Output	Switch Output to System
POK	E6	Output	Regulated output according to VBUS
EN2	H7	Input	Active HIGH for VBUS to SYS path. Internal pull−down resistor of 1 MΩ is included.
EN1	G7	Input	Active LOW for VBUS to VOUT path. Path control is with both EN0 and EN1. Internal pull−down resistor of 1 MΩ is included.
EN0	E4	Input	Active LOW for VBUS to VOUT path. Path control is with both EN0 and EN1. Internal pull−down resistor of 1 MΩ is included.
SHDN	F6	Input	Active HIGH for whole device shutdown. Internal pull−down resistor of 1 MΩ is included.
DIS	E5	Input	Active HIGH for discharge path at VBUS node. Internal pull−down resistor of 1 MΩ is included.
OVLO_SEL	F7	Input	Over−Voltage Lockout Selection for VOUT path. Internal pull−down resistor of 1 MΩ is included. When OVLO_SEL = LOW then OVLO is set typ 13.9 V. When OVLO_SEL = HIGH then OVLO is set typ 21.9 V.
OV_PWR_FLAGB	F5	Output	Open drain output for OV state for VOUT path. External pull−up resistor with bias voltage are required. If not used, leaves the pin floating.

PIN DEFINITIONS (continued)

Name	Bump	Type	Description
VPWR_SIG	E7	Supply	Signal Paths Block power supply
OV_SIG_FLAGB	F4	Output	Open drain output for OV state for CCx/SBUx path. External pull−up resistor with bias voltage are required. If not used, leaves the pin floating.
CC1_C	H1	Input/Output	Connector side of CC1. Connect with either CC1/2 of type C connector. Integrated dead battery resistor of 5.1 kΩ is included, which is only valid when unpowered.
CC2_C	H2	Input/Output	Connector side of CC2. Connect with either CC1/2 of type C connector. Integrated dead battery resistor of 5.1 kΩ is included, which is only valid when unpowered.
SBU1_C	H3	Input/Output	Connector side of SBU1. Connect with either SBU1/2 of type C connector.
SBU2_C	H4	Input/Output	Connector side of SBU2. Connect with either SBU1/2 of type C connector.
DNC	G5, G6, H5, H6	Dummy	Do not connect to any function nodes. Recommended to connect these pins to ground.
CC1	G1	Input/Output	System side of CC1. Connect with either CC1/2 of Type C controller.
CC2	G2	Input/Output	System side of CC2. Connect with either CC1/2 of Type C controller.
SBU1	G3	Input/Output	System side of SBU1. Connect with either SBU1/2 of Type C controller.
SBU2	G4	Input/Output	System side of SBU2. Connect with either SBU1/2 of Type C controller.
GND	A6, A7, B6, B7, C6, C7, D6, D7	GND	Ground

ORDERING INFORMATION

Device	Operating Temperature Range	Marking	Package	Shipping†
FPF3188AUCX	−40°C − +85°C	3Z	WLCSP−56	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Table 1. ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
VBUS to GND & VBUS to VOUT = GND or Float		VBUS	−6 to 28	V
VOUT to GND		VOUT	−0.3 to 28	V
CC1/2_C, SBU1/2_C to GND		VSIG_C	−0.3 to 26	V
CC1/2, SBU1/2 to GND		VSIG	−0.3 to 6	V
SYS to GND		SYS	−0.3 to 6	V
CC1/2, SBU1/2 to GND		POK, VPWR	−0.3 to 6	V
EN(n), SHDN, DIS, OVLO_SEL, OV_PWR_FLAGB or OV_SIG_FLAGB to GND		$V_{EN(n)\_SHDN\_DIS\_OV\_FLAG}$	−0.3 to 6	V
Continuous VBUS to VOUT Current		$I_{IN\_VBUS\_VOUT}$	5.5	A
Peak VBUS to VOUT Current (5 ms)			11	A
Continuous VBUS to SYS Current		$I_{IN\_VBUS\_SYS}$	6	A
Peak VBUS to SYS Current (5 ms)			12	A
Continuous POK Current		I_{IN_POK}	100	mA
Continuous CCx (VCONN) Current		I_{IN_CCx}	1.5	A
Continuous SBUx Current		I_{IN_SBUx}	50	mA
Total Power Dissipation at T_A = 25°C		t_{PD}	2.6	W
Storage Junction Temperature		T_{STG}	−65 to +150	°C
Operating Junction Temperature		T_J	+150	°C
Lead Temperature (Soldering, 10 Seconds)		T_L	+260	°C
Human Body Model, ANSI/ESDA/JEDEC JS−001	Electrostatic Discharge Capability	ESD	2	kV
Charged Device Model, JESD22−C101			1	
Air Discharge at VBUS	IEC61000−4−2 System Level		15	
Contact Discharge at VBUS			3	
Contact Discharge at CCx_C, SBUx_C			3	
V_{BUS}	IEC 61000−4−5	Surge	−200 to +200	V
CCx_C, SBUx_C			−22 to +22	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 2. THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction−to−Ambient (1in.^{2} pad of 2 oz. copper) (Note 1)	$R_{\theta JA}$	48	°C/W

1. Measured using 2S2P JEDEC std. PCB.

Table 3. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
VBUS Operating Voltage	V_{BUS}	2.7	21.5	V
CCx_C Operating Voltage	V_{CCx}	0	5.5	V
SBUx_C Operating Voltage	V_{SBUx}	0	4.6	V
VPWR_SIG Bias Voltage	V_{PWR_SIG}	2.7	5.5	V
Capacitance for VPWR_SIG	C_{PWR}	1	–	μF
Input Capacitance for VBUS	C_{IN}	1	–	μF
Output Capacitance for VOUT	C_{OUT}	1	–	μF
Capacitance for SYS	C_{SYS}	4.7	–	μF
Capacitance for POK	C_{POK}	4.7	–	μF
Ambient Operating Temperature, T_A	T_A	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS V_{BUS} = 2.7 to 21 V, T_A = −40 to 85°C; Typical values are at VBUS = 5 V, $I_{IN} \le 1$ A, SHDN = EN0 = EN1 = EN2 = DIS = LOW, OVLO_SEL = GND, VPWR_SIG = 3.8 V, SBUx_C = 1.5 V, CCx_C = 5 V, POK = Floating, C_{IN} = 1 μF and T_A = 25°C; unless otherwise noted.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Power Paths: SIDO (Single Input Dual Output) VBUS to VOUT and SYS Switch						
BASIC OPERATION						
Power Input Quiescent Current	VBUS = 5 V, EN0 = EN1 = EN2 = LOW	I_{Q_PWR}	80	160	250	μA
	VBUS = 4 V, EN0 = EN1 = EN2 = HIGH		70	145	230	
OVLO Supply Current	VBUS = 15 V, VOUT = 0 V, EN0 = EN1 = EN2 = LOW, OVLO_SEL = GND	$I_{IN\_Q\_PWR}$	130	230	330	μA
	VBUS = 5.5 V, SYS = 0 V, EN0 = EN1 = EN2 = HIGH		70	150	250	μA
Shutdown Current	VBUS = 4.4 V, SHDN = 1.8 V	I_{SD}	–	–	1	μA
Under−Voltage Trip Level	VBUS Rising, T_A = −40 to 85°C	V_{BUS_UVLO}	2.35	2.5	2.65	V
	VBUS Falling, T_A = −40 to 85°C		2.2	2.35	2.5	V
Soft−Start Time	Time from VBUS = VBUS_UVLO to 0.1 x POK	T_{VBUS_START}	–	30	–	ms
VBUS Discharge Resistance	VBUS = 5 V, DIS = 1.8 V	R_{VBUS_PD}	450	600	750	Ω
VBUS Discharge ON Delay Time	VOUT = 5 V Time from DIS = HIGH to Discharge path ON	$t_{VBUS\_DIS\_ON}$	–	0.5	–	μs
VBUS Discharge OFF Delay Time	VOUT = 5 V Time from DIS = LOW to Discharge path OFF	$t_{VBUS\_DIS\_OFF}$	–	1	–	μs
VBUS Discharge Time	VOUT = weak 5 V, CBUS = 1 uF, DIS = EN1 = LOW to HIGH Time from 5 V to 0.5 V at VBUS	t_{VBUS_DIS}	–	3	–	ms
Thermal Shutdown (Note 2)		T_{SDN}	–	140	–	°C
Thermal Shutdown Hysteresis (Note 2)		T_{SDN_HYS}	–	20	–	°C
INTERGRATED BI−DIRECTIONAL TVS						
Positive Reverse Working Voltage		V_{RW_P}	–	–	28	V
Positive Breakdown Voltage	I_{IN} = 1 mA	V_{BR_P}	–	30	–	V
Positive Clamping Voltage (Note 2)	+200 V surge	V_{CL_P}	–	31	–	V
Negative Reverse Working Voltage		V_{RW_N}	−6	–	–	V
Negative Breakdown Voltage	I_{IN} = −1 mA	V_{BR_N}	–	−7	–	V
Negative Clamping	−200 V surge	V_{CL_N}	–	−6	–	V
Voltage (Note 2)			–	–	–	
VBUS TO VOUT SWITCH						
Over−Voltage Trip Level	VBUS Rising, OVLO_SEL = GND T_A = −40 to 85°C	V_{OUT_OVLO}	13.5	13.9	14.3	V
	VBUS Falling, OVLO_SEL = GND T_A = −40 to 85°C		13.3	13.7	14.1	
	VBUS Rising, OVLO_SEL = HIGH T_A = −40 to 85°C		21.4	21.9	22.4	
	VBUS Falling, OVLO_SEL = HIGH T_A = −40 to 85°C		21.0	21.5	22.0	
On−Resistance	VBUS = 5 V, I_{OUT} = 200 mA, T_A = 25°C	R_{ON_VOUT}	20	27	36	mΩ
	VBUS = 12 V, I_{OUT} = 200 mA, T_A = 25°C		20	27	36	
	VBUS = 20 V, I_{OUT} = 200 mA, T_A = 25°C		20	27	36	
Debounce Time	Time from V_{BUS_UVLO} < VBUS < V_{BUS_OVLO} to VOUT = 0.1 x VBUS	t_{DEB_VOUT}	–	15	–	ms

Table 4. ELECTRICAL CHARACTERISTICS V_{BUS} = 2.7 to 21 V, T_A = −40 to 85°C; Typical values are at VBUS = 5 V, $I_{IN} \le 1$ A, SHDN = EN0 = EN1 = EN2 = DIS = LOW, OVLO_SEL = GND, VPWR_SIG = 3.8 V, SBUx_C = 1.5 V, CCx_C = 5 V, POK = Floating, C_{IN} = 1 μF and T_A = 25°C; unless otherwise noted. (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VBUS TO VOUT SWITCH						
Switch Turn−On Time	R_L = 100 Ω, C_L = 1 μF, VOUT from 0.1 x VBUS to 0.9 x VBUS	t_{ON_VOUT}	−	0.4	−	ms
Switch Turn−Off Time (Note 2)	R_L = 100 Ω, No C_L, VBUS > V_{OUT_OVLO} to V_{OUT} = 0.9 x VBUS	t_{OFF_VOUT}	−	50	90	ns
VOUT TO VBUS SWITCH (OTG MODE)						
On−Resistance	VOUT = 5 V, I_{BUS} = 200 mA, T_A = 25°C	R_{ON_OTG}	20	27	36	mΩ
ON Delay Time	VOUT = 5 V, Time from EN0 = EN1 = HIGH → LOW to VBUS = 0.1 x VOUT	t_{DON_OTG}	−	20	−	ms
Switch Turn−On Time	VOUT = 5 V, R_L = 10 Ω, C_L = 1 μF, VBUS from 0.1 x VOUT to 0.9 x VOUT	t_{ON_OTG}	−	700	−	μs
OFF Delay Time	VOUT = 5 V, Time from EN0 = EN1 = LOW → HIGH to VBUS = 0.9 x VOUT	t_{DOFF_OTG}	−	85	−	μs
Switch Turn−Off Time	VOUT = 5 V, R_L = 1 kΩ, C_L = 1 μF, EN0 = EN1 = LOW → HIGH VBUS from 0.9 x VOUT to 0.1 x VOUT	t_{OFF_OTG}	−	4	−	ms
VBUS TO SYS SWITCH						
Over−Voltage Trip Level	VBUS Rising, T_A = −40 to 85°C	V_{SYS_OVLO}	5.00	5.25	5.50	V
	VBUS Falling, T_A = −40 to 85°C		4.8	−	5.3	
On−Resistance	VBUS = 3 V, I_{OUT} = 200 mA, T_A = 25°C	R_{ON_SYS}	28	33	40	mΩ
Reverse Current (Note 2)	VBUS = 0 V, SYS = 4.4 V, T_A = 25°C	I_{RCB}	0.1	2	100	nA
Debounce Time	Time from V_{BUS_UVLO} < VBUS < V_{BUS_OVLO} to SYS = 0.1 x VBUS	t_{DEB_SYS}	−	15	−	ms
Switch Turn−On Time	R_L = 100 Ω, C_L = 1 μF, VOUT from 0.1 x VBUS to 0.9 x VBUS	t_{ON_SYS}	−	0.3	−	ms
Switch Turn−Off Time (Note 2)	R_L = 100 Ω, No CL, VBUS > V_{SYS_OVLO} to SYS = 0.9 x VBUS	t_{OFF_SYS}	−	50	90	ns
POK						
POK Output Voltage	VBUS = 5 V, I_POK = 0 mA, T_A = 25°C	POK	3.6	3.8	4.0	V
	VBUS = 20 V, I_POK = 0 mA, T_A = 25°C		3.6	3.8	4.0	
	VBUS = 5 V, I_POK = 100 mA, T_A = 25°C		3.6	3.8	4.0	
	VBUS = 20 V, I_POK = 100 mA, T_A = 25°C		3.6	3.8	4.0	
DIGITAL SIGNALS						
FLAGB Output LOW Voltage OV_PWR_FLAGB	VI/O = 1.8 V, R_{PU} = 100 kΩ	$V_{FLAGB\_PWR\_OL}$	0.01	−	0.4	V
FLAGB Assertion Delay Time OV_PWR_FLAGB	Time from VBUS = V_{OUT_OVLO} to OV_PWR_FLAGB assertion	$t_{FLAGB\_PWR\_DELAY}$	−	−	3	μs
FLAGB Recovery de− bounce Time OV_PWR_FLAGB	Time from VBUS = V_{OUT_OVLO} to OV_PWR_FLAGB de−assertion	$t_{FLAGB\_PWR\_REC}$	−	15	−	ms
Internal Pull−Down Resistor at EN0, EN1, EN2, DIS, OVLO_SEL and SHDN		$R_{PD\_EN(n)\_DIS\_OV\_SHDN}$	0.7	1	1.3	MΩ
Logic Enable HIGH Voltage	VBUS operating range	$V_{IH\_EN(n)\_DIS\_OV\_SHDN}$	1.2	−	−	V
Logic Enable LOW Voltage	VBUS operating range	$V_{IL\_EN(n)\_DIS\_OV\_SHDN}$	−	−	0.5	V
POK Leakage Current	V_{POK} = 5 V, VBUS = 0 V	I_{POK_LEAK}	0.1	−	1	μA

Table 4. ELECTRICAL CHARACTERISTICS V_{BUS} = 2.7 to 21 V, T_A = −40 to 85°C; Typical values are at VBUS = 5 V, $I_{IN} \le 1$ A, SHDN = EN0 = EN1 = EN2 = DIS = LOW, OVLO_SEL = GND, VPWR_SIG = 3.8 V, SBUx_C = 1.5 V, CCx_C = 5 V, POK = Floating, C_{IN} = 1 μF and T_A = 25°C; unless otherwise noted. (continued)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Signal Paths: CC1/2 AND SBU1/2 Switch						
BASIC OPERATION						
Signal Input Quiescent Current	VPWR_SIG = 3.8 V, VBUS = 0 V	I_{Q_SIG}	30	44	60	μA
	VPWR_SIG = 2.2 V, VBUS = 0 V		0.45	1	3	
Under−Voltage Trip Level	VPWR_SIG Rising, T_A = −40 to 85°C	V_{PWR_UVLO}	2.4	2.52	2.65	V
	VPWR_SIG Falling, T_A = −40 to 85°C		2.25	2.38	2.5	
Debounce Time	Time from VPWR_SIG > V_{PWR_UVLO} to CCx/SBUx = 0.1 x CCx_C/SBUx_C	t_{DEB_SIG}	−	5	−	ms
Switch Turn−Off Time (Note 2)	R_L = 10 MΩ, No CL, VSIG_C > V_{UVLO} to VSIG = 0.9 x VBUS	t_{OFF_SIG}	−	50	90	ns
CC1 AND CC2 SWITCH						
On−Resistance	I_{OUT} = 100 mA, T_A = 25°C	R_{ON_CCx}	70	150	250	mΩ
Over−Voltage Trip Level	CCx_C Rising, T_A = −40 to 85°C	V_{CCx_OVLO}	5.40	5.65	5.75	V
	CCx_C Falling, T_A = −40 to 85°C		5.30	5.55	5.65	V
On−Capacitance (Note 2)	CCx_C = 0~1.2 V, Freq = 400 kHz	C_{ON_CCx}	−	30	−	pF
Off−Capacitance (Note 2)	CCx_C = 0~1.2 V, Freq = 400 kHz, VPWR_SIG < UVLO	C_{OFF_CCx}	−	80	−	pF
ON Band Width (Note 2)	−3 dB BW from CCx_C to CCx, R_L = 50 Ω, C_L = 200 pF, SDD21	BW_{CCx}	−	10	−	MHz
CCx_C to GND Resistance (Note 2)	CCx_C = 4.4 V, Freq = 10 Hz	R_{CCx_C}	5	−	−	MΩ
Integrated Dead BAT Resistance	VPWR_SIG < VPWR_UVLO, CCx_C = 2.6 V, T_A = 25°C	R_{DEAD_BAT}	4.1	5.1	6.1	kΩ
	(Only valid when unpowered)					
SBU1 AND SBU2 SWITCH						
On−Resistance	I_{OUT} = 30 mA, T_A = 25°C	R_{ON_SBUx}	0.6	0.8	1.0	Ω
Over−Voltage Trip Level	SBUx_C Rising, T_A = −40 to 85°C	V_{SBUx_OVLO}	4.75	4.9	5.0	V
	SBUx_C Falling, T_A = −40 to 85°C		4.6	4.75	4.85	V
On−Capacitance (Note 2)	SBUx_C = 0.1 V, Freq = 1 MHz	C_{ON_SBUx}	−	20	−	pF
Band Width (Note 2)	−3 dB BW from SBUx_C to SBUx, R_L = 50 Ω, C_L = 5 pF	BW_{SBUx}	−	100	−	MHz
SBUx_C to GND Resistance (Note 2)	SBUx_C = 4.4 V, Freq = 10 Hz	R_{SBUx_C}	5	−	−	MΩ
SBUx_C Leakage Current (Note 2)	SBUx_C = 2.0 V, SBUx = floating, T_A = 25°C	I_{SBUx_Leak}	0.01	0.2	1	nA
DIGITAL SIGNALS						
FLAGB Output LOW Voltage OV_SIG_FLAGB	VI/O = 1.8 V, R_{PU} = 100 kΩ	$V_{FLAGB\_SIG\_OL}$	0.01	−	0.4	V
FLAGB Assertion Delay Time OV_SIG_FLAGB	Time from Pin_C = V_{OVLO} to OV_SIG_FLAGB assertion	$t_{FLAGB\_SIG\_DELAY}$	−	−	3	μs
FLAGB Recovery De−bounce Time OV_SIG_FLAGB	Time from Pin_C = V_{OVLO} to OV_SIG_FLAGB de−assertion	$t_{FLAGB\_SIG\_REC}$	−	8	−	ms

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Guaranteed by design and characterization.

OPERATIONS

VBUS TO VOUT PATH (CHARGING MODE) ON/OFF BY EN0 AND EN1 (VBUS > UVLO)

EN0	EN1	SHDN	VBUS to VOUT Path
LOW	LOW	LOW	ON (Closed)
LOW	HIGH	LOW	OFF (Open)
HIGH	X	LOW	OFF (Open)
X	X	HIGH	OFF (Open)

VOUT TO VBUS PATH (OTG MODE) ON/OFF BY VPWR_SIG AND VOUT (EN0 = EN1 = LOW)

VPWR_SIG	VOUT > VBUS	SHDN	VOUT to VBUS Path
< UVLO	X	LOW	OFF (Open)
> UVLO	YES	LOW	ON (Closed), OTG Mode
> UVLO	NO	LOW	ON (Closed), Charge Mode
X	X	HIGH	OFF (Open)

VBUS TO SYS PATH (FACTORY TEST MODE) ON/OFF BY EN2

EN2	SHDN	VBUS to SYS Path
LOW	LOW	OFF (Open)
HIGH	LOW	ON (Closed)
X	HIGH	OFF (Open)

SIGNAL PATHS (CCx AND SBUx) ON/OFF BY VPWR_SIG AND VBUS

VBUS	VPWR_SIG	SHDN	Signal Paths	Dead BAT on CCx_C
< UVLO	< UVLO	LOW	OPEN	5.1 kΩ R_{DEAD_BAT} is seen
> UVLO	X	LOW	CLOSED	Floating
X	> UVLO	LOW	CLOSED	Floating
X	X	HIGH	OPEN	Floating

TIMING DIAGRAMS

VBUS to VOUT Path

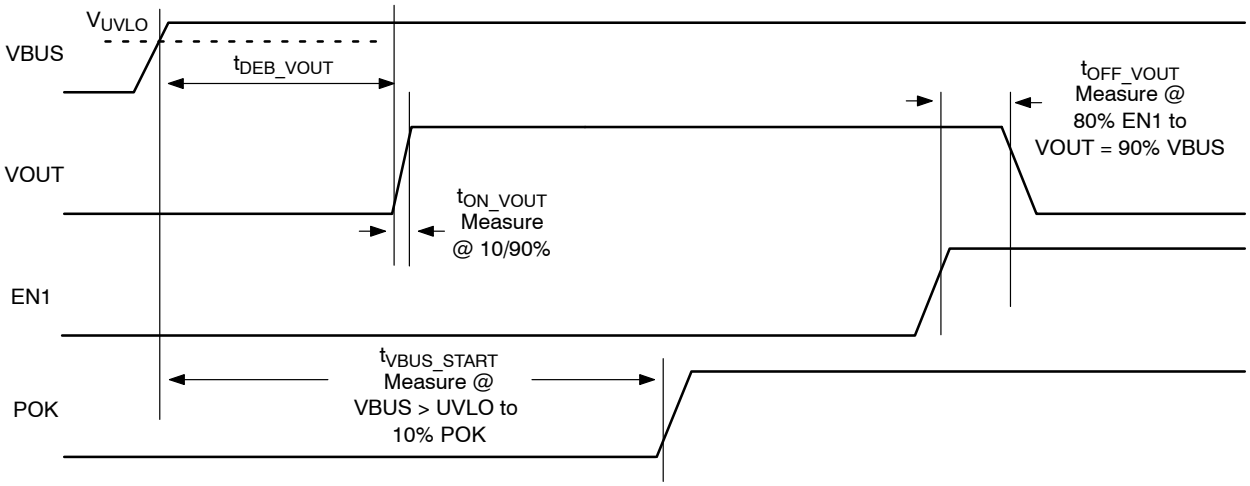


Figure 5. VBUS to VOUT Power Up/Down and Normal Operation (EN0 = LOW)

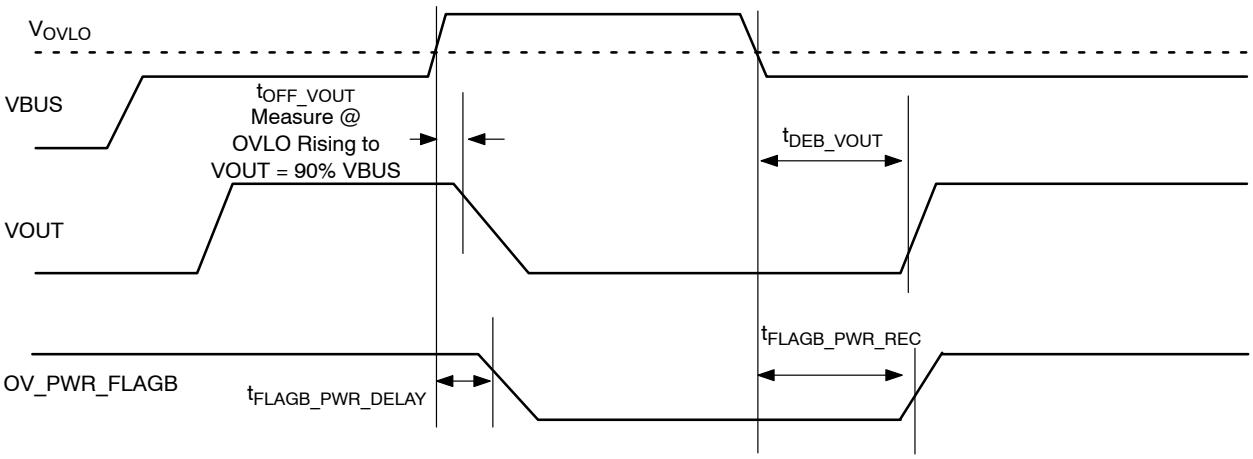


Figure 6. VBUS to VOUT OVLO Operation (EN0 = EN1 = LOW)

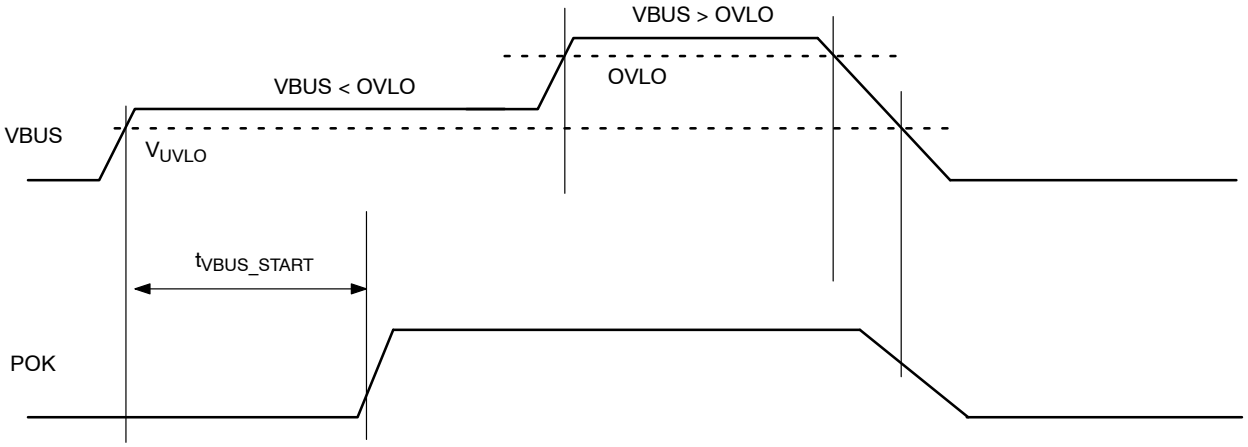


Figure 7. Always ON Based POK Operation (EN0 = X, EN1 = X, EN2 = X & SHDN = LOW)

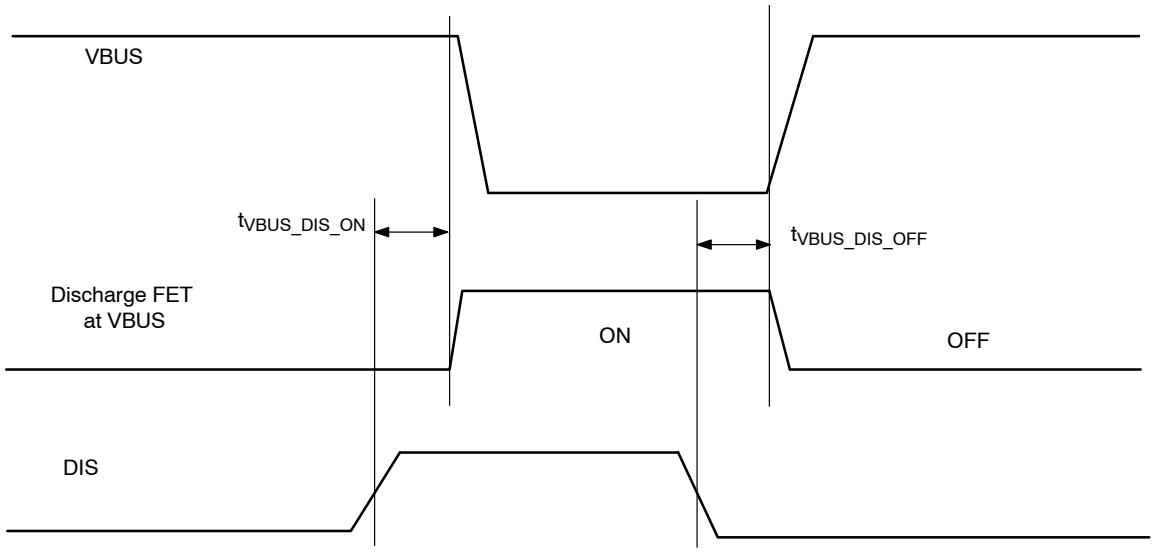


Figure 8. VBUS Discharge Operation by DIS Pin (EN0 = X, EN1 = X, EN2 = X, SHDN = LOW & VOUT = weak 5 V)

VOUT to VBUS Path (OTG Mode)

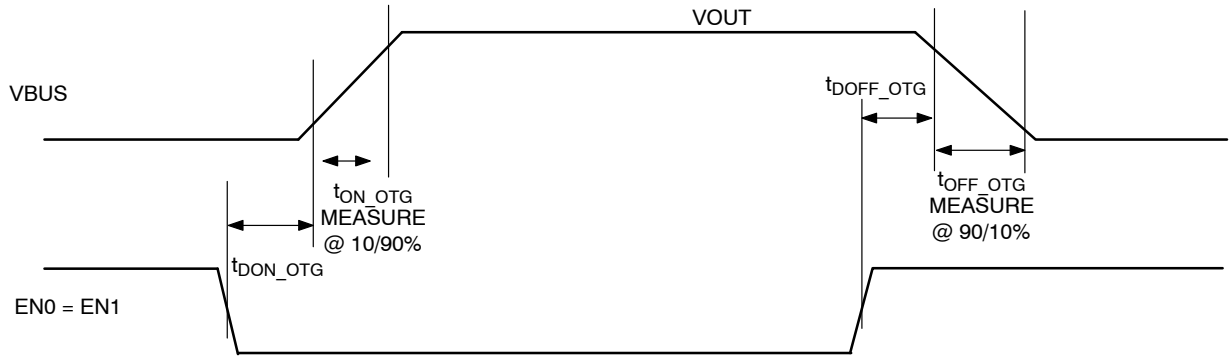


Figure 9. OTG Mode Operation (VOUT = 5 V, VPWR_SIG > UVLO)

VBUS to SYS Path

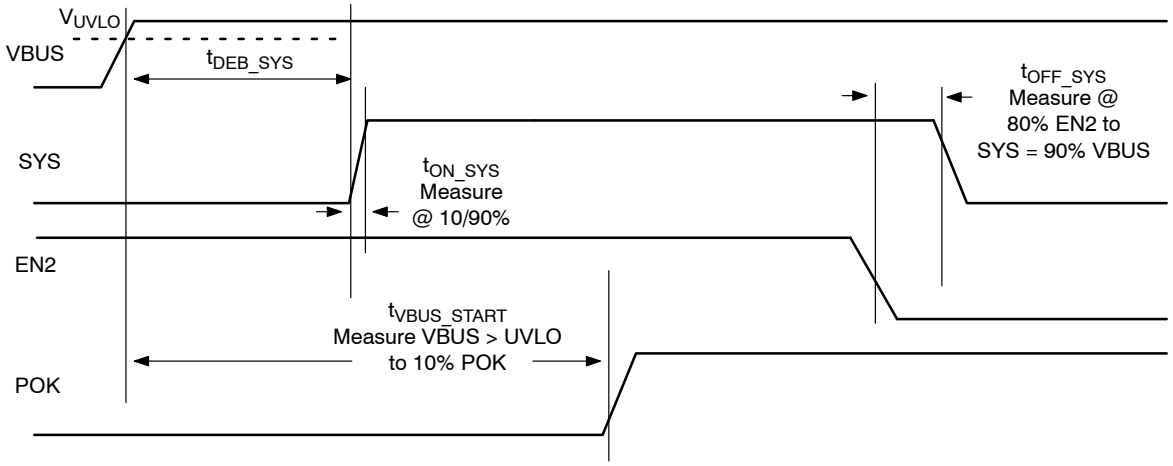


Figure 10. VBUS to SYS Power Up/Down and Normal Operation

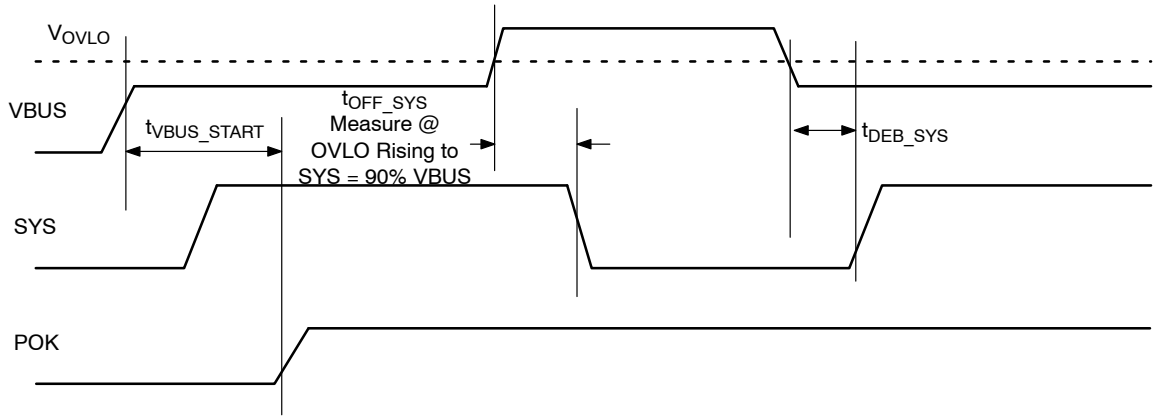


Figure 11. VBUS to SYS OVLO Operation (EN2 = HIGH)

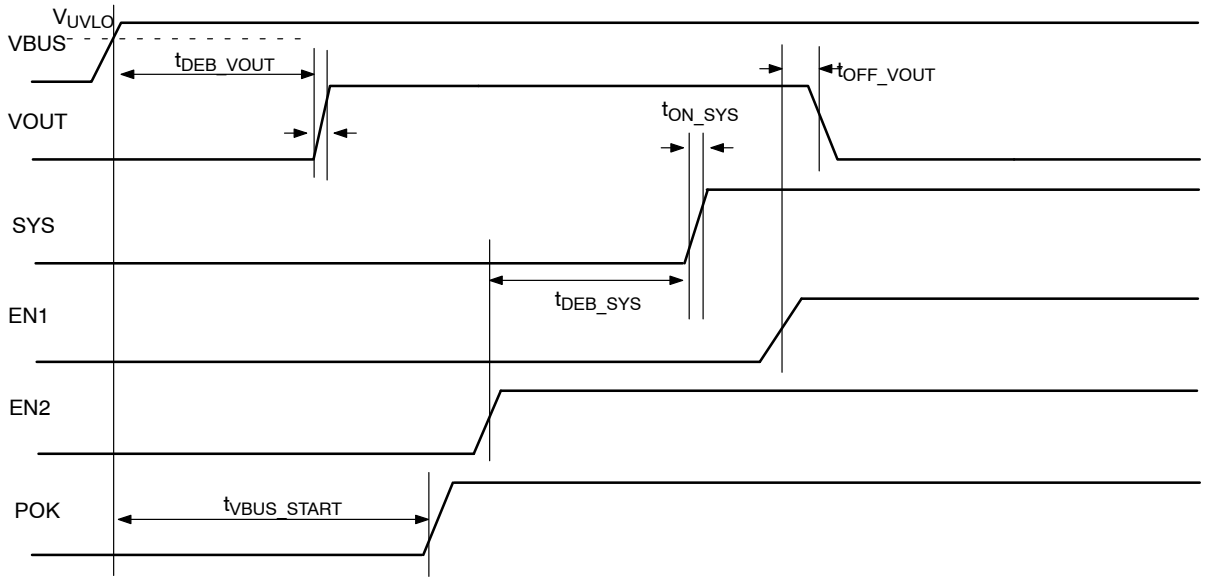


Figure 12. Overall Power Path ON/OFF Operation (EN0 = SHDN = LOW)

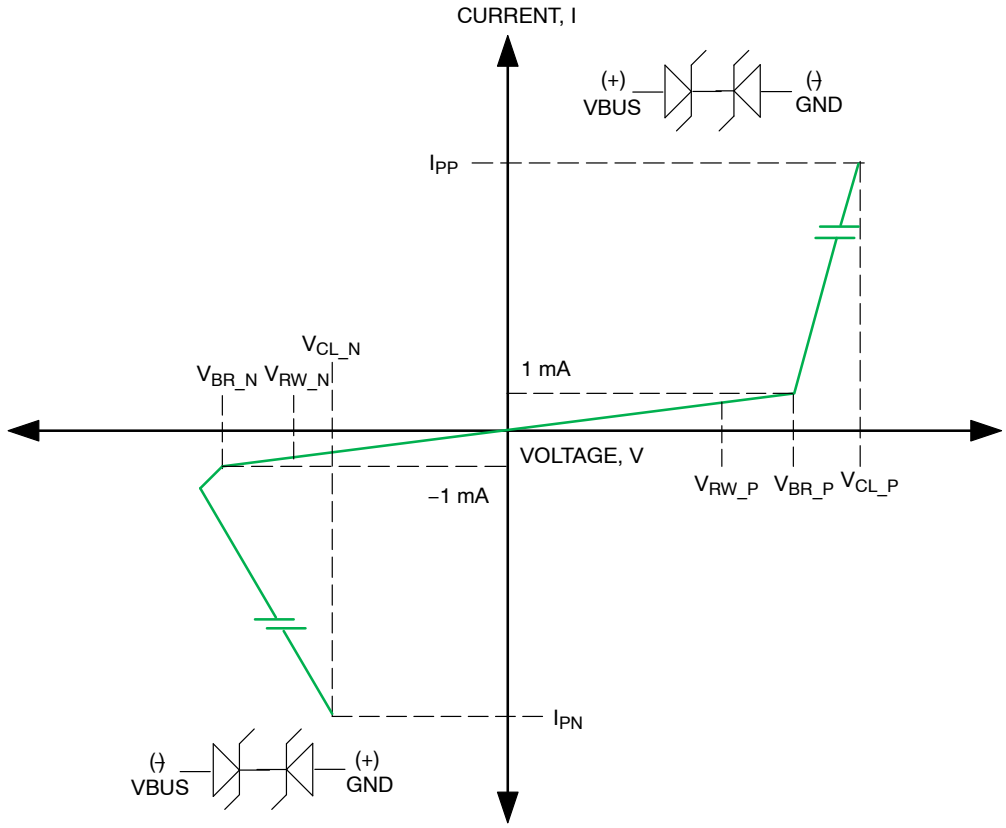


Figure 13. Integrated TVS IV Curve at VBUS

CCx/SBUx Path

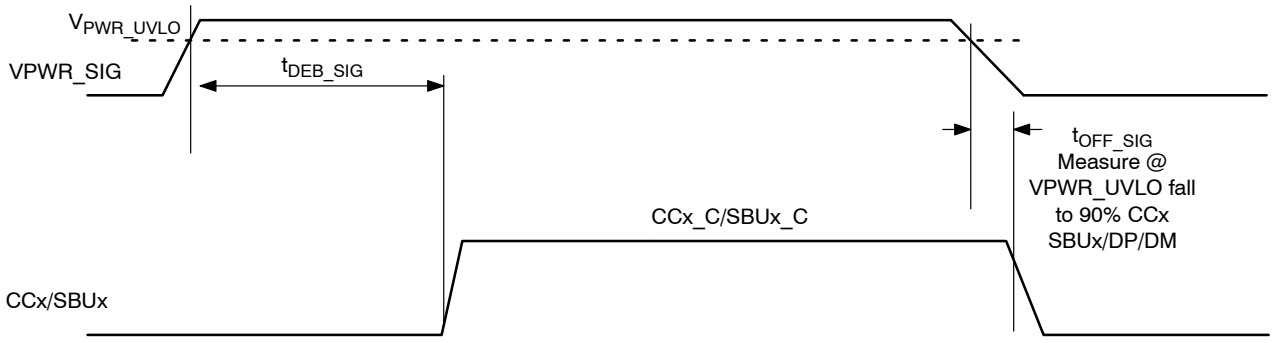


Figure 14. CCx_C/SBUx_C to CCx/SBUx Power Up/Down (VBUS < UVLO)

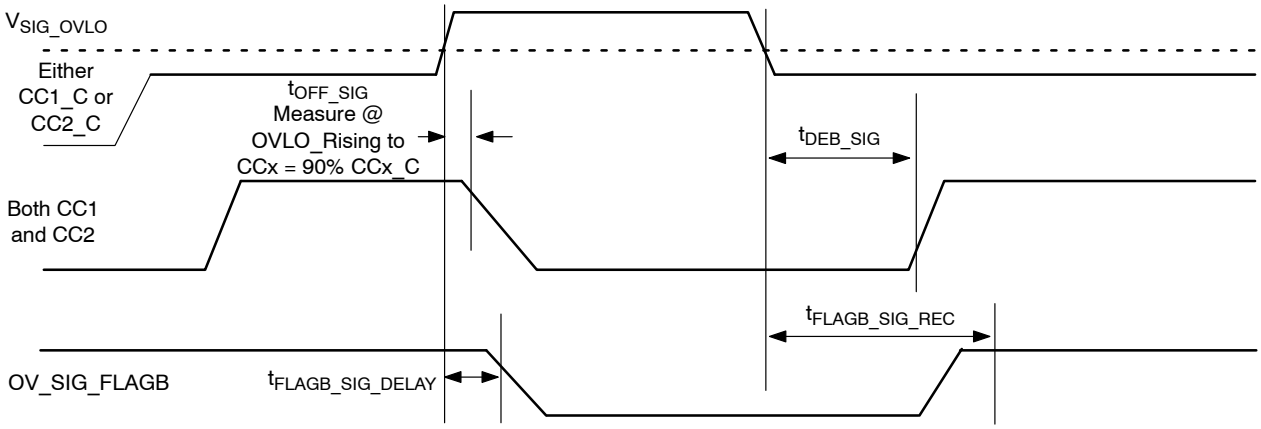


Figure 15. CCx_C to CCx OVLO Operation (Either VBUS or VPWR_SIG > UVLO)

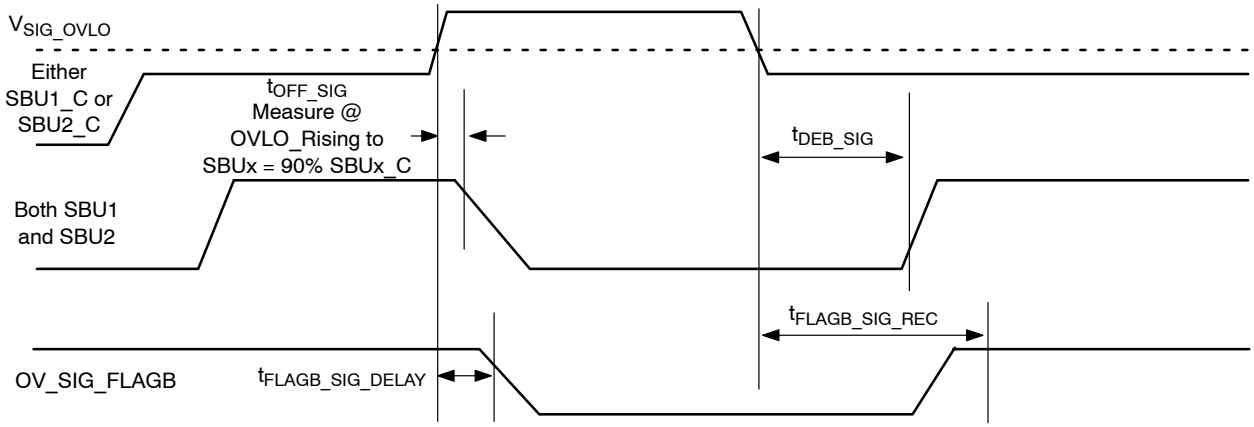


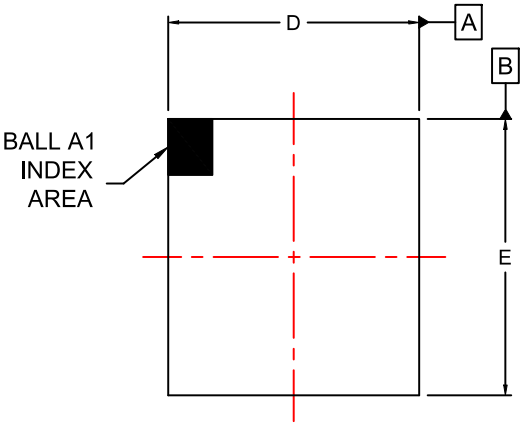
Figure 16. SBUx_C to SBUx OVLO Operation (Either VBUS or VPWR_SIG > UVLO)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

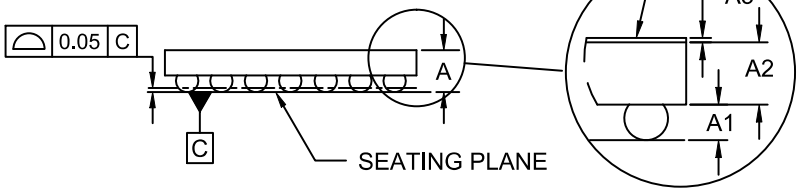
ON Semiconductor®

WLCSP56 3.11x3.41x0.599
CASE 567XJ
ISSUE O

DATE 12 FEB 2019



TOP VIEW



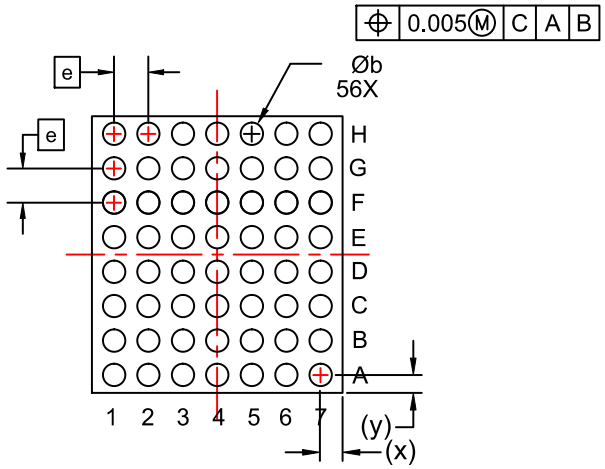
SIDE VIEW

DETAIL A

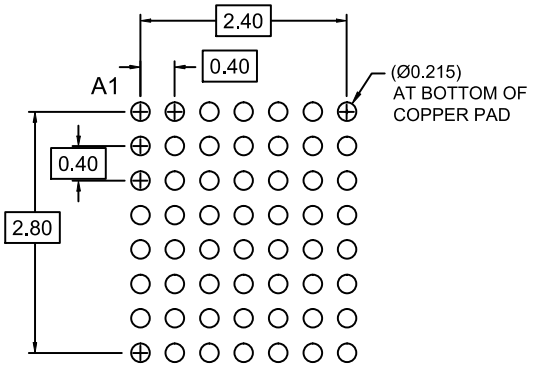
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DATUM C APPLIES TO THE SPHERICAL CROWN OF THE SOLDER BALLS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.558	0.599	0.640
A1	0.174	0.194	0.214
A2	0.362	0.380	0.398
A3	0.022	0.025	0.028
b	0.240	0.260	0.280
D	3.080	3.110	3.140
E	3.380	3.410	3.440
e	0.40 BSC		
x	0.340	0.355	0.370
y	0.290	0.305	0.320



BOTTOM VIEW



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