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FMS6141
Low-Cost, Single-Channel 4th-Order Standard Definition Video Filter Driver

Features

- Single 4th-Order 8 MHz (SD) Filter
- Drives Single, AC- or DC-coupled, Video Loads ($2\ V_{pp}$, 150 Ω)
- Drives Dual, AC- or DC-coupled, Video Loads ($2V_{pp}$, 75Ω)
- Transparent Input Clamping
- AC- or DC-Coupled Input
- AC- or DC-Coupled Output
- DC-Coupled Output Eliminates AC-Coupling Capacitors
- Single Supply
- Robust 8 kV ESD Protection
- Lead-Free Packages: SOIC-8 or SC70-5

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players
- HDTVs
- Personal Video Recorders (PVR)
- Video On Demand (VOD)

Description

The FMS6141 Low-Cost Video Filter is intended to replace passive LC filters and drivers with a low-cost integrated device. The 4th-order filter provides improved image quality compared to typical 2nd or 3rd-order passive solutions.

The FMS6141 may be directly driven by a DC-coupled DAC output or an AC-coupled signal. Internal diode clamps and bias circuitry may be used if an AC-coupled input is required *(see Application Information for details).*

The FMS6141's output can drive an AC- or DC-coupled single (150 Ω) or dual (75 Ω) load. DC-coupling the output removes the need for output coupling capacitors. The input DC level is offset approximately +280 mV at the output (*see Application Information for details).*

Related Applications Notes

- http://www.onsemi.com/pub/Collateral/AN-6041.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN-6024.pdf.pdf

Functional Block Diagram

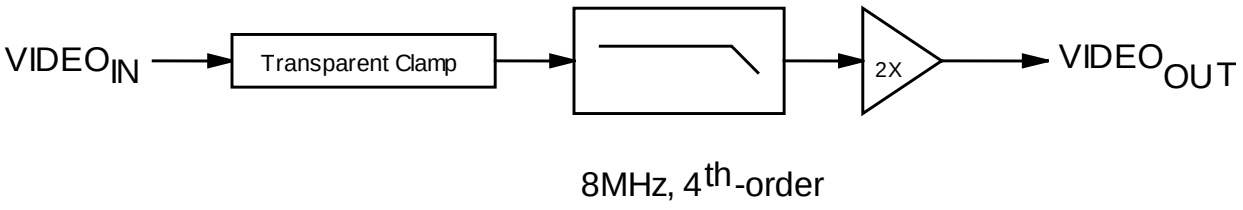


Figure 1. Block Diagram

August-2024, Rev. 3
Publication Order Number:
FMS6141/D

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FMS6141CSX	-40°C to +85°C	8-Lead, Small Outline Integrated Circuit (SOIC)	Tape and Reel
FMS6141S5X	-40°C to +85°C	5- Lead SC70 Package	Tape and Reel

Pin Configurations

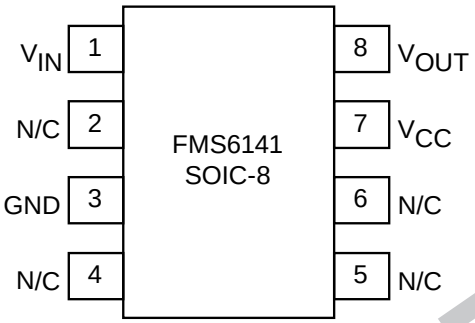


Figure 2. SOIC-8

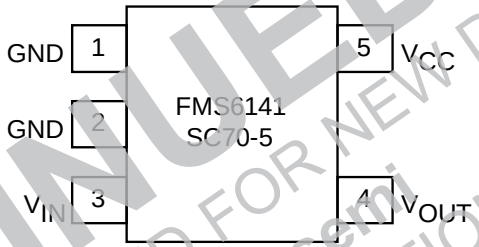


Figure 3. SC70

Pin Definitions

SOIC Pin #	SC70 Pin#	Name	Description
1	3	V_{IN}	Video input
2		N/C	No Connect
3	1, 2	GND	Must Be Connected to Ground
4		N/C	No Connect
5		N/C	No Connect
6		N/C	No Connect
7	5	V_{CC}	+5V Supply, Do Not Float
8	4	V_{OUT}	Filtered Video Output

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC} +0.3	V
I_{OUT}	Output Current, Do Not Exceed		50	mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	-40		85	°C
V_{CC}	V_{CC} Range	4.75	5.00	5.25	V

ESD Information

Symbol	Parameter	Value	Unit
ESD	Human Body Model, JESD22-A114	8.0	kV
	Charged Device Model, JESD22-C101	1.5	kV

Reliability Information

Symbol	Parameter		Min.	Typ.	Max.	Unit
T_J	Junction Temperature				+150	°C
T_{STG}	Storage Temperature Range		-65		+150	°C
T_L	Lead Temperature (Soldering, 10 s)				300	°C
Θ_{JA}	Thermal Resistance (JEDEC Standard Multi-Layer Test Boards, Still Air)	SOIC-8		115		°C/W
		SC70-5		332		°C/W

DC Specifications

T_A = 25°C, V_{CC} = 5.0 V, R_S = 37.5 Ω; input is AC coupled with 0.1 µF; output is AC coupled with 220 µF into a 150 Ω load; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current[1]	No Load		7	12	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC-Coupled		1.4		V_{pp}
PSRR	Power Supply Rejection Ratio	DC		40		dB

Note:

1. 100% tested at 25°C

AC Electrical Specifications

T_A = 25°C, V_{CC} = 5.0 V, R_S = 37.5 Ω; input is AC coupled with 0.1 µF; output is AC coupled with 220 µF into a 150 Ω load; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
AV	Channel Gain[2]		5.6	6.0	6.4	dB
f_{1dB}	-1dB Bandwidth[2]		4.0	6.5		MHz
f_C	-3dB Bandwidth			7.7		MHz
f_{SB}	Attenuation (Stopband Reject)	f = 27 MHz		42		dB
dG	Differential Gain			0.4		%
dϕ	Differential Phase			0.4		°
THD	Output Distortion (all channels)	V_{OUT} = 1.8 V_{pp}, 1 MHz		0.4		%
SNR	Signal-to-Noise Ratio	NTC-7 Weighting; 100 kHz to 4.2 MHz		75		dB
t_{pd}	Propagation Delay	Delay from input to output, 4.5 MHz		55		ns

Note:

2. 100% tested at 25°C

Application Information

Input Considerations

The FMS6141 Low-Cost Video Filter provides 6 dB (2X) gain from input to output. The device provides an internal diode clamp to support AC-coupled input signals. In this configuration, a 0.1 µF ceramic capacitor is used to AC couple the input signal. If the input signal does not go below ground, the clamp is inactive; but if the input signal goes below ground, the clamp circuitry sets the bottom of the sync tip (or lowest voltage) to just below ground. The input level set by the clamp, combined with the internal DC offset, keeps the output signal within an acceptable range. This clamp feature also allows the FMS6141's input to be directly driven (DC-coupled) by a ground referenced DAC output. Figure 4 shows typical DC voltage levels for the input and output signals when driven by a DC-coupled DAC output or an AC-coupled and clamped Y, CV signal.

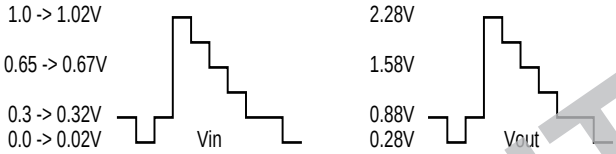


Figure 4. Typical DC Voltage Levels

Output Considerations

The FMS6141 outputs will be DC offset from the input by 150 mv therefore V_{OUT} = 2*V_{IN} DC+150 mv. This offset is required to obtain optimal performance from the output driver and is held at the minimum value in order to decrease the standing DC current into the load. Since the FMS6141 has a 2x (6 dB) gain, the output is typically connected via a 75 Ω series back-matching resistor followed by the 75 Ω video cable. Because of the inherent divide by two of this configuration, the blanking level at the load of the video signal is always less then 1 V. When AC-coupling the output ensure that the coupling capacitor of choice will pass the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. In order to obtain the highest quality output video signal the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the FMS6141 output driver. Recommend distance from device pin to place series termination resistor should be no greater than 0.1 inches.

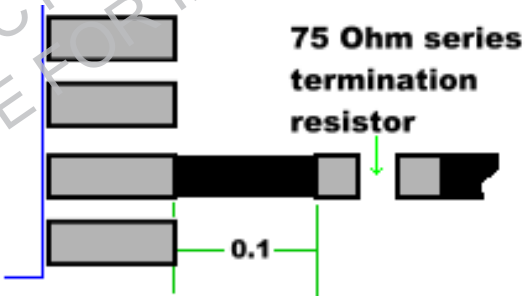


Figure 5. Distance from Device Pin to Series Termination Resistor

I/O Configurations

Figure 6 shows a typical AC-coupled input configuration for driving the filter/driver. Using this configuration, a 0.1 µF ceramic capacitor is used to AC couple the input signal. The coupling capacitor and the input termination resistor at the input of the filter/driver should be placed close to the input pin for optimal signal integrity.

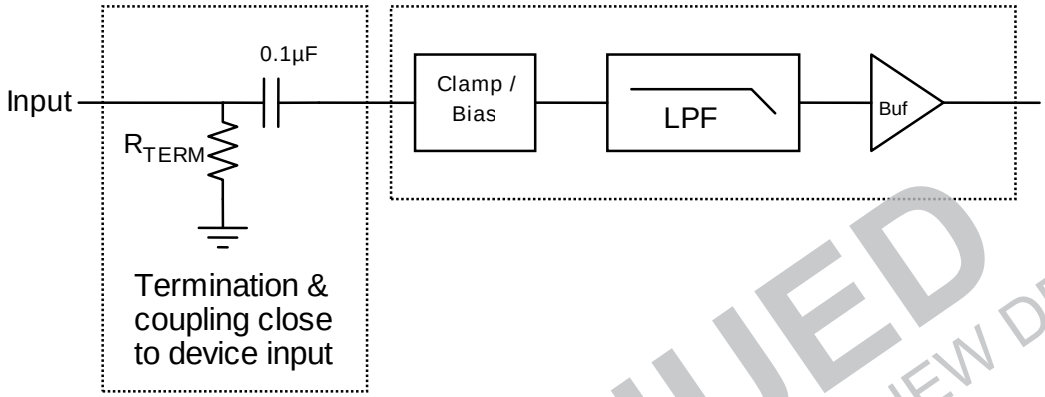


Figure 6. Typical Input Configuration

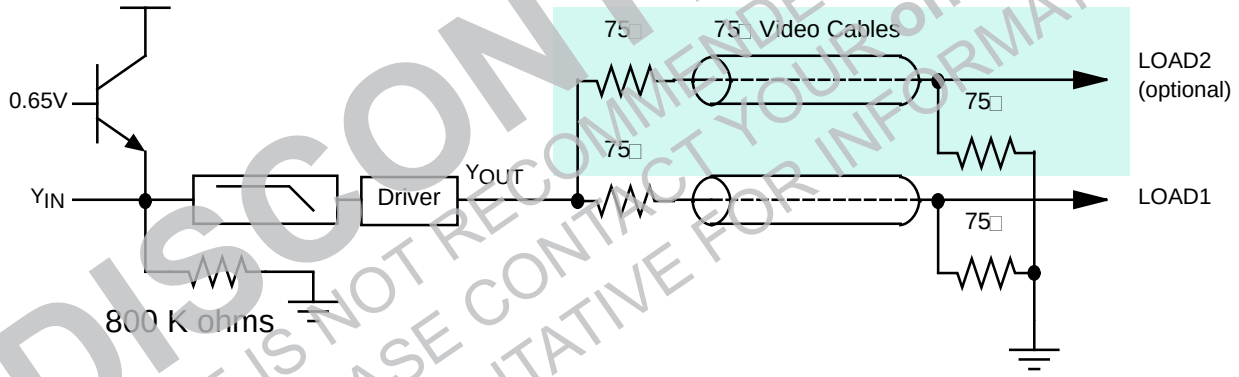


Figure 7. Conceptual Illustration — Input Clamp Circuit and Output Driver Connected to Drive Single or Dual Video Loads

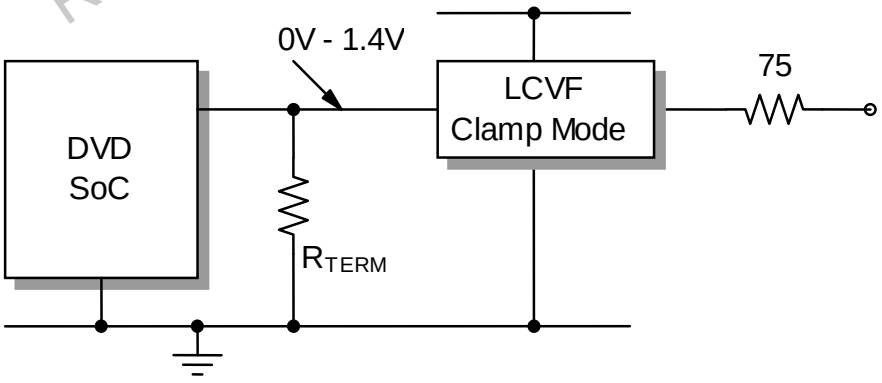


Figure 8. DC-Coupled Input and DC-Coupled Output

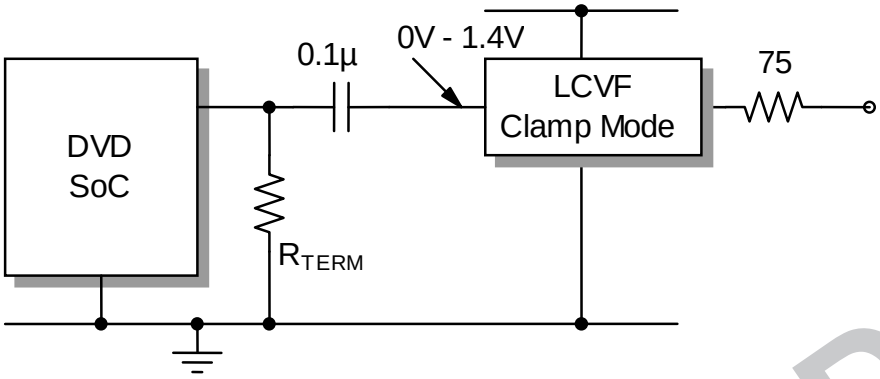


Figure 9. AC-Coupled Input and DC-Coupled Output

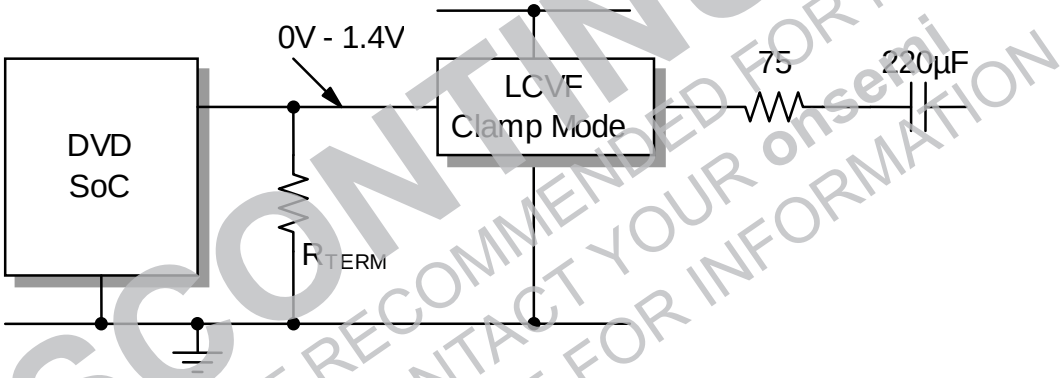


Figure 10. DC-Coupled Input and AC-Coupled Output

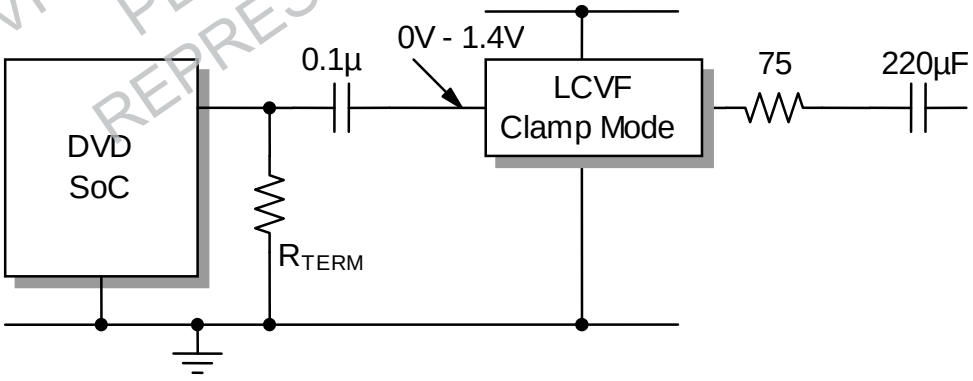


Figure 11. AC-Coupled Input and AC-Coupled Output

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. ON Semiconductor offers a demonstration board for the FMS6141 to guide layout and aid device evaluation. The demo board is a four-layer board with full power and ground planes. Following this layout configuration provides optimum performance and thermal characteristics for the device. For the best results, follow the steps and recommended routing rules listed below.

Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces should run on top of the ground plane at all times.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10 µF and 0.1 µF ceramic power supply bypass capacitors.
- Place the 0.1 µF capacitor within 0.1 inches of the device power pin.
- Place the 10 µF capacitor within 0.75 inches of the device power pin.
- For multilayer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body by at least 0.5 inches on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players are at +70°C; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) and below (bottom plane) each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70 µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques can provide a first-order approximation.

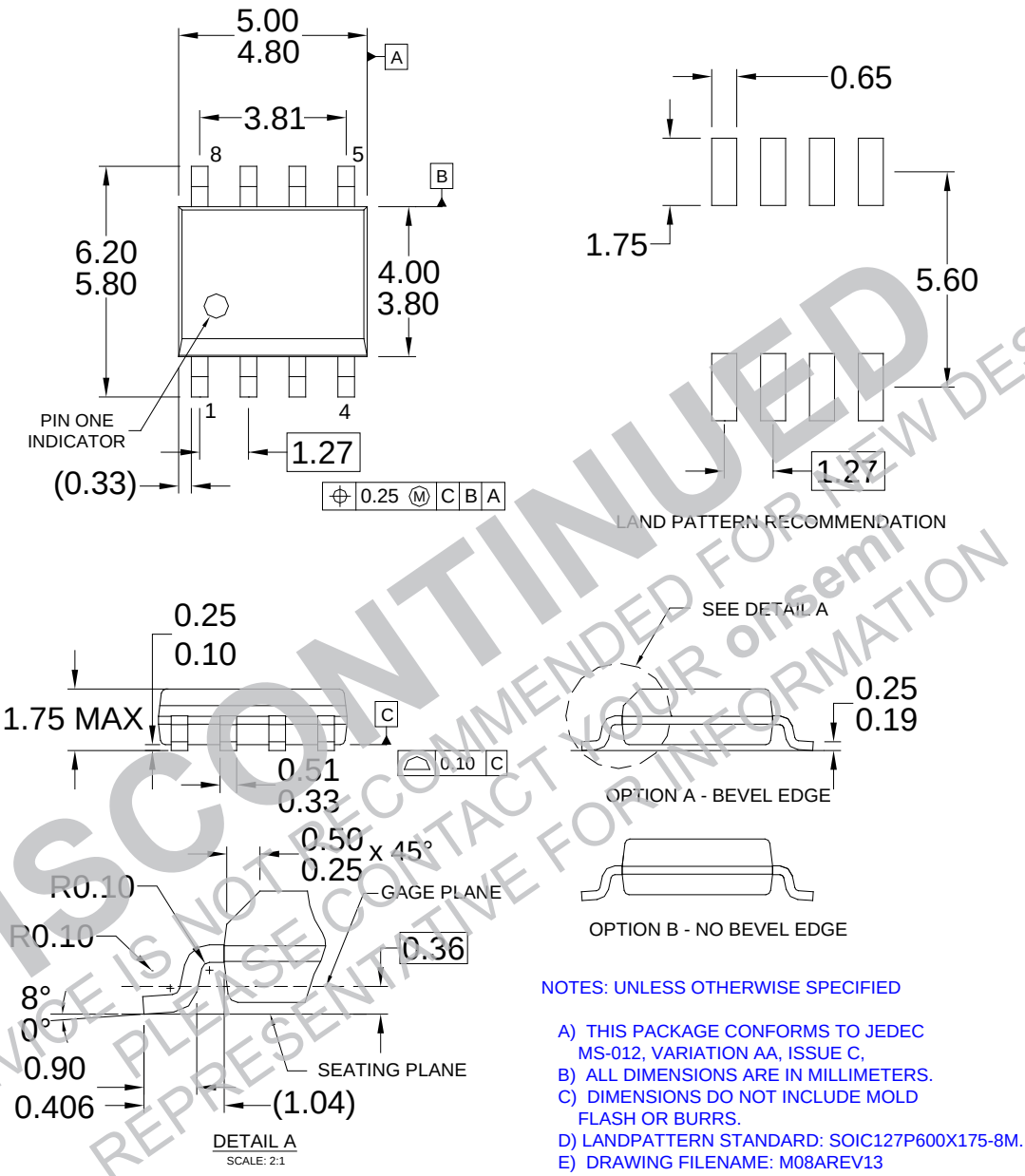
Power Dissipation

Consider the FMS6141's output drive configuration when calculating overall power dissipation. Care must be taken not to exceed the maximum die junction temperature. The following example can be used to calculate the FMS6141's power dissipation and internal temperature rise.

$T_J = T_A + P_{CHANNEL}\ \Theta_{JA}$
where $P_{CHANNEL} = V_{CC} \bullet I_{CH} + (V_O^2/R_L)$
$V_O = 2V_{IN} + 0.280V$
$I_{CH} = I_{CC} + (V_O/R_L)$
V_{IN} = RMS value of input signal
I_{CC} = 7mA
V_S = 5V
R_L = channel load resistance

The FMS6141 is specified to operate with output currents typically less than 50 mA, which is more than sufficient for a dual (75 Ω) video load. The internal amplifiers of the FMS6141 are current limited to a maximum of 100 mA and can withstand a brief-duration short-circuit condition, but this capability is not guaranteed.

Physical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M.
E) DRAWING FILENAME: M08AREV13

Figure 12. SOIC-8 Package

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact an ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor's worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.

Physical Dimensions (Continued)

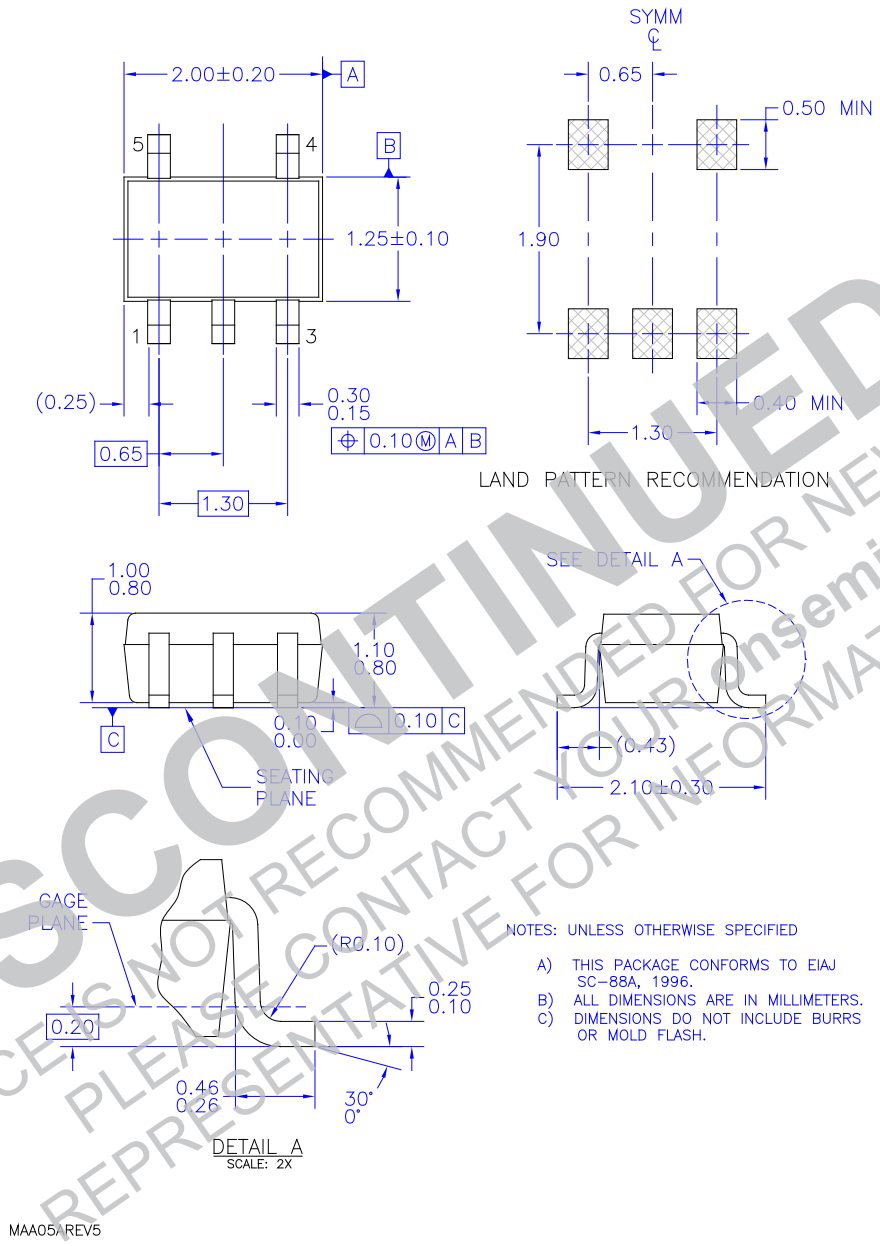


Figure 13. SC70-5 Package

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