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June 2013

FLS0116 MOSFET Integrated Smart LED Lamp Driver IC with PFC Function

Features

- Built-in MOSFET(1 A / 550 V)
- Digitally Implemented Active-PFC Function
- No Additional Circuit for Achieving High PF
- Application Input Range: 80 V_{AC} ~ 308 V_{AC}
- Built-In HV Supplying Circuit: Self Biasing
- AOCP Function with Auto-Restart Mode
- Built-In Over-Temperature Protection (CTP)
- Cycle-by-Cycle Current Limit
- Current Sense Pin Open Prot don
- Low Operating Current: 0.85 A (Typi I)
- Under-Voltage Lock
 Win 5
 Hystrogis
- Programmable Osc ation Frequency
- Programm^r ... _ED \\ \text{\tirr}\text{\ti}\text{\texi\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\text{\text{\text{\texi}\text{\text{\text{\text{\text{\texi}\text{\text{\text{\text{\texicr{\texictex{\texit{\text{\texi}\text{\text{\texi}\text{\text{\te
- Analog D. min ncue.
- Soft-S 't Function
- se ern veference: ±3%

A lictions

- LED Lamp for Decorative Lighting
- LFD Lamp for Low-Power Lighting Fixture

Description

The FLS011 LED mp from is a simple IC with integrater Mc FET of rPC function. The special "adopted nital techn que automatically detects input volution ion at sends a internal reference signal active power factor. When AC input is applied to the PFC function is a tematically enabled. When Description in a tematically enabled is automatically disabled. The FLS0116 ones not need a bulk (electronal) capacito for supply fail stability, which significantly improves LED lamp life.

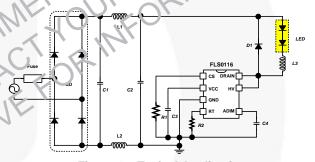


Figure 1. Typical Application

Ordering Information

Part Number Operating Temperature Range		Package	Packing Method	
FLS0116MX	-40°C to +125°C	7-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150-inch, Narrow Body	Tape & Reel	

Block Diagram

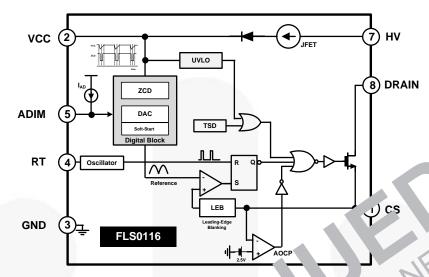


Figure 2. Block [ram

Pin Configuration

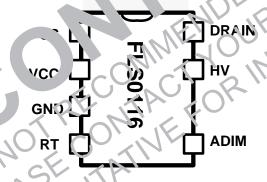


Figure 3. Pin Configuration

Pin Definitions

Pin#	Name	Description			
1	CS	Current Sense . Limits output current, depending on the sensing resistor voltage. The CS pin is also used to set the LED current regulation.			
2	VCC	C. Supply pin for stable IC operation; ZCD signal detection used for accurate PFC function			
3	GND GROUND. Ground for the IC				
4	RT	RT. Programmable operating frequency using an external resistor; the IC has pre-fixed frequency when this pin is open or floating.			
5	Analog Dimming. Connect to the internal current source. Use to change the output current source and the output current source and the output current source and the output current source. Use to change the output current source and the output curr				
7	HV	High Voltage. Connect to the high-voltage line and supply current to the IC.			
8	DRAIN	DRAIN. The drain pin of internal MOSFET			

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pa	rameter	Min.	Max.	Unit
V _{CC}	IC Supply Voltage			20	V
HV	High Voltage Sensing			550	V
DRAIN	Internal Drain Voltage			550	V
V_{ADIM}	Analog Dimming			5	V
V_{RT}	RT Pin Voltage			5	V
V _{CS}	Allowable Current Sensing Detection	n Voltage	- 1		V
T _A	Operating Ambient Temperature Ra	inge	-40	25	°C
TJ	Operating Junction Temperature		-40	+150	°C
T _{STG}	Storage Temperature Range		05	+150	°C
θЈΑ	Thermal Resistance Junction-Air ^(1,2)		17	135	°C/W
P _D	Power Dissipation		2	660	mW
ESD	Electrostatic Discharge Capability	Human Jdy 10d JESL22-A114 Ch y Devic 10cJ, JES 22?-C101	Sel	2000 1000	V

Notes

- 1. Thermal resistance test board. Size: 76 m x 14.3 mi x 1.6 min (150P); JEDEC standard: JESD51-2, JESD51-3.
- Assume no ambient airflow

Electrical Characteristics

Typical values are at T_A = +25°C. Specifications to -40°C ~ 125°C are guaranteed by design based on final characterization results.

Symbol	Parameter Condition		Min.	Тур.	Max.	Unit
V _{CC} Bias Se	ection					
Vcc	V _{CC} Regulator Output Voltage	V _{HV} =100 V _{DC}	14.0	15.5	17.0	V
V _{CCST+}	UVLO Positive-Going Threshold	V _{CC} Increasing	12	13	14	V
$V_{\text{CCST-}}$	UVLO Negative-Going Threshold	V _{CC} Decreasing	7	8	9	V
V_{CCHYS}	UVLO Hysteresis		4	5	6	V
I_{HV}	HV Pin Current	V _{HV} =100 V _{DC} , RT=Open		0.85	1.20	mA
I _{ST}	Startup Current			1	50	μΑ
Switching 9	Section	_				25
		R _T =5.95 kΩ	30r	250	300	kHz
fosc	Operating Frequency	R _T =87 kΩ	'n	20	24	kHz
	7.	R _T Open		·15.0	49.5	kHz
t _{MIN}	Minimum On Time ⁽³⁾		7.0	400		ns
D _{MAX}	Maximum Duty Cycle		7	5.2	\\O	%
t _{LEB}	Leading Edge Blanking Time ⁽³⁾	T OF	0	350		ns
V_{RT}	Voltage Reference of RT Pin	SUL	R	0.577		V
Soft-Start S	Section	10/10/	7.(24		
t _{ss}	Soft-Start T	DC Mode	18	60	72	ms
LSS	Soit-Start 1	AC Mode	, ,	7		Periods
Reference	Ser	14 50,				
V _{CS1}	1007	DC Mode	0.354	0.365	0.376	.,
V	Internal Reservoltage of CS Pin	AC Mode ⁽³⁾	0.485	0.500	0.515	- V
rtectic	Se on S S	7				
C SNCL	Over-Vollage Protection on VCC Fin		17.7	18.7	19.7	V
VALUP	Abnormal OCF Level at CS Pio(5)			2.5		V
t _{AOCP}	Abnormal Detection Time(3)			70		ns
TTSDL	Thermal Shutdown Threshold ⁽³⁾		140	150	100	°C
T _{TSDHY}	Thermal Shutdown Threshold Hysteresis (3)			50	7	°C
Dimming S	ection				- /:	
V _{ADIM(ST+)}	Analog Dimming Positive Going Threshold ⁽³⁾		3.15	3.50	3.85	V
V _{ADIM(ST-)}	Analog Dimming Negative Going Threshold ⁽³⁾			0.50	0.75	V
I _{AD}	Internal Current Source for ADIM Pin		9	12	15	μA

Continued on the following page...

Electrical Characteristics (Continued)

Typical values are at T_A = +25°C. Specifications to -40°C ~ 125°C are guaranteed by design based on final characterization results.

Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
MOSFET Se	ection					
BV _{DSS}	Breakdown Voltage	V _{CC} =0 V, I _D =250 μA	550			V
I _{LKMOS}	Internal MOSFET Leakage Current	V _{DS} =550 V _{DC} , V _{GS} =0 V			250	μΑ
R _{ON(ON)}	Drain-Source On Resistance ⁽³⁾	V _{GS} =10 V, V _{DGS} =0 V, T _C =25°C		7.3	10.0	Ω
C _{ISS}	Input Capacitance ⁽³⁾	V _{GS} =0 V,V _{DS} =25 V, f=1 MHz		135		pF
Coss	Output Capacitance ⁽³⁾	V _{GS} =0 V,V _{DS} =25 V, f=1 MHz				pF
C _{RSS}	Reverse Transfer Capacitance ⁽³⁾	V _{GS} =0 V,V _{DS} =25 V, f=1 MHz				ρĒ
t _{d(ON)}	Turn-On Delay ⁽³⁾	V _{DD} =350 V, I _D =1 A		10		ns
t _r	Rise Time ⁽³⁾	V _{DD} =350 V, I _D =1 A		114	110	ns
t _{d(OFF)}	Turn-Off Delay ⁽³⁾	V _{DD} =350 V, I _D =1 A		14.9	110	ns
t _f	Fall Time ⁽³⁾	V _{DD} =350 V, I _D =1 A		36.8		ns

Note:

3. These parameters, although guaranteed, are not 100% to 'ed production.

Functional Description

The FLS0116 is a basic PWM controller for buck converter topology in Continuous Conduction Mode (CCM) with an intelligent PFC function that uses a digital control algorithm. An internal self-biasing circuit uses the high-voltage switching device. The IC does not need an auxiliary powering path to the VCC pin typical in flyback control ICs or PSR product family.

When the input voltage applied to the HV pin is within operating range (25 V to 500 V), the FLS0116 maintains a 15.5 V DC voltage at the VCC pin for stable operation. The UVLO block functions such that when the $V_{\rm CC}$ voltage rises higher than $V_{\rm CCST+},$ the internal UVLO block releases and starts operation. Otherwise, the $V_{\rm CC}$ goes down to the $V_{\rm CCST-}$ and IC operation stops. Normally, the hysteresis function provides stable operation even if the input voltage is operating under very noisy or unstable circumstances.

The FLS0116 has a "smart" internal digital block for determining input condition: AC or DC. When an AC source with 50 Hz or 60 Hz is applied to the IC, the IC automatically changes its internal reference signal, which is similar to input signal, for creating high power factor. When a DC source connects to the IC, th internal reference immediately changes to DC.

Soft-Start Function

The FLS0116 has an internal soft start now of reduce inrush current at startup when the C starts operation following an internal quence the internal reference slowly increase a re-det mined fixed time. After this transier period, the mal reference goes to a steady-stallevel. In this time, the IC continually trier a mid pure in immation from the VCC pin. If the IC received in a mation from the VCC pin.

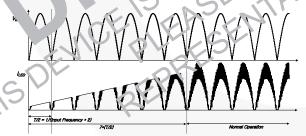


Figure 4. Soft-Start Function in AC Input Mode

Internal PFC Function: How to Achieve High Power Factor

The FLS0116 has a simple, "smart", internal PFC function that does not require additional pins for detecting input phase information or an electrolytic capacitor for supply voltage stabilization. For achieving high PF, the FLS0116 does not use the rectification capacitor after the bridge diode. This is important because the IC instead uses fluctuation in the signal on the VCC pin. Basically, the VCC pin, which is supplies

power for the IC, has voltage ripple as well as the rectification voltage after bridge, changing voltage level according to the V_{CC} capacitor value. Using this kind of voltage fluctuation on the VCC pin, the IC can detect the time reference and create the internal ZCD signal.

For precise and reliable internal reference for input voltage signal, the FLS0116 uses a digital technique (sigma/delta modulation) and creates a new internal signal (DAC_OUT) that has the same phase as the input voltage, as shown in Figure 5. This signal enters the final comparator and is compared with current information from the sensing resistor

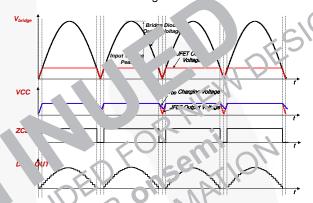


Figure 5 Internal PFC Function

Self-Bidsing Function

The celf-biasing function, using an HV device, can supply enough operating current to the IC and guarantee similar startup time across the whole input voltage range (80 V~308 V_{AC}). However, self-biasing has a weakness in high-voltage condition. Normally, he HV device acts as constant current source, so the internal HV device has power loss when high input voltage connects to the HV pin. This power loss is proportional to input voltage. To reduce this power loss, one of the possible solutions is an additional resistor between the input voltage source and the HV pin, as shown in Figure 6.

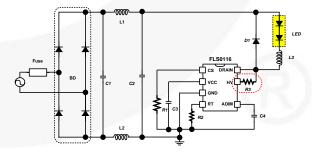


Figure 6. High-Voltage Application

Dimming Function

The FLS0116 uses the ADIM pin for analog or 0 V to 10 V dimming by using a resistive divider. The peak voltage of internal reference, which is DAC_OUT signal in Figure 5, is changed by the V_{ADIM} level, as shown in Figure 7, and has different peak level according to the operating mode.

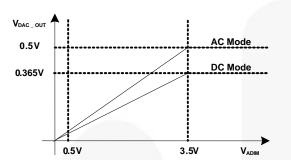


Figure 7. VADIM vs. VDAC_OUT(peak)

Inductor Design

The fixed internal duty ratio range is below 50%, or around 400 ns, from a timing point of view. The range is dependent on the input voltage and number of LEP, its string.

Minimum duty is calculated as:

$$D_{\min} = \frac{n \cdot V_f}{\eta \cdot V_{in(\max)}} \tag{1}$$

where:

 η = efficiency of stem;

 $V_{IN(max)}$ = maxim int voltac

 $V_f = \text{for and drop } V \text{ and in LED; and}$

n LE in series connection.

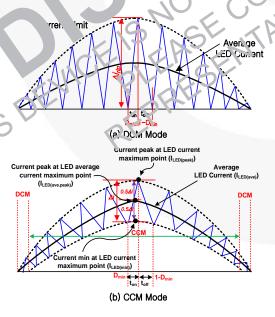


Figure 8. DCM and CCM Operation

In DCM Mode, inductance is:

$$L_{m} = \frac{n \cdot V_{f} \cdot (1 - D_{\min})}{f_{s} \cdot \Delta i_{rin}} [H]$$
 (2)

If the peak current is fixed at 350 mApk, the formula for the peak current is:

$$I_{LED(ave.peak)} = \Delta i_{con} + \frac{\Delta i_{rip}}{2} \quad [A]$$

In FL7701, the LED RMS current determines the inductance parameter. To drive for CCM Mode, define LED RMS current first, as:

$$I_{LED(rms)} = \frac{I_{LED(ave.peak)}}{\sqrt{2}} \quad [A]$$
 (4)

Substituting Equation (2) for 'qu' on (4) the inductance of inductor in the med.

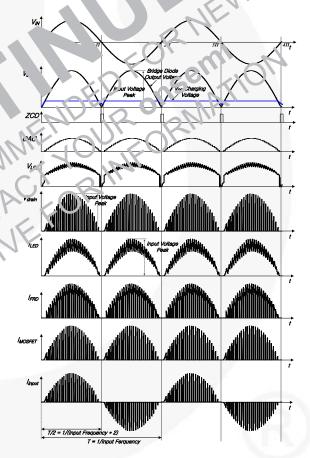


Figure 9. Typical Performance Characteristics

Example Application Circuits

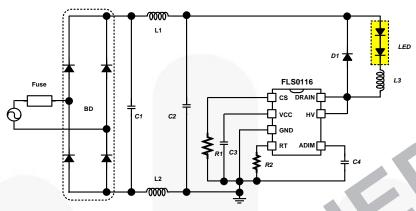
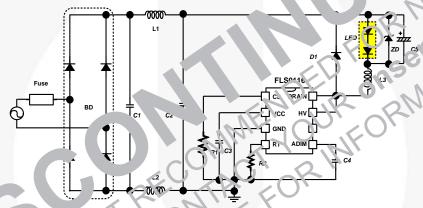


Figure 10. Application Circuit without Electrolytic pa or



rigure 11. Application Circuit with Electrolytic Capacitor

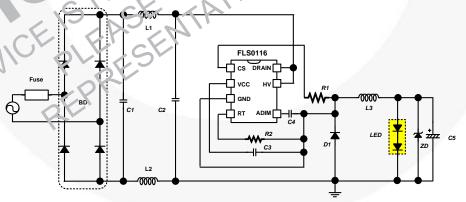
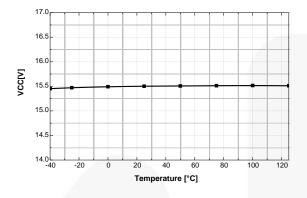


Figure 12. Application Circuit of High-Side Operation with Electrolytic Capacitor

Typical Characteristics



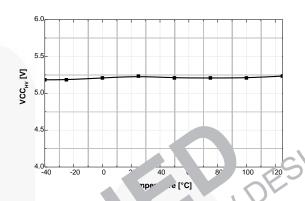
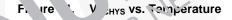
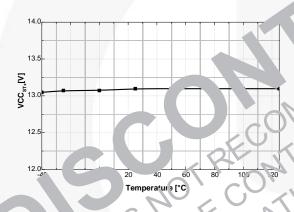
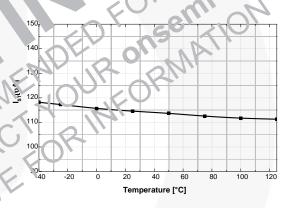


Figure 13. V_{CC} vs. Temperature

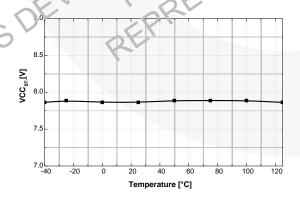






gure 15 V_{CCST}, vs. 7emperature

Figure 16. I_{ST} vs. Temperature



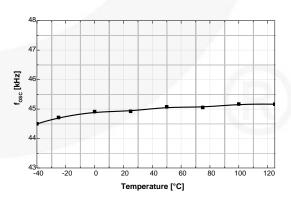
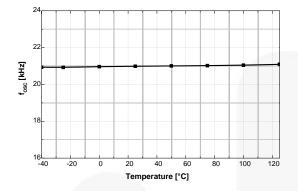


Figure 17. V_{CCST-} vs. Temperature

Figure 18. fosc vs. Temperature (RT=Open)

Typical Characteristics



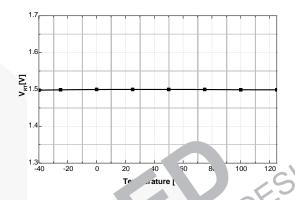
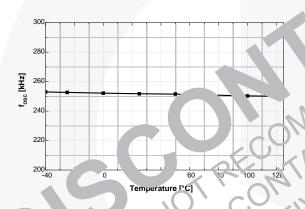
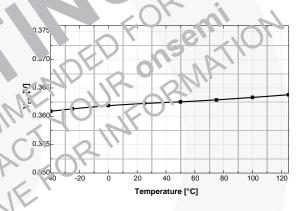


Figure 19. f_{OSC} vs. Temperature (RT=87k Ω)

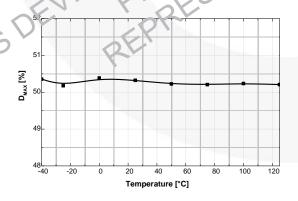
Fig. 20. 'RT . femperature





Figur 21. fosc vs. Temperature (RT=5.95)(2)

Figure 22. V_{CS} vs. Temperature



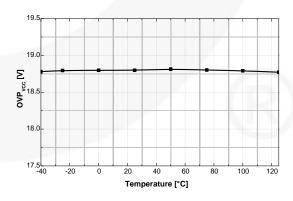
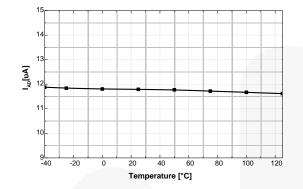


Figure 23. D_{MAX} vs. Temperature

Figure 24. OVP_{VCC} vs. Temperature

Typical Characteristics



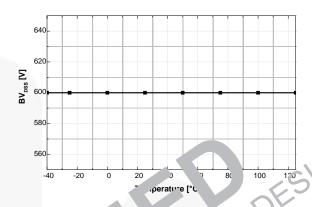
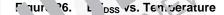


Figure 25. I_{AD} vs. Temperature



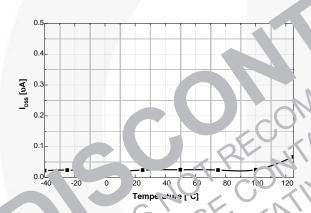
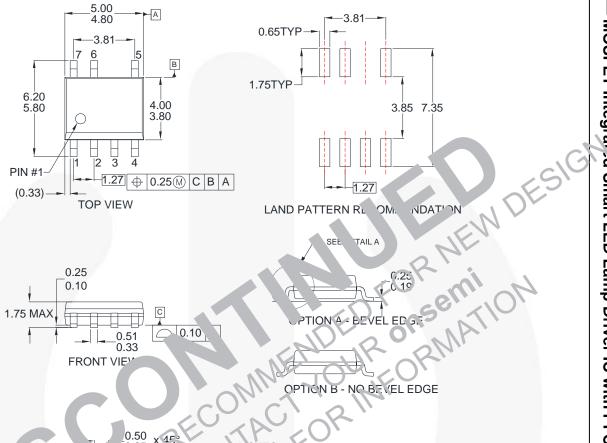
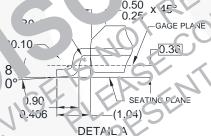


Figure 27. Jose vs. Temporature

Physical Dimensions





NOTES:

- A) THIS PACKAGE DOES NOT FULLY CONFORMS TO JEDEC MS-012 VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) DRAWING FILENAME: M07Brev3

Figure 28. 7-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150-Inch Narrow Body

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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