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FAIRCHILD SEMICONDUCTOR®

December 2009

FIN324C

24-Bit Ultra-Low Power Serializer / Deserializer Supporting Single and Dual Displays

Features

Ultra-Low Operating Power: ~4mA at 5.44MHz

Supports Dual-Display Implementations with RGB or Microcontroller Interface

No External Timing Reference Needed

SPI Mode Support

Single Device Operates as a Serializer or Deserializer

Direct Support for Motorola®-Style R/W Microcontroller Interface

Direct Support for Intel®-Style /WE, /RE Microcontroller Interface

15MHz Maximum Strobe Frequency

Utilizes Fairchild's Proprietary CTL Serial I/O Technology

Available in BGA and MLP packages

Wide Parallel Supply Voltage Range: 1.60 to 3.0V

Low Power Core Operation: $V_{DDS/A}$=2.5 to 3.0V

Voltage Translation Capability Across Pair with No External Components

High ESD Protection: >15kV IEC 61000

Power-Saving Burst-Mode Operation

Applications

Single or Dual 16/18-Bit RGB Cell Phone Displays

- Single or Dual 16/18-Bit Cell Phone Displays with Microcontroller Interface
- Single or Dual Mobile Display at QVGA or HVGA Resolution

Description

The FIN324C is a 24-bit serializer / deserializer with dual strobe inputs. The device can be configured as a master or slave device through the master/slave select pin (M/S). This allows for the same device to be used as either a serializer or deserializer, minimizing component types in the system. The dual strobe inputs allow implementation of dual-display systems with a single pair of µSerDes. The FIN324C can accommodate RGB, microcontroller, or SPI mode interfaces. Read and write transactions are supported when operating with a microcontroller interface for one or both displays. Unlike other SerDes solutions, no external timing reference is required for operation.

The FIN324C is designed for ultra-low power operation. Reset (/RES) and standby (/STBY) signals put the device in an ultra-low power state. In standby mode, the outputs of the slave device maintain state, allowing the system to resume operation from the last-known state.

The device utilizes Fairchild's proprietary ultra-low power, low-EMI Current Transfer Logic™ (CTL) technology. The serial interface disables between transactions to minimize EMI at the serial interface and to conserve power. CMOS parallel output buffers have been implemented with slew rate control to adjust for capacitive loading and to minimize EMI.

Related Application Notes

For additional Information, please visit:
http://www.fairchildsemi.com/userdes.

- *AN-5058 µSerDes™ Frequently Asked Questions*
- *AN-5061 µSerDes™ Layout Guidelines*
- *AN-6047 FIN324C Reset and Standby*

Ordering Information

Order Number	Operating Temperature Range	Package Description	Eco Status	Packing Method
FIN324CMLX	-30 to 85°C	40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square	Green	Tape & Reel
FIN324CGFX	-30 to 85°C	42-Ball, Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5 x 4.5mm Wide, 0.5mm Ball Pitch	RoHS	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

Typical Application Diagram

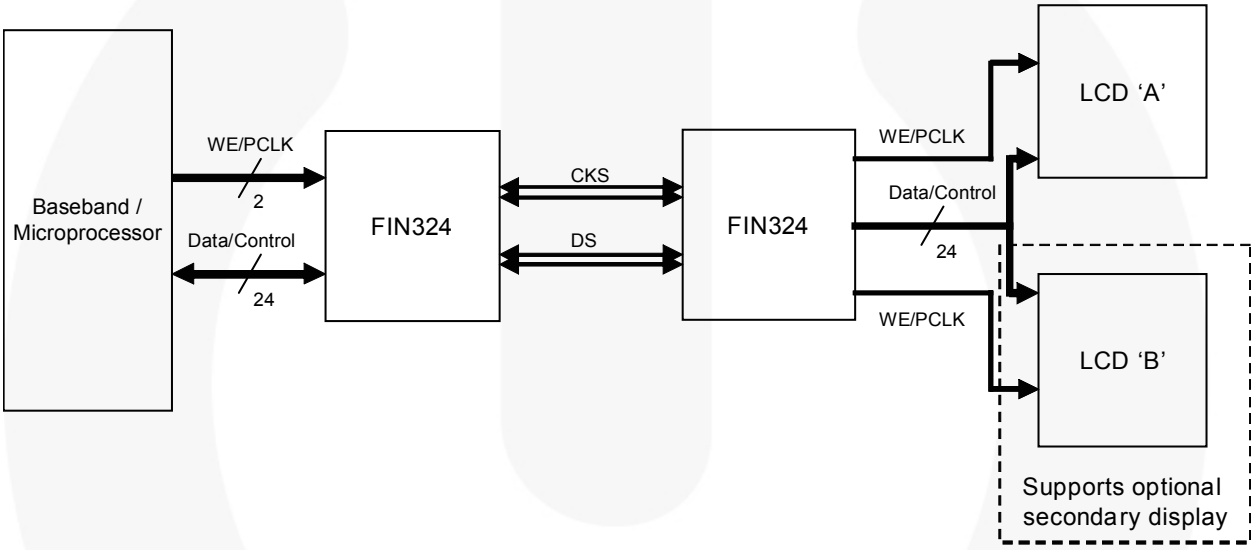


Figure 1. Typical Application Diagram

Pin Definitions

Pin	I/O Type	# Pins	Description of Signals
M/S	CMOS IN	1	Master/Slave Control Input: The master is tied to the processor. The slave is tied to the display(s). M/S=1 MASTER, M/S=0 SLAVE
/RES	CMOS IN	1	Reset and power-down signal /RES=0: Resets and powers down all circuitry /RES=1: Device enabled
/STBY	CMOS IN	1	Master standby signal /STBY=0: Device powered down /STBY=1: Device enabled
SLEW	CMOS IN	1	Slave output slew rate control SLEW=1: Fast edge rate SLEW=0: Slow edge rate
PAR/SPI	CMOS IN	1	Parallel / SPI display interface select PAR/SPI=1: Parallel Interface PAR/SPI=0: SPI Interface using STRB0 and WCLK0
CKSEL	CMOS IN	1	Master clock source select input. CKSEL=1: STRB1 and WCLK1 Active CKSEL=0: STRB0 and WCLK0 Active
DP[17:0]	CMOS I/O	18	Parallel data I/O. I/O direction controlled by M/S pin and R/W internal state. DP[6] SPI mode SCLK signal pin when PAR/SPI=0 (Slave Only) DP[7] SPI mode SDAT signal pin when PAR/SPI=0(Slave Only)
CNTL[5:0]	CMOS I/O	6	Parallel data I/O. I/O direction controlled by M/S pin M/S=1: Inputs M/S=0: Outputs
R/W	CMOS I/O	1	Read / Write input control or output signal. M/S=1: Input M/S=0: Output Functional operation: R/W=1: Read R/W=0: Write
STRB0 STRB1	CMOS IN	2	Word latch or pixel clock input.
WCLK0 WCLK1	CMOS OUT	2	Word latch or pixel clock output.
SCLK SDAT /CS	CMOS I/O	2	SPI mode signal pins. The master SCLK input is shared with CNTL[5] when M/S=1 and PARI/SPI=0. The master SDAT input is shared with CNTL[4] when M/S=1 and PARI/SPI=0. The master /CS input is shared with STRB0 when M/S=1 and PAR/SPI=0. The slave SCLK output is shared with DP[6] and CNTL[5] when M/S=0 and PAR/SPI=0. The slave SDAT output is shared with DP[7] and CNTL[4] when M/S=0 and PAR/SPI=0. The slave /CS output is shared with WCLK0 when M/S=0 and PAR/SPI=0.
CKS+ CKS-	Differential Serial I/O	2	Serial clock differential signal(1)
DS+ DS-	Differential Serial I/O	2	Serial data differential signal(1)
VDDP	Supply	1	Power supply for parallel I/O and internal circuitry.
VDDS	Supply	1	Power supply for serial I/O.
VDDA	Supply	1	Power supply for internal bit clock generator.
GND	Supply	1-3	Ground Pins: BGA - C1 and D2; E3 is for supplier use only and must be tied to ground. MLP - center pad; Pin 12 is for supplier use only and must be tied to ground.

Note:

1. Serial I/O signals are swapped on the slave so system traces do not have to cross between master and slave.

Pin Assignments

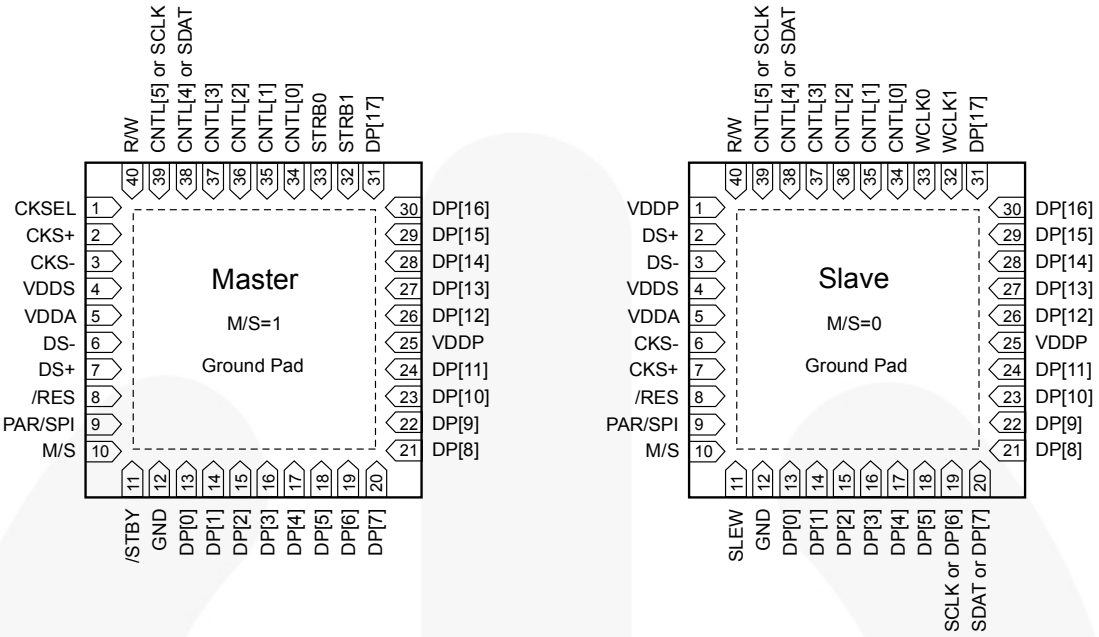
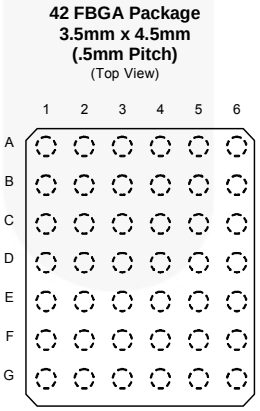


Figure 2. MLP Pin Assignments (40 Pins, 6x6mm, .5mm Pitch, Top View)



Master (M/S=1)

	1	2	3	4	5	6
A	R/W	CNTL[4] or SDAT	CNTL[2]	STROB0	DP[17]	DP[16]
B	CKSEL	CNTL[5] or SCLK	CNTL[3]	STROB1	DP[15]	DP[14]
C	GND	VDDP	CNTL[1]	CNTL[0]	DP[13]	DP[12]
D	CKS+	GND	M/S	DP[11]	DP[9]	DP[10]
E	CKS-	VDDS	GND	DP[2]	DP[7]	DP[8]
F	DS-	VDDA	PAR/SPI	DP[0]	DP[4]	DP[6]
G	DS+	/RES	/STBY	DP[1]	DP[3]	DP[5]

Slave (M/S=0)

	1	2	3	4	5	6
A	R/W	CNTL[4] or SDAT	CNTL[2]	WCLK0	DP[17]	DP[16]
B	VDDP	CNTL[5] or SCLK	CNTL[3]	WCLK1	DP[15]	DP[14]
C	GND	VDDP	CNTL[1]	CNTL[0]	DP[13]	DP[12]
D	DS+	GND	M/S	DP[11]	DP[9]	DP[10]
E	DS-	VDDS	GND	DP[2]	DP[7] or SDAT	DP[8]
F	CKS-	VDDA	PAR/SPI	DP[0]	DP[4]	DP[6] or SCLK
G	CKS+	/RES	SLEW	DP[1]	DP[3]	DP[5]

Figure 3. BGA Pin Assignments

System Control Pins

(M/S) Master / Slave Selection: A given device can be configured as a master or slave device based on the state of the M/S pin.

Table 1. Master/Slave

M/S	Configuration
0	Slave Mode
1	Master Mode

(PAR/SPI) SPI Mode Selection: The PAR/SPI signal configures STRB0(WCLK0) for SPI mode write operation. STRB1(WCLK1) always operates in parallel mode. Control signals CNTL[5:0] all pass in SPI mode. In SPI mode, the SCLK signal is used to strobe the serializer. SPI mode supports SPI writes only.

Table 2. Channel 0 PAR/SPI Configuration

PAR /SPI	M/S=1 MASTER	M/S=0 SLAVE
0	SPI Mode SDAT=CNTL[4] SCLK=CNTL[5] /CS=STRB0	SPI Mode SDAT=DP[7] & CNTL[4] SCLK=DP[6] & CNTL[5] /CS=WCLK0
1	Parallel Mode	Parallel Mode

(CKSEL) Strobe Selection Signal: The CKSEL signal exists only on the master device and determines which strobe signal is active. The active strobe signal is selected by CKSEL and PAR/SPI inputs.

Table 3. PAR/SPI

PAR /SPI	CKSEL	Master Strobe Source	Slave Strobe Source
0	0	CNTL[5]	DP[6] & CNTL[5]
0	1	STRB1	WCLK1
1	0	STRB0	WCLK0
1	1	STRB1	WCLK1

(/RES, /STBY) Reset and Standby Mode Functionality: Reset and standby mode functionality is determined by the state of the /RES and /STBY signals for the master device and the /RES and internal standby-detect signal for the slave device. The /RES control signal has a filter that rejects spurious pulses on /RES.

Table 4. Reset and Standby Modes

/RES	/STBY(2)	Master	Slave
0	X	Reset Mode	Reset Mode
1	0	Standby Mode	Standby Mode(2)
1	1	Operating Mode	Operating Mode

Note:

2. The slave device is put into standby mode through control signals sent from the master device.

Table 5. Reset and Standby Mode States

Pin	Master Reset / Standby	Slave Reset	Slave Standby
DP[17:0]	Disabled	Low	Last Data
CNTL[5:0]	Disabled	Low	Last Data
STRB[0:1] (WCLK[0:1])	Disabled	High	High

(SLEW) Slew Control: The slew control operates only when in slave mode. This signal changes the edge rate of the DP[17:0], CNTL[5:0], R/W, WCLK1, and WCLK0 signals to optimize edge rate for the load being driven. Master read mode outputs have "slow" edge rates. *See the AC Deserializer Specifications table for "slow" and "fast" edge rates.*

Table 6. Slew Rate Control

/STBY (SLEW)	Slave M/S=0
0	"Slow"
1	"Fast"

CMOS I/O Signals

System Control Signals

The system control signals consist of M/S, /RES, /STBY(SLEW), PAR/SPI, and CKSEL. For connectivity flexibility, these signals are over-voltage tolerant to the maximum supply voltage connected to the device. This allows these signals to be tied HIGH to either a V_{DDS} or V_{DDP} supply without static current consumption. These signals are all CMOS inputs and should never be allowed to float.

Parallel I/O Signals

The parallel data port signals consist of the DP[17:0], CNTL[5:0], R/W, and STRB1(0)(WCLK1(0)) signals. These signals have built-in voltage translation, allowing the signals of the master and slave to be connected to different V_{DDP} supply voltages.

Serial I/O Signals

CTL I/O Technology

The serial I/O is implemented using Fairchild's proprietary differential CTL I/O technology. During data transfers, the serial I/O are powered up to a normal operating mode around .5V. Upon completion of a data transfer, the serial I/O goes to a lower power mode around V_{DDS}.

The serial I/O signal traces should not cross between the master and the slave. The pin locations have been designed to eliminate the need to cross traces. *See Table 7, Figure 4, and Figure 5.*

Serial I/O Orientation Logic

Table 7. Serial Pin Orientation

	Master (M/S=1) (Pad/Pin #)				Slave (M/S=0) (Pad/Pin #)			
Package	CKS+	CKS-	DS-	DS+	CKS+	CKS-	DS-	DS+
MLP	2	3	6	7	7	6	3	2
BGA	D1	E1	F1	G1	G1	F1	E1	D1

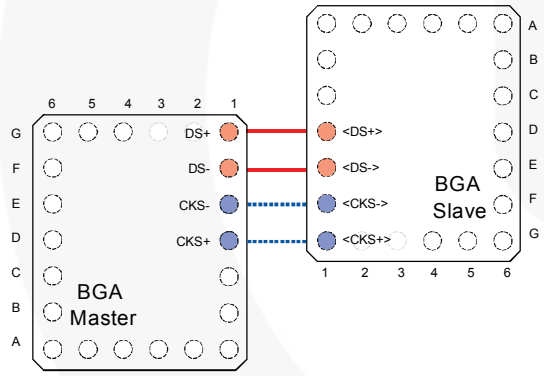


Figure 4. BGA Pair

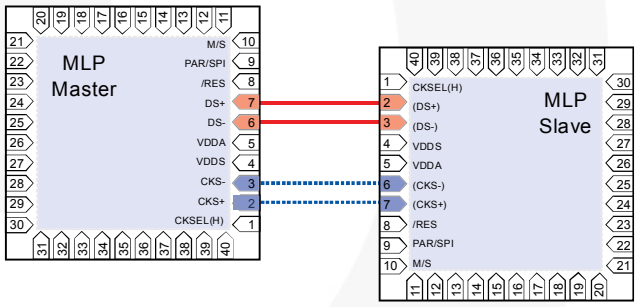


Figure 5. MLP Pair

Master/Slave READ Transactions

Read transactions have two phases: The Read-Control Phase, where CNTL[5:0], R/W, CKSEL are transmitted to the deserializer; and the Read-Data Phase, where the DP[17:0] signals of the slave are read and transmitted back to the master device. The slave device generates its own strobe signal for latching in the data. Slave data must be valid prior to the WCLKn signal going HIGH.

Master Serializer Operation (Read Control Phase)
When the R/W signal is asserted HIGH and the STROBE signal transitions LOW, the Read-Control Phase of the read cycle is initiated. The R/W signal must not transition until the READ cycle completes. For a READ transaction, only eight control signals are captured. The 18 DP bits are ignored during the READ operation. The following sequence must occur for data to be serialized properly:

1. CPU selects input strobe source (CKSEL=0 or 1).
2. CPU sends signals (R/W=1, CKSEL, CNTL[5:0]).
3. CPU sends LOW STROBE signal.

Slave Deserializer Operation (Read-Control Phase)
1. Captures data from serial transfer.
2. Internally decodes that this is a READ transaction.
3. Outputs control signals and prepares DP pins to accept data.
4. Outputs falling edge of WCLK pulse.

Slave Serializer Read Operation (Read-Data Phase)
The slave serializer is enabled on the tail end of the Read-Control Phase of operation. The operation of the serializer is identical to the master serialization except that the strobe signal is generated internally and only the data bits DP[17:0] are captured.

1. Display device outputs data onto DP bus on falling edge of WCLK.
2. Captures parallel data on generated rising edge of WCLK signal.
3. Serializes data stream.

Master Deserializer Read Operation (Read-Data Phase):
1. Receives valid serial stream.
2. Outputs data DP[17:0].
3. CPU asserts rising edge of strobe signal to capture data.

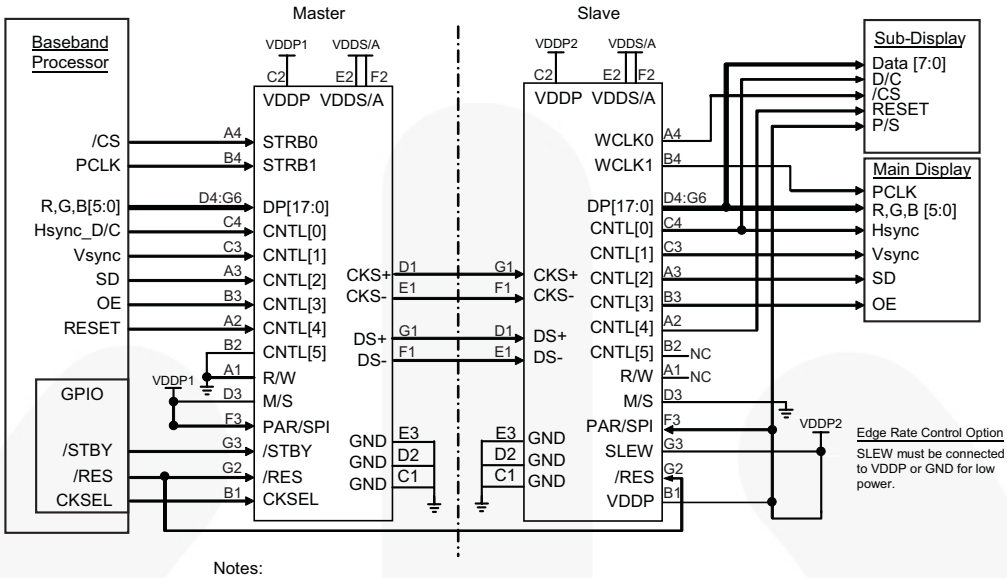
SPI WRITE transaction

SPI mode is activated by asserting the PAR/SPI signal low on both the master and slave device. A SPI write is only performed when CKSEL=0. During a SPI transaction, SCLK must be connected to CNTL[5] and is the strobe source for serialization. SDAT is on CNTL[4] and all of the remaining control signals and STRB0 are serialized. STRB0 should be connected to the SPI mode chip select.

On the rising edge of SCLK, all eight control signals (CNTL[5:0], R/W, CKSEL) are captured and serialized. The data signals are not sent. The deserializer captures the serial stream and outputs it to the parallel port.

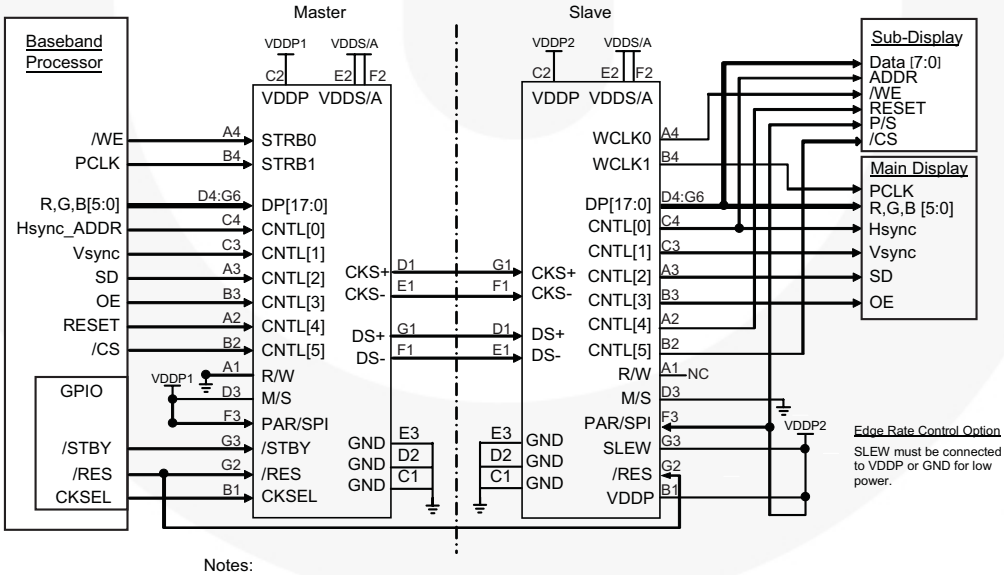
As shown in Table 2, SDAT and SCLK are output on multiple pins. The DP[7] and DP[6] connections can be used for displays with dual-mode operation and the data pins are multiplexed with the SPI signals. CNTL[5] and CNTL[4] signals can be used when the signals are not multiplexed.

Applications Diagrams



Notes:
1. Write-only Interface.
2. Unused slave output pin must be NC (No Connection).
3. /CS used to strobe sub-display data.
4. PCLK used for RGB mode.
5. Pin numbers for BGA package.

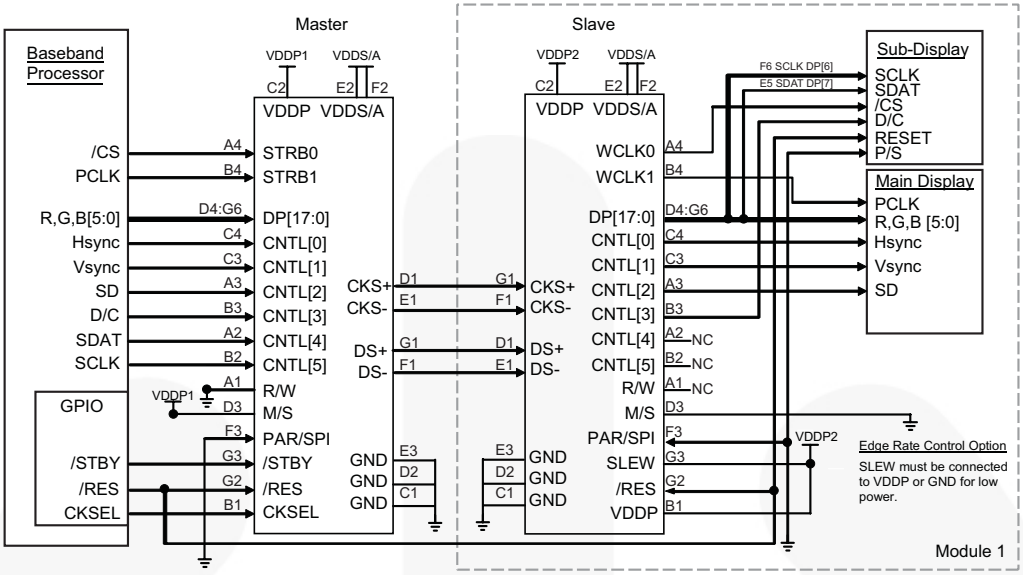
Figure 6. Dual Display with Parallel RGB Main Display and 6800-Style Microcontroller Sub-Display



Notes:
1. Write-only Interface.
2. Unused slave output pin must be NC (No Connection).
3. /WE used to strobe sub-display data.
4. PCLK used for RGB mode.
5. Pin numbers for BGA package.

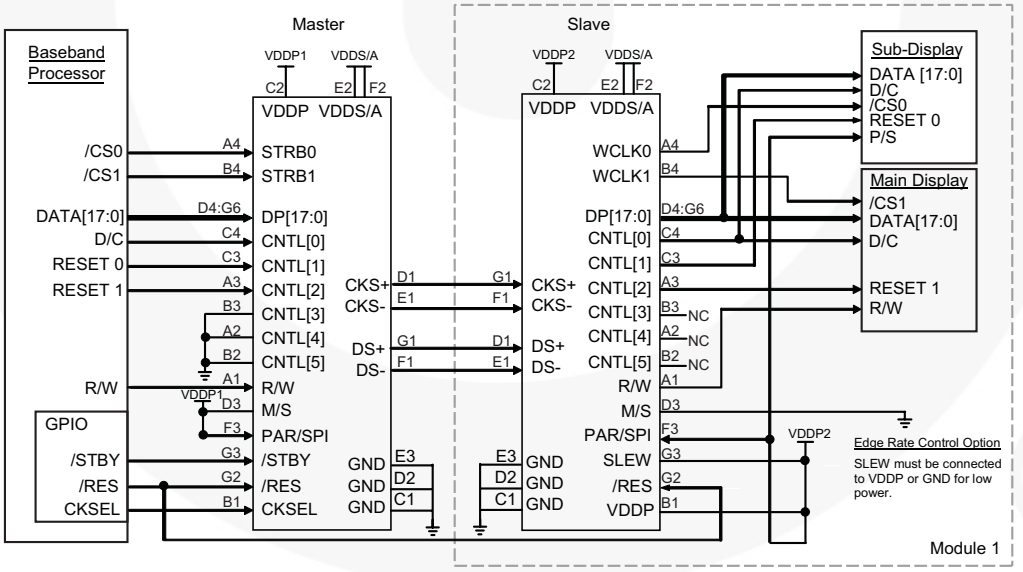
Figure 7. Dual Display with Parallel RGB Main Display and x86-Style Microcontroller Sub-Display

Application Diagrams (Continued)



Notes:
1. Write-only interface (R/W hardwired LOW).
2. SPI sub-display interface PAR/SPI=LOW for both master and slave.
3. SCLK connected to CNTL[5]; SDAT connected to CNTL[4].
4. Shared data pin SDAT; SCLK connections on sub-display.
5. Unused slave output pin must be NC (No Connection).
6. Pin numbers for BGA package.

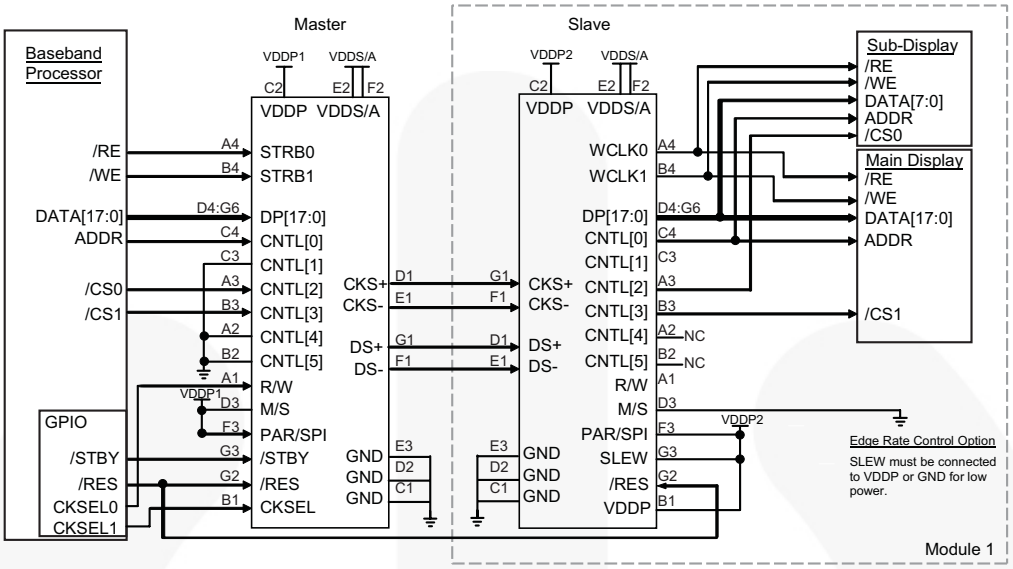
Figure 8. Dual Display with RGB Main Display and SPI Sub-Display Interface



Notes:
1. R/W interface. R/W signal connected to baseband microprocessor.
2. Unused slave output pin must be NC (No Connection).
3. PAR/SPI connected HIGH to indicate parallel operation.
4. Pin numbers for BGA package.

Figure 9. R/W Dual Display with Parallel Microcontroller Main Display and Sub-Display

Application Diagrams (Continued)



Notes:
1. Dual display R/W Intel® interface.
2. Unused slave output pin must be NC (No Connection).
3. GPIO signal used to select READ or WRITE functionality. Connected to CKSEL and R/W.
4. Displays selected via the chip selects.
5. Pin numbers for BGA package.

Figure 10. Dual R/W x86-Style Microcontroller Display Interface

Additional Application Information

Flex Cabling: The serial I/O information is transmitted at a high serial rate. Care must be taken implementing this serial I/O flex cable. The following best practices should be used when developing the flex cabling or Flex PCB.

Keep all four differential Serial Wires the same length.

Do not allow noisy signals over or near differential serial wires.
Example: No CMOS traces over differential serial wires.

Use only one ground plane or wire over the differential serial wires. Do not run ground over top and bottom.

Design goal of 100-ohms differential characteristic impedance.

Do not place test points on differential serial wires.

Use differential serial wires a minimum of 2cm away from the antenna.

Visit Fairchild's website at http://www.fairchildsemi.com/products/interface/userdes.html, contact your sales rep, or contact Fairchild directly at interface@fairchildsemi.com for applications notes or flex guidelines.

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	Supply Voltage		-0.5	+3.6	V
	All Input/Output Voltage		-0.5	V_{DDP}+0.5	V
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Maximum Junction Temperature			+150	°C
T_L	Lead Temperature (Soldering, 4 Seconds)			+260	°C
ESD	IEC 61000 Board Level			15	kV
	Human Body Model, JESD22-A114	All Pins		7.5	kV
		Serial I/0, /RES, PAR/SPI to GND		14.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{DDA}, V_{DDS}[3]	Supply Voltage	2.5	3.0	V
V_{DDP}	Supply Voltage	1.6	$V_{DDA/S}$	V
T_A	Operating Temperature	-30	+85	°C

Note:

3. V_{DDA} and V_{DDS} supplies must be hardwired together to the same power supply. V_{DDP} must be less than or equal to V_{DDA}/V_{DDS}.

Electrical Specifications

Values valid for over supply voltage and operating temperature ranges unless otherwise specified.

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
DC Parallel I/O and Serial Characteristics							
V_{IH}	Input High Voltage			0.7 x V_{DDP}		V_{DDP}	V
V_{IL}	Input Low Voltage			GND		0.3 x V_{DDP}	V
V_{OH}	Output High Voltage	SLEW=0 I_{OH}=-250µA		0.8 x V_{DDP}			V
		SLEW=1 I_{OH}=-1mA					
V_{OL}	Output Low Voltage	SLEW=0 I_{OL}=250µA				0.2 x V_{DDP}	V
		SLEW=1 I_{OL}=1mA					
I_{IN}	Input Current			-5		5	µA
V_{GO}	Serial Input Voltage Ground Offset	Slave Relative to Master			0		V
Z	Serial Transmission Line Impedance			70	100	120	Ω
Power Characteristics							
I_{DYN_SER}	Dynamic Current of Master Device	$V_{DDA/S}$=2.75V, M/S=1, V_{DDP}=1.8V, /STBY=1, /RES=1	5.44MHz		4		mA
			12.00MHz		7		
			15.00MHz		8		
I_{DYN_DES}	Dynamic Current of Slave Device	$V_{DDA/S}$=2.75V M/S=0 V_{DDP}=1.8V, /STBY=1, /RES=1, C_L=0pF	5.44MHz		5		mA
			12.00MHz		8		
			15.00MHz		10		
I_{BRST_M}	Burst Standby Current of Master	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, M/S=1, /STBY=1, /RST=1, No STROBE Signal, C_L=0pF			1.3		mA
I_{BRST_S}	Burst Standby Current of Slave	$V_{DDA/S}$=2.75V, V_{DDP}=1.8V, M/S=0, /STBY=1, /RST=1, No STROBE Signal, C_L=0pF			1.8		mA
I_{STBY}	Standby Current	Serializer or Deserializer $V_{DDS/A}$=V_{DDP}=3.0V, /STBY=0, /RST=1				10	µA
I_{RES}	Reset Current	Serializer or Deserializer $V_{DDS/A}$=V_{DDP}=3.0V, /RST=0				10	µA
AC Operating Characteristics							
f_{WSTRB0}	Write Strobe Frequency	CKSEL=0 STRB0		0		8	MHz
f_{WSTRB1}	Write Strobe Frequency	CKSEL=1 STRB1		0		15	MHz
f_{RSTRB}	Read Strobe Frequency			0		2	MHz
t_R, t_F	Input Edge Rates[5]					40	ns
t_{S1}	Write Mode Setup Time	DP before STRBn ↑, Figure 11		5			ns
t_{H1}	Write Mode Hold Time	DP after STRBn ↑, Figure 11		15			ns
t_{S2}	READ Mode Setup Time	R/W, CNTL before STRBn ↓ Figure 12		0			ns
t_{H2}	READ Mode Hold Time	R/W, CNTL after STRBn ↓ Figure 12		16			ns
$t_{S\text{-}STRB}$	CKSEL to STRBn Setup Time	CKSEL before active edge STRBn[4], CKSEL before SPI /CS, SPI /CS before CKSEL Figure 13, Figure 14		50			ns

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
AC Deserializer Specifications						
t_{R0}, t_{F0}	Output Edge Rates of WCLK0,WCLK1	SLEW=0, CL=5pF 20% to 80%(5)	8		17	ns
		SLEW=1, C_L=5pF 20% to 80%(5)			10	
t_{R1}, t_{F1}	Output Edge Rates of R/W, DP[17:0] CNTL[5:0]	SLEW=0, C_L=5pF 20% to 80%(5)	8		22	ns
		SLEW=1, C_L=5pF 20% to 80%(5)			17	
t_{CS}	CNTL[5:0],R/W to Falling Edge of WCLKn	M/S=0(5), C_L=5pF 50% to 50%(5) Figure 15	0	4		ns
$t_{PDV-WR0}$	DP, CNTL to WCLK0 ↑	PAR/SPI=1(5), Figure 15	50	60		ns
$t_{PDV-WR1}$	DP, CNTL to WCLK1 ↑	PAR/SPI=1(5), Figure 15	18	24		ns
t_{PDV-RD}	CNTL to WCLKn ↑	PAR/SPI=1(5), Figure 17	200	224		ns
$t_{PDV-SPI}$	Data, CNTL to SCLK ↑	PAR/SPI=0(5), Figure 16	40	60		ns
$t_{PWL-WR0}$	WCLK0 Pulse Width Low; Write Mode	M/S=0, R/W=0, PAR/SPI=1(5,7) Figure 15	50	56		ns
$t_{PWL-WR1}$	WCLK1 Pulse Width Low; Write Mode	M/S=0, R/W=0, PAR/SPI=1(5,7) Figure 15	18	20		ns
t_{PWL-RD}	Pulse Width Low of WCLK; Read Mode	M/S=0, R/W=1, PAR/SPI=1(5,7) Figure 17	200	220		ns
$t_{PWL-SPI}$	Pulse Width Low of WCLK; SPI Mode	M/S=0, R/W=0, PAR/SPI=0(5,7) Figure 16	40	56		ns
AC Data Latencies						
t_{PD-WR0}	Write Latency	WRITE Mode, CKSEL=0(8,9,10) Figure 15		147		ns
t_{PD-WR1}	Write Latency	WRITE Mode, CKSEL=1(8,9,10) Figure 15		111		ns
t_{PD-RD}	Total Read Latency	READ Mode(8,10,11) Figure 17		340	480	ns
t_{PD-RDC}	Read Control Latency	READ Mode(8,10,12) Figure 17		276		ns
t_{PD-RDD}	Read Data Latency	READ Mode(8,10,13) Figure 17		84		ns
t_{PD-SPI}	SPI Write Latency	SPI-WRITE Mode(8,10,14) Figure 16		115		ns
AC Oscillator Specifications						
f_{OSC}	Serial Operating Frequency		240	275	310	MHz
$t_{OSC-STBY}$	Oscillator Stabilization Time After Standby	V_{DDA}=V_{DDS}=2.75V /RES=1, /STBY ↑ Transition		15	30	µs
$t_{OSC-RES}$	Oscillator Stabilization Time After Reset	V_{DDA}=V_{DDS}=2.75V /STBY=1, /RES ↑ Transition		30	50	µs
AC Reset and Standby Timing						
$t_{VDD-OFF}$	Power Down Relative to /RES(15)	Figure 19	20			µs
$t_{STRB-RES}$	/RES after last STRBn ↑	M/S=1, /STBY=1, R/W=0(16) Figure 19	0			ns
$t_{STRB-STBY}$	Standby time after last strobe	M/S=1, /STBY=1(17) Figure 19	200			ns
$t_{RES-OFF}$	Master/Slave Reset Disable Time	M/S=1 /STBY=1, /RES=↓ Figure 19		15	20	µs

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{VDD-SKEW}$	Allowed Skew between V_{DDP} and $V_{DDA/S}$[18]	Figure 18	-∞		+∞	ms
$t_{VDD-RES}$	Minimum Reset Low Time After V_{DD} Stable	M/S=0, /RES=↑[19] Figure 18	20			µs
$t_{RES-STBY}$	/STBY Wait Time After /RES ↑	M/S=1 /RES=1, /STBY= ↑ Figure 18	20			µs
t_{DVALID}	/STBY to Active Edge of Strobe	M/S=0 /RES=1[20] Figure 18	30			µs

Notes:

4. Active edge of strobe is the rising edge for a write transaction and the falling edge for a read transaction.
5. Characterized, but not production tested.
6. Indirectly tested through serial clock frequency and serial data bit tests.
7. Pulse width low WCLKn measurements are measured at 30% of V_{DDP}. Measurements apply when SLEW=0 or SLEW=1.
8. Minimum times occur with maximum oscillator frequency. Maximum times occur with minimum oscillator frequency.
9. Write latency is the sum of the delay through the master serializer and slave deserializer, plus the flight time across the flex cable and I/O propagation delays.
10. Assumes propagation delay across the flex cable and through the I/Os of 20ns.
11. Total read latency t_{PD-RD} is the sum of the Read-Control Phase latency (t_{PD-RDC}) and the Read-Data Phase latency (t_{PD-RDD}). $t_{PD-RD}=t_{PD-RDC}+ t_{PD-RDD}$.
12. Read-Control latency is the sum of the delay through the master serializer and slave deserializer, plus flex cable flight times and I/O propagation delays.
13. Read Data latency is the sum of the delay through the slave serializer and master deserializer, plus flex cable flight times and I/O propagation delays.
14. SPI-Write latency is the sum of the delay through the master serializer and slave deserializer, plus the flight time across the flex cable and I/O propagation delays.
15. Timing allows the device to completely reset prior to powering down.
16. Internal reset filter allows assertion prior to completion of read or write date transfer.
17. Timing ensures that last write transaction is complete prior to going into standby.
18. $V_{DDA/S}$ must power up together. V_{DDP} may power-up relative to $V_{DDA/S}$ in any order without static power being consumed. Guaranteed by characterization.
19. /RES signal should be held low for minimum time specified after supplies go HIGH. It is recommended that /RES be held low during the power supply ramp.
20. STRBn must be held off until internal oscillator has stabilized.

Typical Performance Characteristics

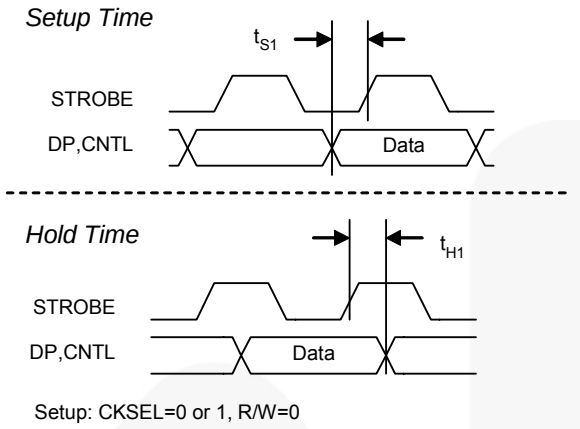


Figure 11. Master Write Setup and Hold Time

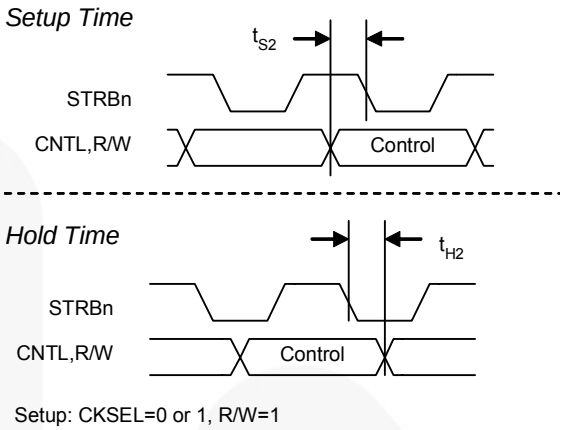


Figure 12. Master Read Setup and Hold Time

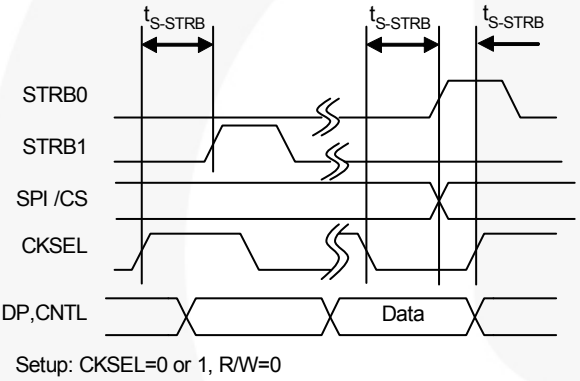


Figure 13. CKSEL Write Setup Time

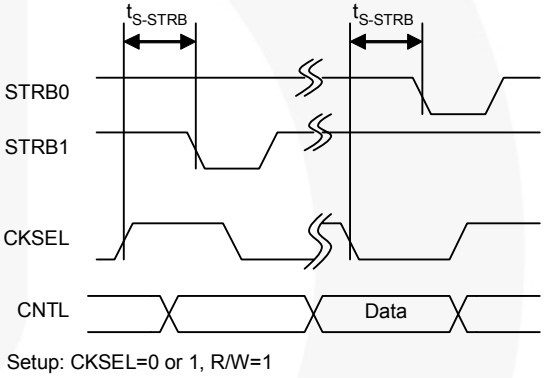


Figure 14. CKSEL Read Setup Time

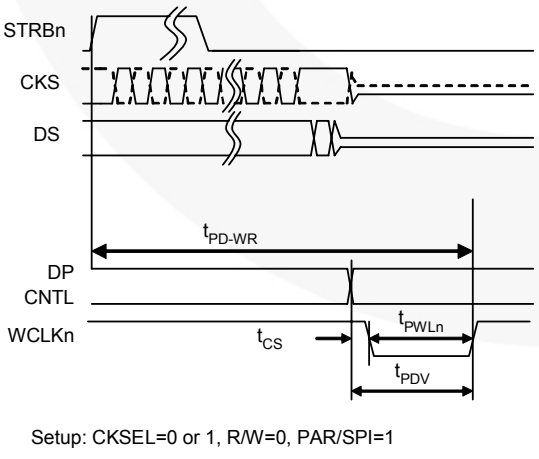


Figure 15. Slave Write Mode Timing

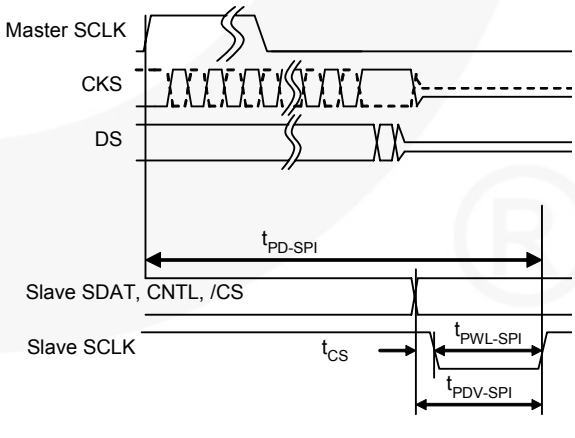


Figure 16. Slave SPI Mode Timing

Typical Performance Characteristics (Continued)

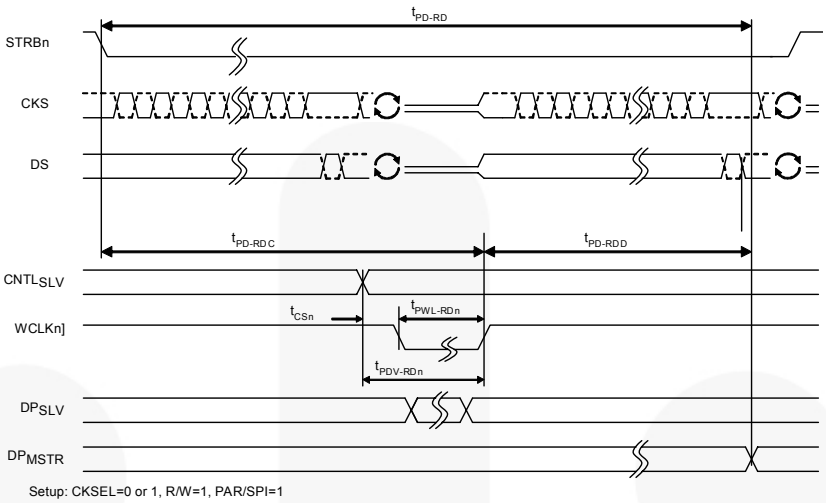


Figure 17. Slave Read Mode Timing

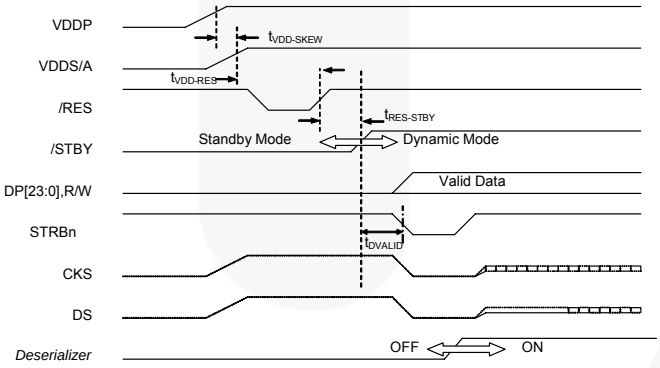


Figure 18. Power-Up Timing

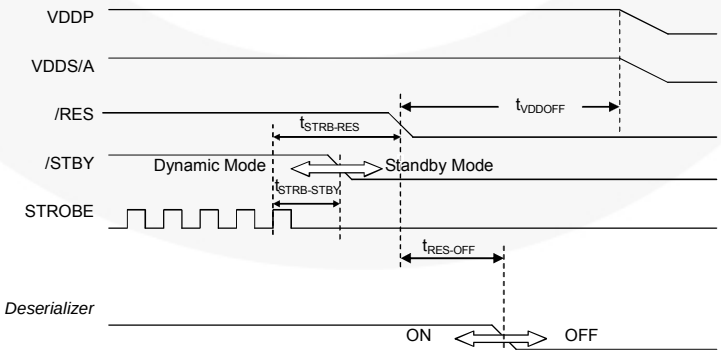
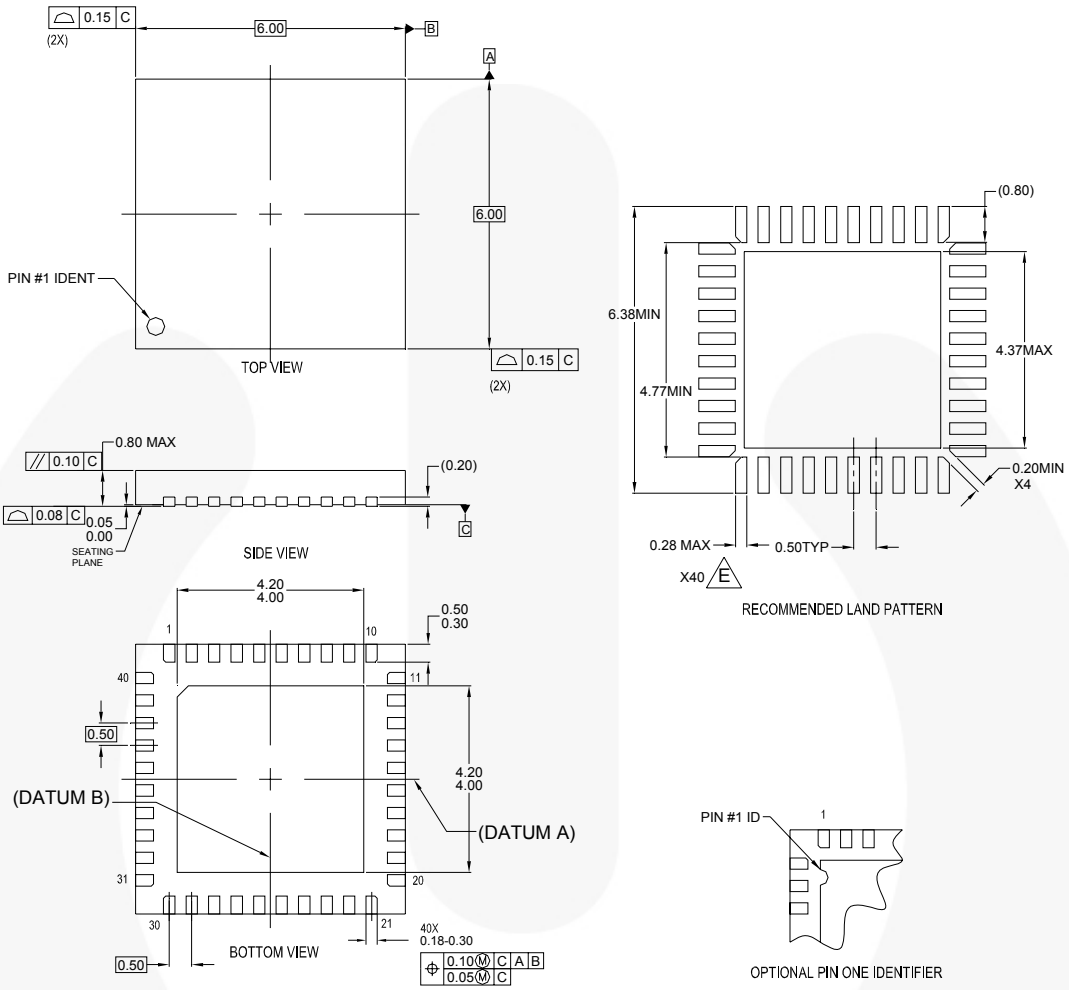


Figure 19. Power-Down Timing

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-220, VARIATION WJJD-2 WITH EXCEPTION THAT THIS IS A SAWN VERSION..

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.

D. LAND PATTERN PER IPC SM-782.

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

F. DIMENSIONS ARE NOT INCLUSIVE OF BURRS, MOLD FLASH, OR TIE BAR PROTRUSIONS.

G. DRAWING FILENAME: MKT-MLP40Arev3.

Figure 20. 40-Lead, Molded Leadless Package (MLP)

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Physical Dimensions (Continued)

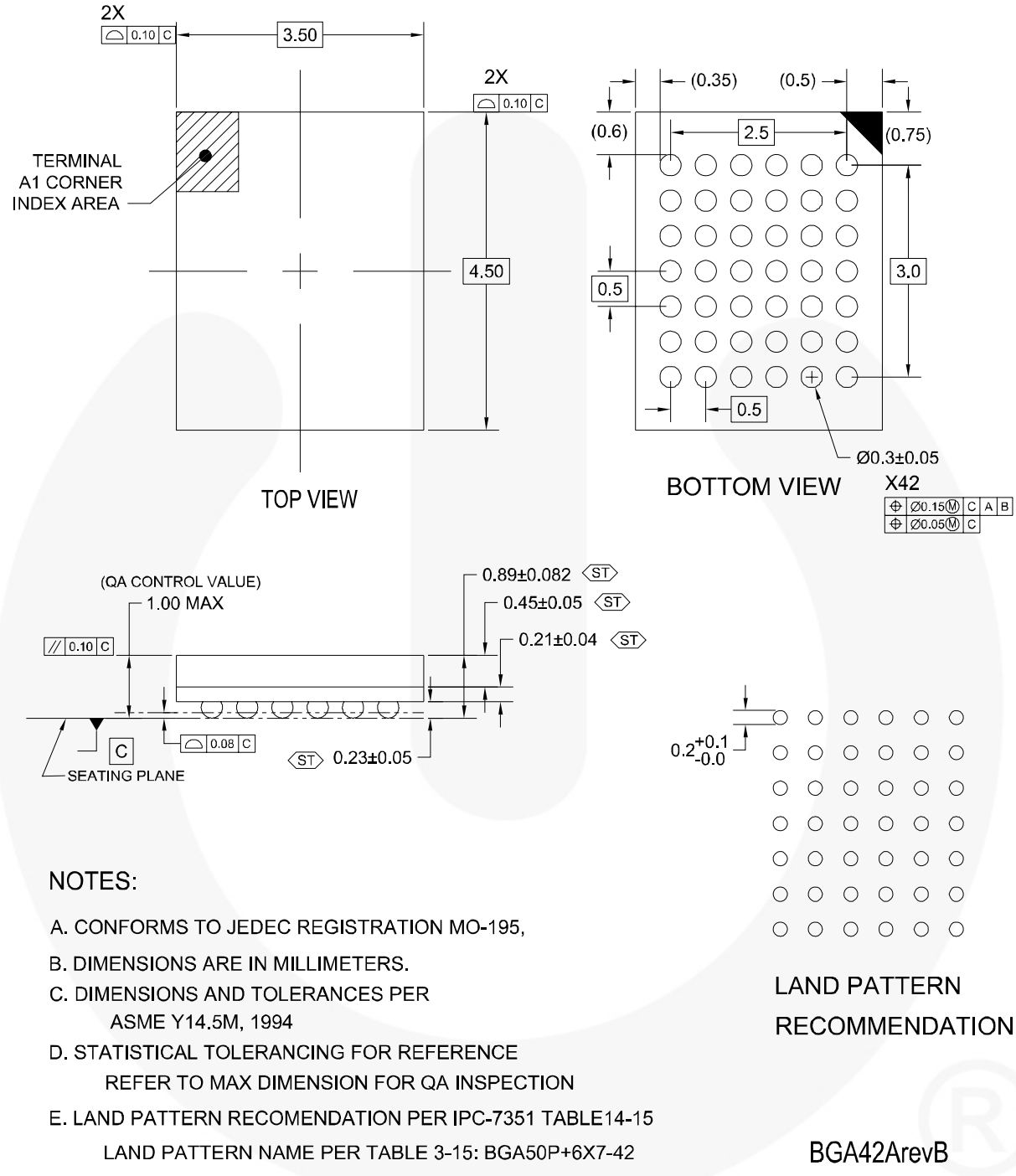

Figure 21. 42-Ball, Ball Grid Array (BGA) Package

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