

MOSFET – P-Channel, POWERTRENCH[®], Common Drain: 1.5 V, WLCSP -20 V, -3 A, 126 mΩ

FDZ1905PZ

General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two common drain P-channel MOSFETs, which enables bidirectional current flow, on ON Semiconductor's advanced 1.5 V POWERTRENCH process with state of the art "low pitch" WLCSP packaging process, the FDZ1905PZ minimizes both PCB space and $r_{S1S2(on)}$. This advanced WLCSP MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, ultra-low profile packaging, low gate charge, and low $r_{S1S2(on)}$.

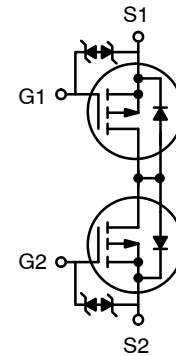
Features

- Max $r_{S1S2(on)}$ = 126 mΩ at $V_{GS} = -4.5$ V, $I_{S1S2} = -1$ A
- Max $r_{S1S2(on)}$ = 141 mΩ at $V_{GS} = -2.5$ V, $I_{S1S2} = -1$ A
- Max $r_{S1S2(on)}$ = 198 mΩ at $V_{GS} = -1.8$ V, $I_{S1S2} = -1$ A
- Max $r_{S1S2(on)}$ = 303 mΩ at $V_{GS} = -1.5$ V, $I_{S1S2} = -1$ A
- Occupies only 1.5 mm² of PCB area, less than 50% of the area of 2 x 2 BGA
- Ultra-thin package: less than 0.65 mm height when mounted to PCB
- High power and current handling capability
- HBM ESD protection level > 4 kV (Note 3)
- This Device is Pb-Free and is RoHS Compliant

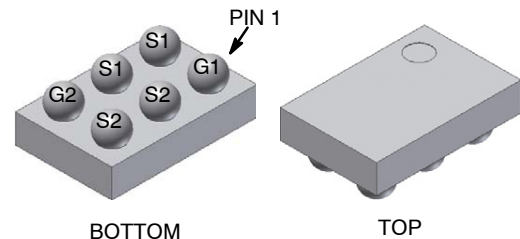


ON Semiconductor[®]

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P-Channel MOSFET

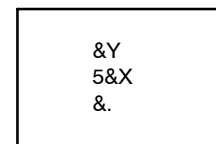


BOTTOM

TOP

**WLCSP6 1.5x1x0.6
CASE 567PW**

MARKING DIAGRAM



- | | |
|----|------------------------|
| 5 | = Specific Device Code |
| &Y | = Year Date Code |
| &X | = Weekly Date Code |
| &. | = Pin Mark |

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDZ1905PZ

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter		Rating	Unit
V_{S1S2}	Source1 to Source2 Voltage		-20	V
V_{GS}	Gate to Source Voltage		± 8	V
I_{S1S2}	Source1 to Source2 Current	- Continuous, $T_A = 25^\circ\text{C}$ (Note 1a)	-3	A
		- Pulsed	-15	
P_D	Power Dissipation (Steady State)	$T_A = 25^\circ\text{C}$ (Note 1a)	1.5	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	0.9	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	83	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	140	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

I_{S1S2}	Zero Gate Voltage Source1 to Source2 Current	$V_{S1S2} = -16\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
I_{GSS}	Gate Body Leakage Current	$V_{GS} = \pm 8\text{ V}, V_{S1S2} = 0\text{ V}$	-	-	± 10	μA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{S1S2}, I_{S1S2} = -250\text{ mA}$	-0.4	-0.7	-1.0	V
$r_{S1S2(on)}$	Static Source1 to Source2 On Resistance	$V_{GS} = -4.5\text{ V}, I_{S1S2} = -1\text{ A}$	-	99	126	$\text{m}\Omega$
		$V_{GS} = -2.5\text{ V}, I_{S1S2} = -1\text{ A}$	-	112	141	
		$V_{GS} = -1.8\text{ V}, I_{S1S2} = -1\text{ A}$	-	132	198	
		$V_{GS} = -1.5\text{ V}, I_{S1S2} = -1\text{ A}$	-	164	303	
		$V_{GS} = -4.5\text{ V}, I_{S1S2} = -1\text{ A}, T_J = 125^\circ\text{C}$	-	135	195	
g_{FS}	Forward Transconductance	$V_{S1S2} = -5\text{ V}, I_{S1S2} = -1\text{ A}$	-	8	-	S

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{S1S2} = -10\text{ V}, I_{S1S2} = -1\text{ A}$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	-	12	22	ns
t_r	Rise Time		-	36	58	ns
$t_{d(off)}$	Turn-Off Delay Time		-	143	229	ns
t_f	Fall Time		-	182	291	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FDZ1905PZ

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 83°C/W when mounted on a 1 in² pad of 2 oz copper



b. 0°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 ms, Duty cycle < 2.0%.
3. The diode connected between the gate and source serves only protection against ESD. No gate overvoltage rating is implied.

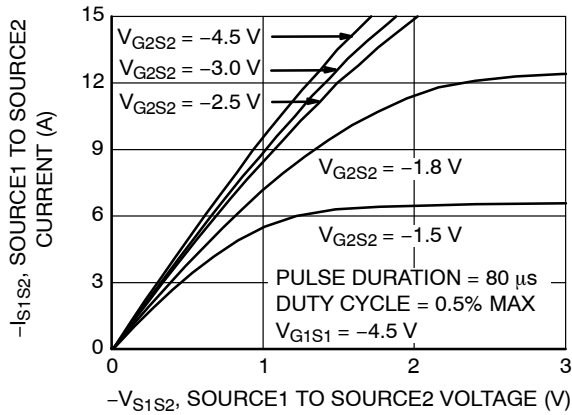
TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Figure 1. On Region Characteristics

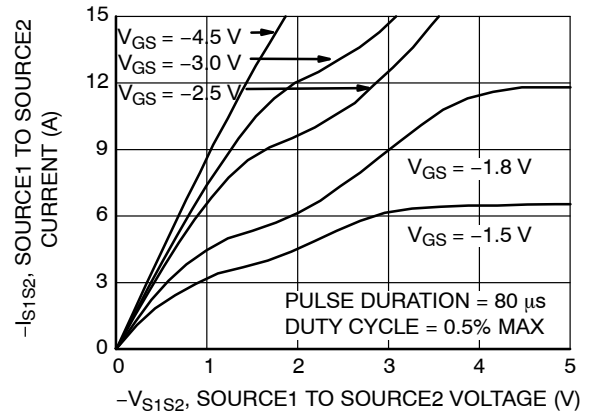


Figure 2. On Region Characteristics

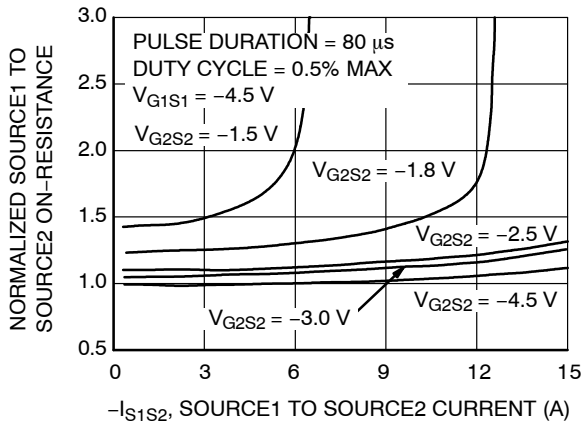


Figure 3. Normalized On-Resistance vs Drain Current and Gate Voltage

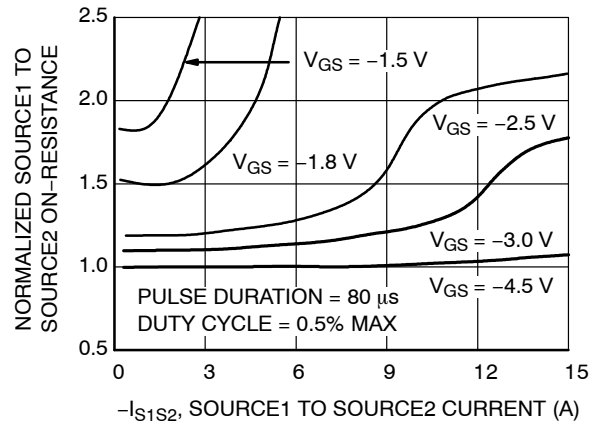


Figure 4. Normalized On-Resistance vs Drain Current and Gate Voltage

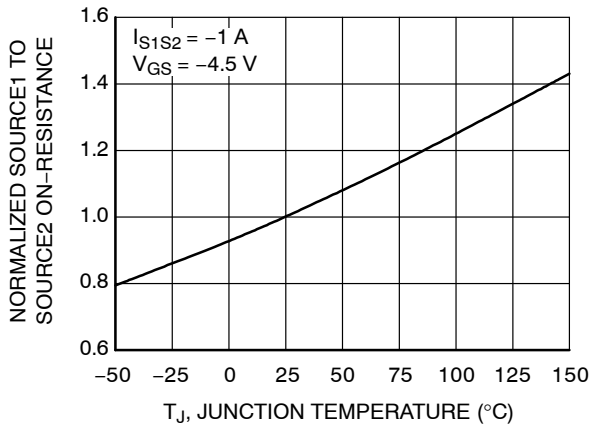


Figure 5. Normalized On-Resistance vs Junction Temperature

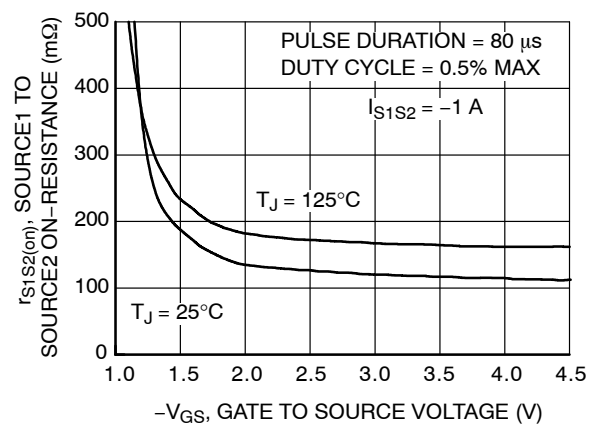


Figure 6. On-Resistance vs Gate to Source Voltage

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

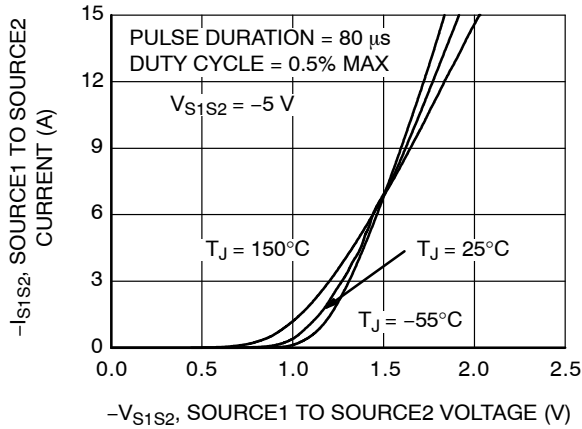


Figure 7. Transfer Characteristics

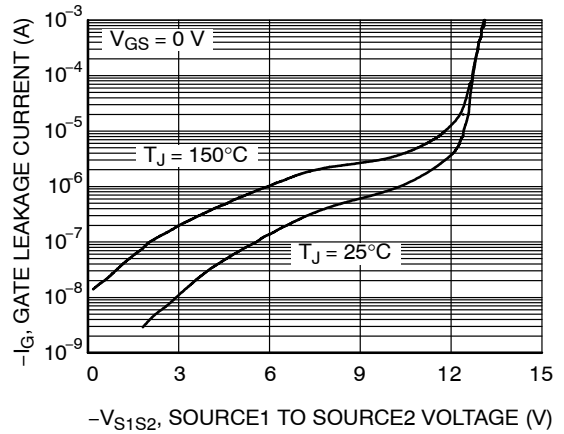


Figure 8. Gate Leakage vs Gate to Source Voltage

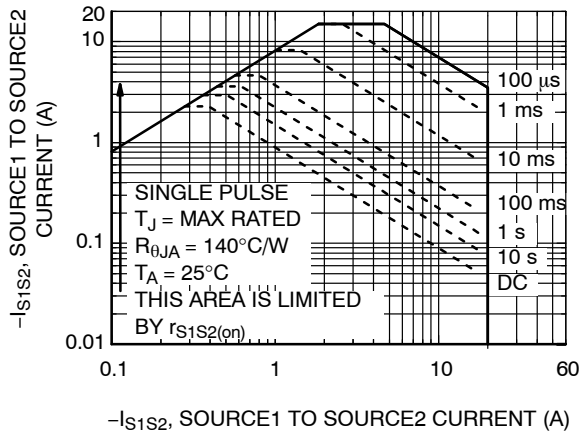


Figure 9. Forward Bias Safe Operating Area

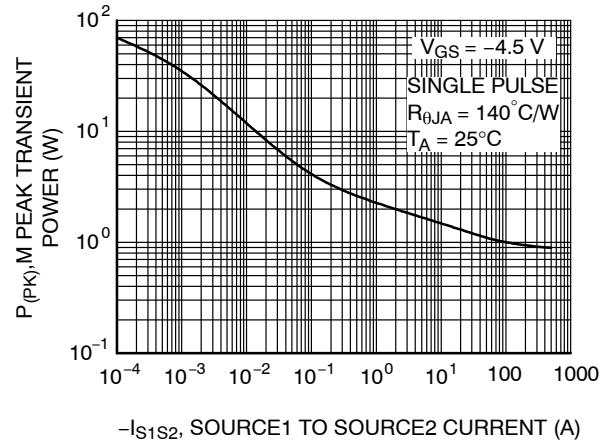


Figure 10. Single Pulse Maximum Power Dissipation

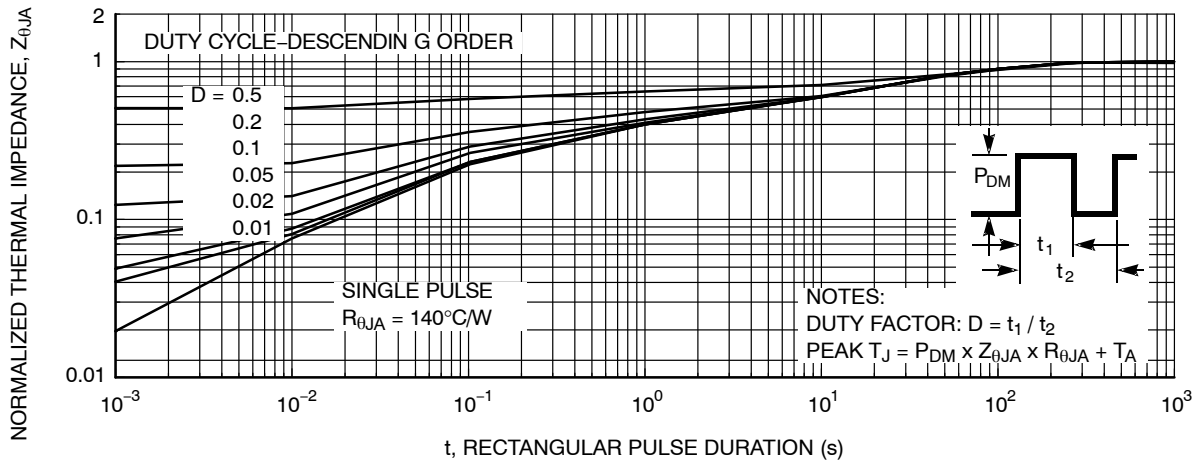


Figure 11. Transient Thermal Response Curve

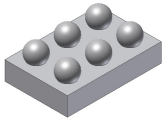
FDZ1905PZ

ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping [†]
FDZ1905PZ	5	WLCSP6 1.5x1x0.6 (Pb-Free)	7"	8 mm	5000 / Tape & Reel

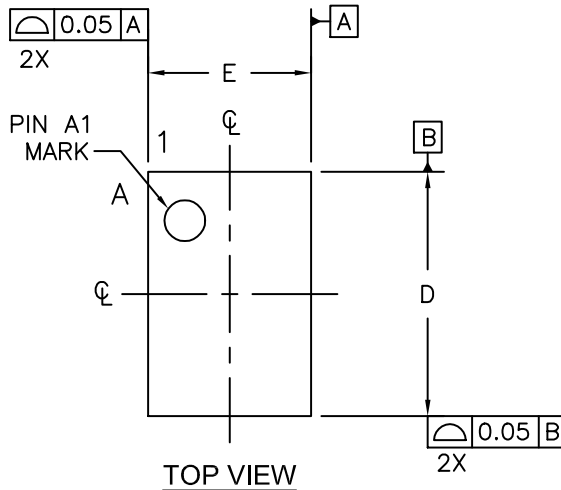
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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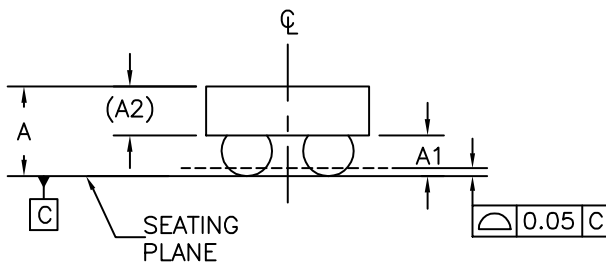


WLCSP6 1.5x1x0.6
CASE 567PW
ISSUE A

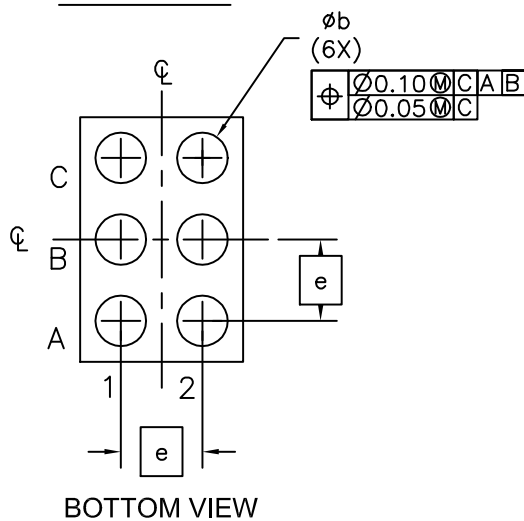
DATE 04 AUG 2021



TOP VIEW



FRONT VIEW

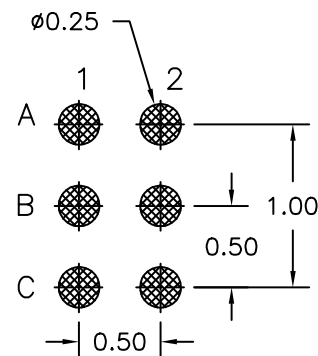


BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE
AS OF OCTOBER 2005.
C) DRAWING CONFORMS TO ASME
Y14.5M-2009

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	-	-	0.60
A1	0.22	0.25	0.28
A2	0.30 REF		
b	0.24	0.31	0.39
D	1.45	1.50	1.55
E	0.95	1.00	1.05
e	0.50 BSC		



LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DOCUMENT NUMBER:	98AON13306G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	WLCSP6 1.5x1x0.6	PAGE 1 OF 1

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