

MOSFET – N-Channel, POWER TRENCH®

100 V, 80 A, 6.4 mΩ

FDWS86068-F085

Features

- Typ $R_{DS(on)}$ = 5.2 mΩ at $V_{GS} = 10$ V, $I_D = 80$ A
- Typ $Q_{g(tot)}$ = 31 nC at $V_{GS} = 10$ V, $I_D = 80$ A
- UIS Capability
- Qualified to AEC Q101
- Wettable flanks for automatic optical inspection (AOI)
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Steering

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, Unless otherwise specified)

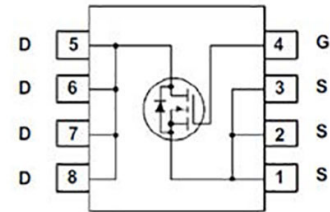
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current ($T_C = 25^\circ\text{C}$) Continuous ($V_{GS} = 10$ V) (Note 1) Pulsed	80 (see Fig. 4)	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)	36	mJ
P_D	Power Dissipation Derate above 25°C	214 1.43	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+150$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance (Junction to case)	0.7	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Maximum Thermal Resistance (Junction to Ambient) (Note 3)	50	$^\circ\text{C}/\text{W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

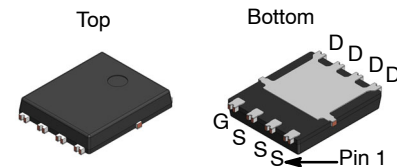
1. Current is limited by wirebond configuration.
2. Starting $T_J = 25^\circ\text{C}$, $L = 20$ μH , $I_{AS} = 60$ A, $V_{DD} = 80$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. The maximum rating presented here is based on mounting on a 1 in2 pad of 2oz copper.

V_{DSS}	I_D MAX	$R_{DS(on)}$ MAX
100 V	80 A	6.4 mΩ

ELECTRICAL CONNECTION

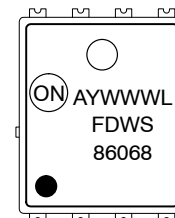


N-Channel MOSFET



DFNW8
CASE 507AU

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
WL = Assembly Lot
FDWS86068 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDWS86068-F085	DFNW8 (Power 56) (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100	–	–	V
I_{DSS}	Drain to Source Leakage Current	$V_{DS} = 100\ \text{V}$, $V_{GS} = 0\ \text{V}$ ($T_J = 25^\circ\text{C}$) ($T_J = 175^\circ\text{C}$) (Note 4)	– –	– –	1 1	μA mA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 80\ \text{A}$ ($T_J = 25^\circ\text{C}$) ($T_J = 175^\circ\text{C}$) (Note 4)	– –	5.2 11.4	6.4 14	$\text{m}\Omega$

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	2220	–	pF
C_{oss}	Output Capacitance		–	1350	–	pF
C_{rss}	Reverse Transfer Capacitance		–	19	–	pF
R_g	Gate Resistance	$V_{GS} = 0.5\ \text{V}$, $f = 1\ \text{MHz}$	–	0.3	–	Ω
$Q_{g(tot)}$	Total Gate Charge	$V_{GS} = 0$ to $10\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 80\ \text{A}$	–	31	43	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to $2\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 80\ \text{A}$	–	4	–	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 50\ \text{V}$, $I_D = 80\ \text{A}$	–	12	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	7	–	nC

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 50\ \text{V}$, $I_D = 80\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	–	30	ns
$t_{d(on)}$	Turn-On Delay Time		–	15	–	ns
t_r	Turn-On Rise Time		–	6	–	ns
$t_{d(off)}$	Turn-Off Delay Time		–	24	–	ns
t_f	Turn-Off Fall Time		–	7	–	ns
t_{off}	Turn-Off Time		–	–	48	ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$I_{SD} = 80\ \text{A}$, $V_{GS} = 0\ \text{V}$	–	0.95	1.3	V
		$I_{SD} = 40\ \text{A}$, $V_{GS} = 0\ \text{V}$	–	0.87	1.2	V
T_{rr}	Reverse Recovery Time	$I_F = 80\ \text{A}$, $dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$	–	61	80	ns
Q_{rr}	Reverse Recovery Charge		–	56	84	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production

TYPICAL CHARACTERISTICS

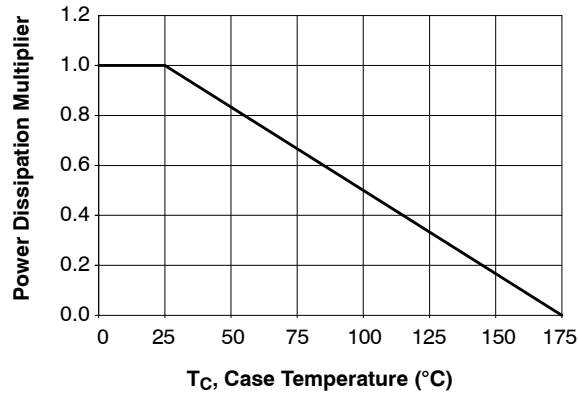
(T_J = 25°C unless otherwise noted)

Figure 1. Normalized Power Dissipation vs. Case Temperature

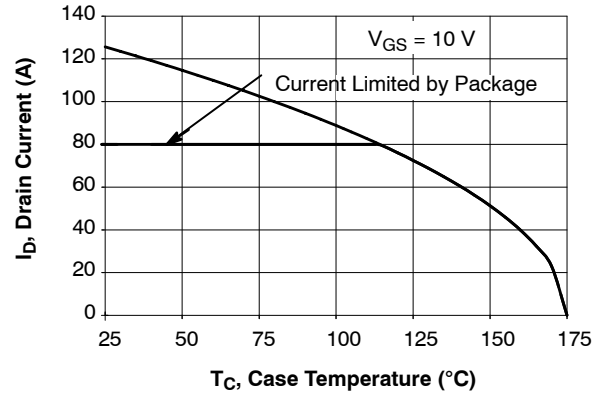


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

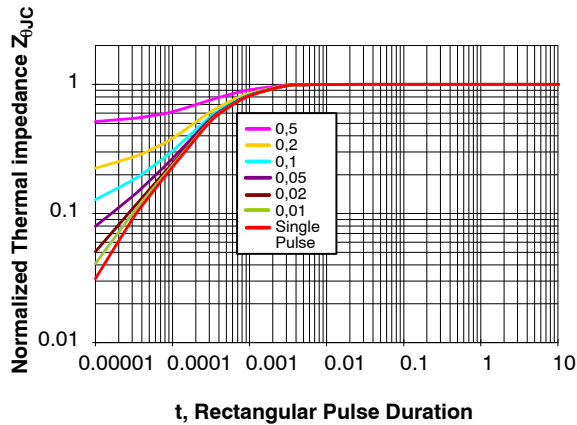


Figure 3. Normalized Maximum Transient Thermal Impedance

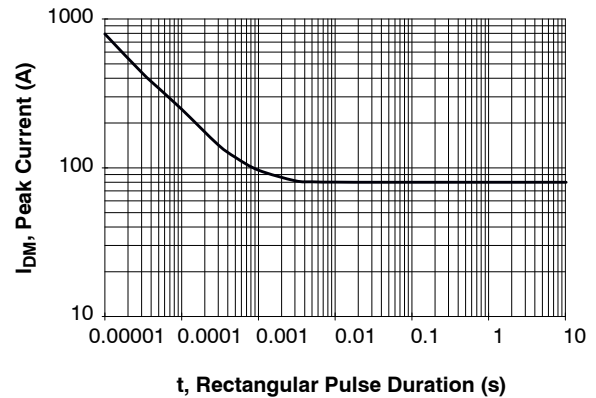


Figure 4. Peak Current Capability

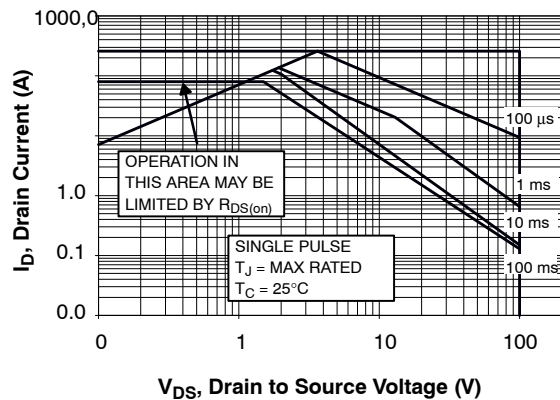


Figure 5. Forward Bias Safe Operating Area

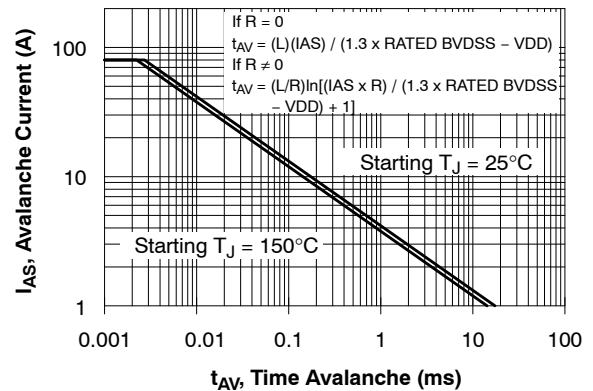
(Note: Refer to onsemi Applications Notes [AN7514](#) and [AN7515](#))

Figure 6. Unclamped Inductive Switching Capability

TYPICAL CHARACTERISTICS

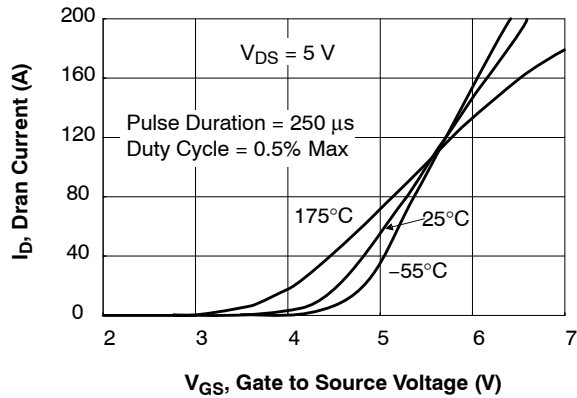
(T_J = 25°C unless otherwise noted)

Figure 7. Transfer Characteristic

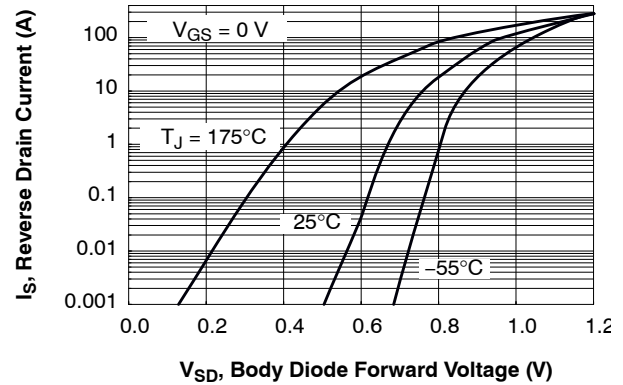


Figure 8. Forward Diode Characteristics

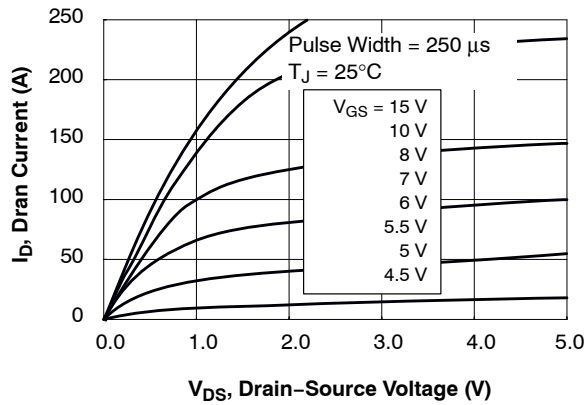


Figure 9.

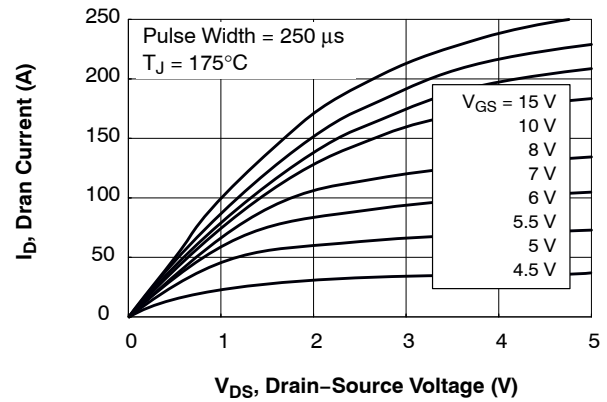
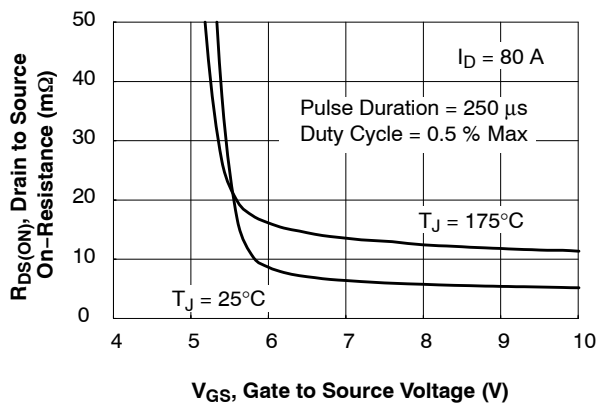
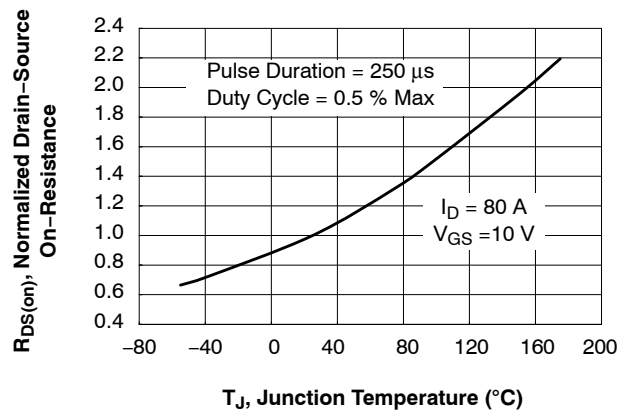


Figure 10. Peak Current Capability

Figure 11. $R_{DS(on)}$ vs. Gate VoltageFigure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

TYPICAL CHARACTERISTICS

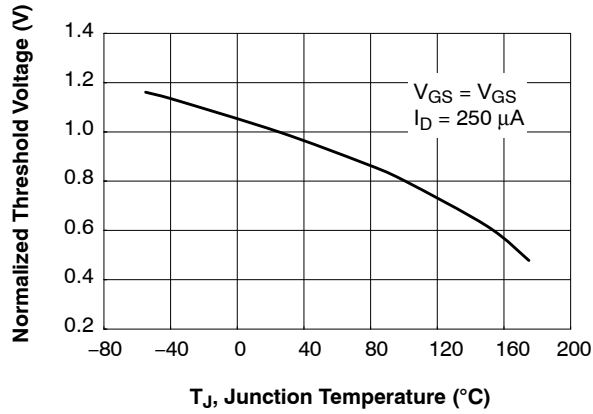
(T_J = 25°C unless otherwise noted)

Figure 13. Normalized Gate Threshold Voltage vs. Temperature

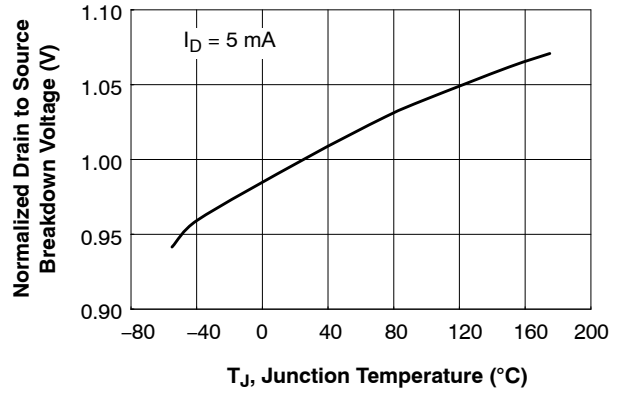


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

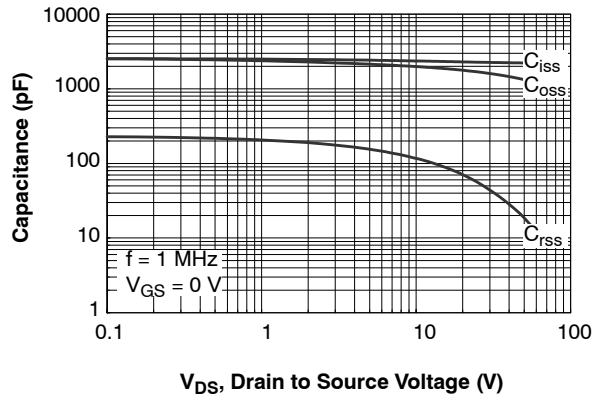


Figure 15. Capacitance vs. Drain to Source Voltage

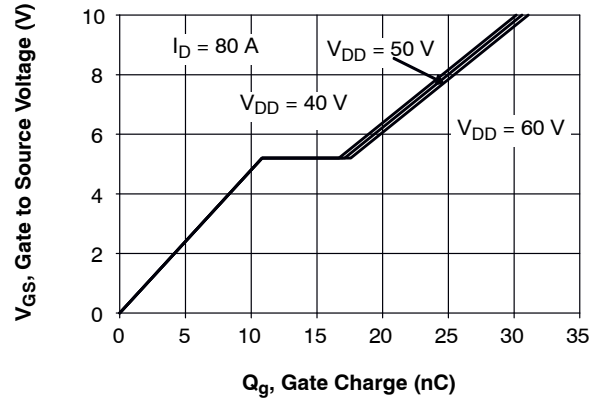
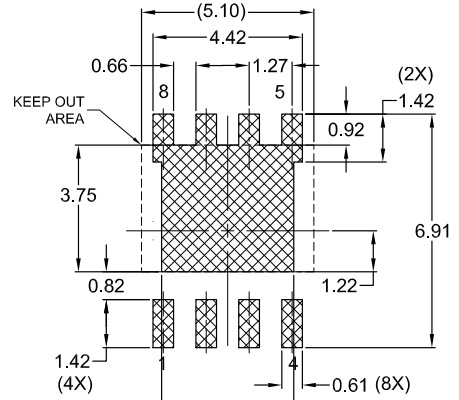
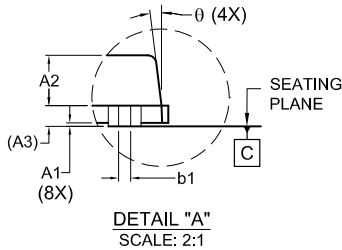
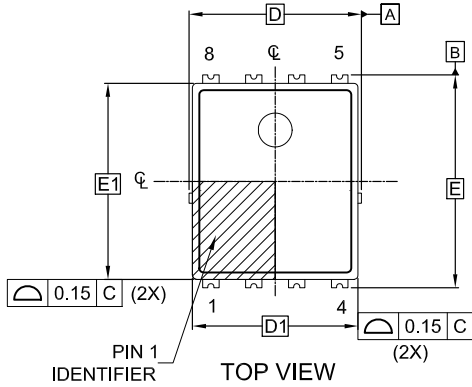


Figure 16. Gate Charge vs. Gate to Source Voltage

PACKAGE DIMENSIONS

DFNW8 5.2x6.3, 1.27P
CASE 507AU
ISSUE A

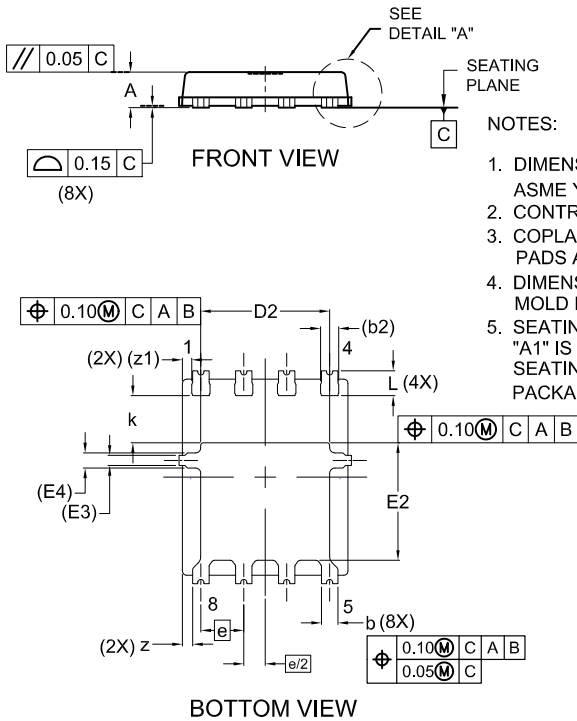


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR
PB-FREE STRATEGY AND SOLDERING DETAILS,
PLEASE DOWNLOAD THE ON SEMICONDUCTOR
SOLDERING AND MOUNTING TECHNIQUES
REFERENCE MANUAL, SOLDERM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	-	-	0.05
A2	0.65	0.75	0.85
A3	0.30 REF		
b	0.47	0.52	0.57
b1	0.13	0.18	0.23
b2	(0.54)		
D	5.00	5.10	5.20
D1	4.80	4.90	5.00
D2	3.72	3.82	3.92
E	6.20	6.30	6.40
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	0.30 REF		
E4	0.45 REF		
e	1.27 BSC		
e/2	0.635BSC		
k	1.30	1.40	1.50
L	0.64	0.74	0.84
z	0.24	0.29	0.34
z1	(0.28)		
θ	0°	---	12°

POWERTRENCH is a registered trademark of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba “**onsemi**” or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**’s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided “as-is” and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. “Typical” parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including “Typicals” must be validated for each customer application by customer’s technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800–282–9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[onsemi:](#)

[FDWS86068-F085](#)