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ON Semiconductor®

FDS8935

Dual P-Channel PowerTrench® MOSFET

-80 V, -2.1 A, 183 mΩ

Features

- Max $r_{DS(on)}$ = 183 mΩ at $V_{GS} = -10$ V, $I_D = -2.1$ A
- Max $r_{DS(on)}$ = 247 mΩ at $V_{GS} = -4.5$ V, $I_D = -1.9$ A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- RoHS Compliant

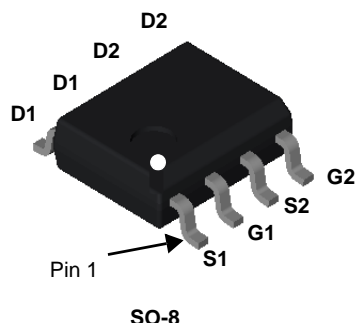


General Description

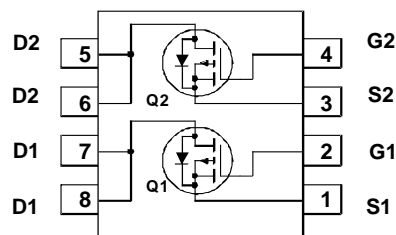
- This P-channel MOSFET is produced using ON Semiconductor's advanced PowerTrench® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Applications

- Load Switch
- Synchronous Rectifier



SO-8



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-80	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current -Continuous	-2.1	A
	-Pulsed	-10	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	37	mJ
P_D	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	3.1	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	1.6	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8935	FDS8935	SO-8	13 "	12 mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	-80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C		-61		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -64\ \text{V}$, $V_{GS} = 0\ \text{V}$			-1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = -250\ \mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, referenced to 25°C		5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\ \text{V}$, $I_D = -2.1\ \text{A}$		148	183	m Ω
		$V_{GS} = -4.5\ \text{V}$, $I_D = -1.9\ \text{A}$		176	247	
		$V_{GS} = -10\ \text{V}$, $I_D = -2.1\ \text{A}$, $T_J = 125^\circ\text{C}$		249	308	
g_{FS}	Forward Transconductance	$V_{DS} = -10\ \text{V}$, $I_D = -2.1\ \text{A}$		6.4		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -40\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$		661	879	pF
C_{oss}	Output Capacitance			47	63	pF
C_{rss}	Reverse Transfer Capacitance			24	36	pF
R_g	Gate Resistance			6		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -40\ \text{V}$, $I_D = -2.1\ \text{A}$, $V_{GS} = -10\ \text{V}$, $R_{GEN} = 6\ \Omega$		5	10	ns
t_r	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			22	36	ns
t_f	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-10\ \text{V}$	$V_{DD} = -40\ \text{V}$, $I_D = -2.1\ \text{A}$	13	19	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $-5\ \text{V}$		7	10	nC
Q_{gs}	Gate to Source Charge			1.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			2.6		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = -2.1\ \text{A}$ (Note 2)		-1.8	-1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = -1.3\ \text{A}$ (Note 2)		-0.8	-1.2	
t_{rr}	Reverse Recovery Time	$I_F = -2.1\ \text{A}$, $di/dt = 300\ \text{A}/\mu\text{s}$		19	30	ns
Q_{rr}	Reverse Recovery Charge			34	54	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a $1\ \text{in}^2$ pad 2 oz copper pad on a $1.5 \times 1.5\ \text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz copper



b) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad

2. Pulse Test: Pulse Width $< 300\ \mu\text{s}$, Duty cycle $< 2.0\%$.

3. Starting $T_J = 25^\circ\text{C}$, $L = 3.0\ \text{mH}$, $I_{AS} = -5.0\ \text{A}$, $V_{DD} = -80\ \text{V}$, $V_{GS} = -10\ \text{V}$.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

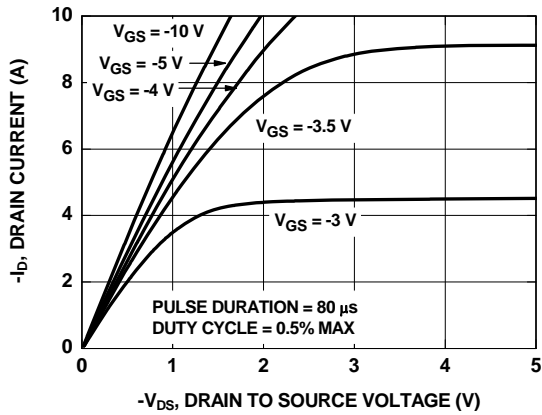


Figure 1. On-Region Characteristics

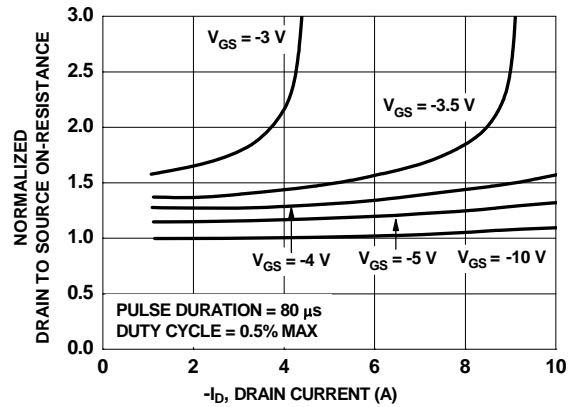


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

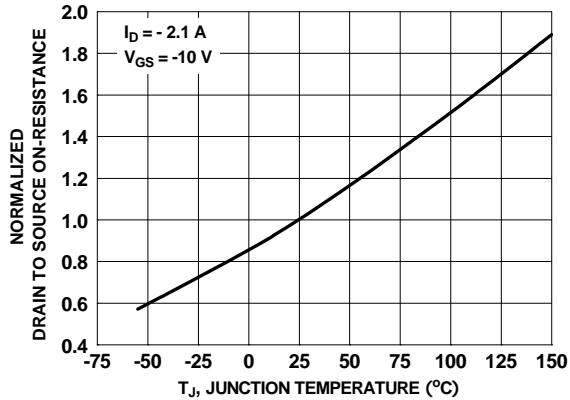


Figure 3. Normalized On-Resistance vs Junction Temperature

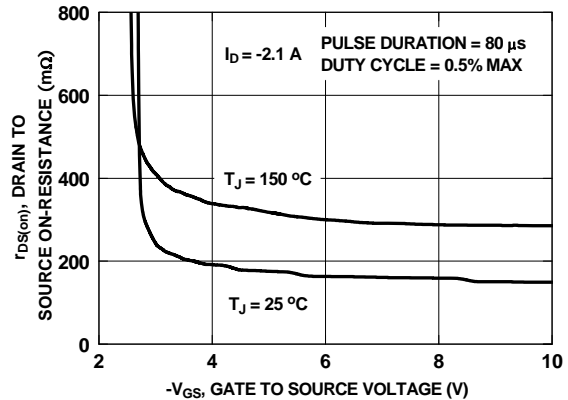


Figure 4. On-Resistance vs Gate to Source Voltage

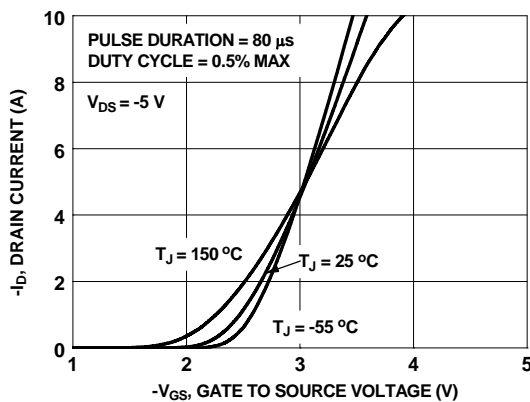


Figure 5. Transfer Characteristics

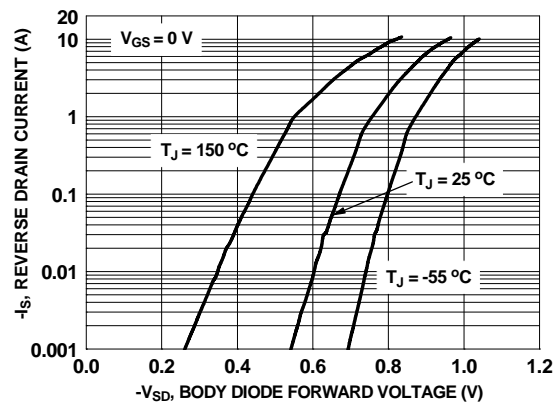


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

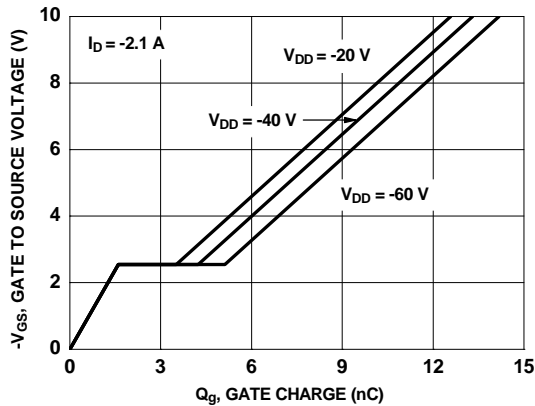


Figure 7. Gate Charge Characteristics

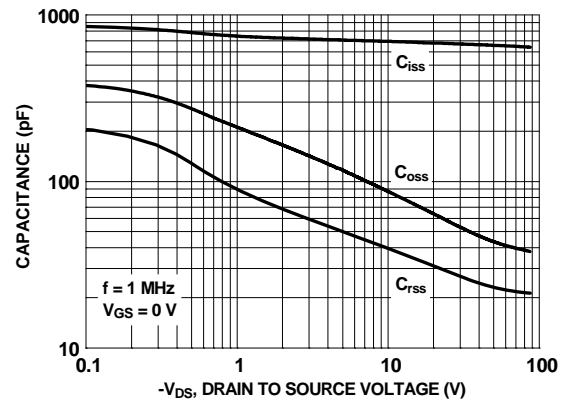


Figure 8. Capacitance vs Drain to Source Voltage

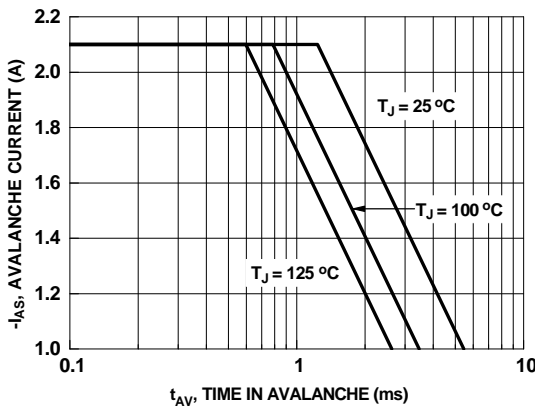


Figure 9. Unclamped Inductive Switching Capability

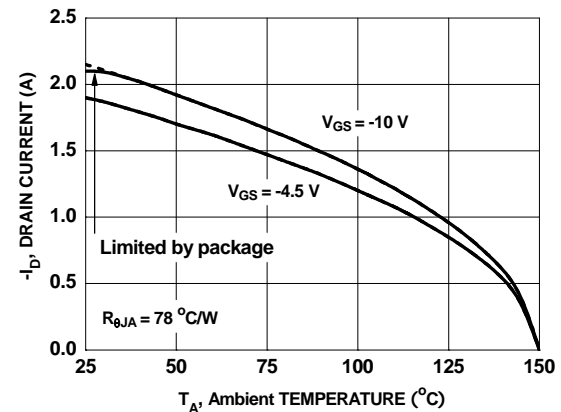


Figure 10. Maximum Continuous Drain Current vs Ambient Temperature

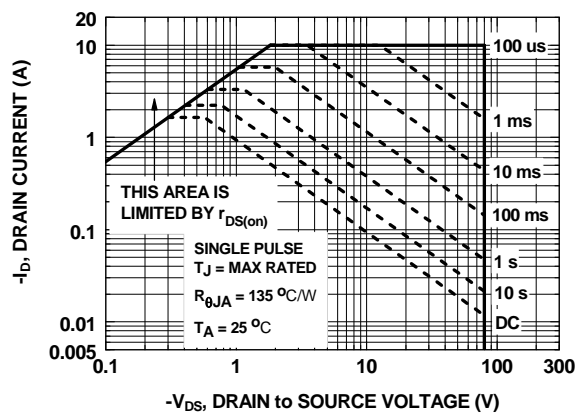


Figure 11. Forward Bias Safe Operating Area

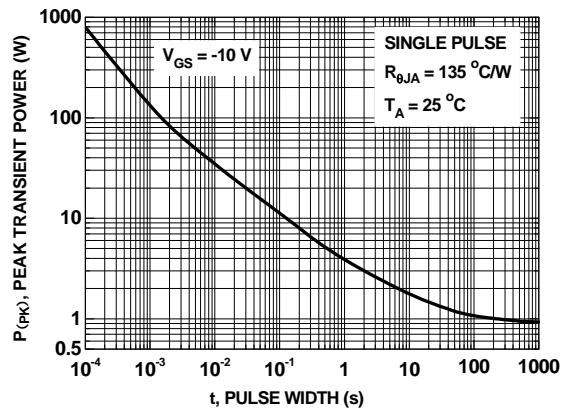
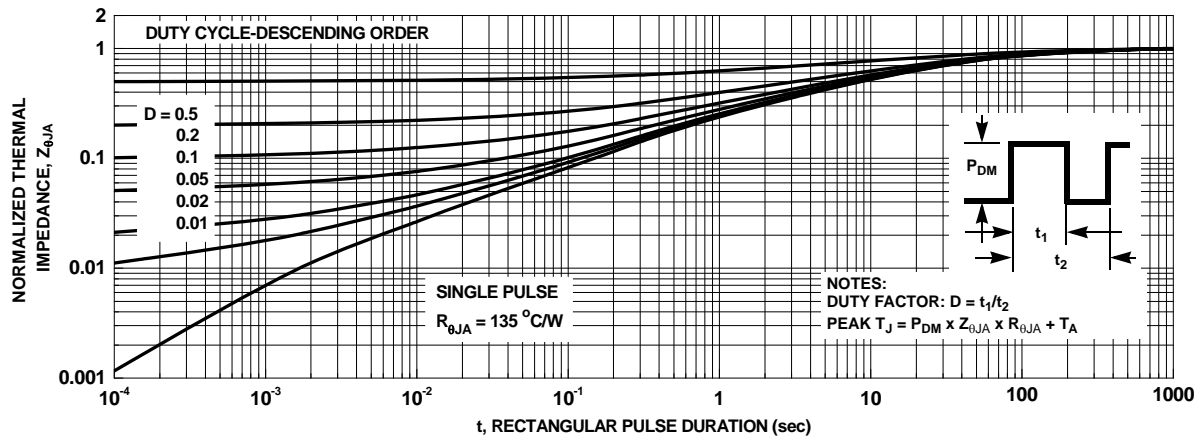


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted



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