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FDS3512

80V N-Channel PowerTrench® MOSFET

General Description

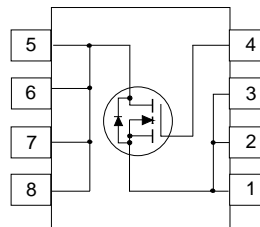
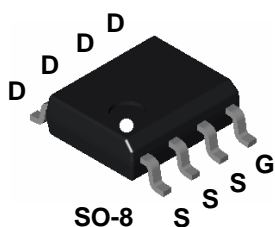
This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications.

The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

Features

- 4.0 A, 80 V $R_{DS(ON)} = 70 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 80 \text{ m}\Omega @ V_{GS} = 6 \text{ V}$
- Low gate charge (13nC Typical)
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	80	V
V_{GSS}	Gate-Source Voltage	± 20	V
I_D	Drain Current – Continuous (Note 1a)	4.0	A
	– Pulsed	30	
P_D	Power Dissipation for Single Operation (Note 1a)	2.5	W
	(Note 1b)	1.2	
	(Note 1c)	1.0	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to $+175$	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C}/\text{W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS3512	FDS3512	13"	12mm	2500 units

Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Drain-Source Avalanche Ratings (Note 2)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 40\text{ V}$, $I_D = 4.0\text{ A}$			90	mJ
I_{AR}	Maximum Drain-Source Avalanche Current				4.0	A

Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\ \mu\text{A}$	80			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		80		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$			-100	nA

On Characteristics (Note 2)

$V_{GS(th)n}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$	2	2.4	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-6		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.0\text{ A}$ $V_{GS} = 6\text{ V}$, $I_D = 3.7\text{ A}$ $V_{GS} = 10\text{ V}$, $I_D = 4.0\text{ A}$, $T_J = 125^\circ\text{C}$		50 55 91	70 80 135	m Ω
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 5\text{ V}$	20			A
G_{FS}	Forward Transconductance	$V_{GS} = 10\text{ V}$, $I_D = 4.0\text{ A}$		14		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$		634		pF
C_{oss}	Output Capacitance			58		pF
C_{rss}	Reverse Transfer Capacitance			28		pF

Switching Characteristics (Note 2)

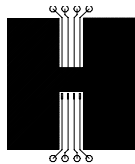
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$		7	14	ns
t_r	Turn-On Rise Time			3	6	ns
$t_{d(off)}$	Turn-Off Delay Time			24	38	ns
t_f	Turn-Off Fall Time			4	8	ns
Q_g	Total Gate Charge	$V_{DS} = 40\text{ V}$, $I_D = 4.0\text{ A}$, $V_{GS} = 10\text{ V}$		13	18	nC
Q_{gs}	Gate-Source Charge			2.4		nC
Q_{gd}	Gate-Drain Charge			2.8		nC

Drain-Source Diode Characteristics and Maximum Ratings

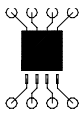
I_S	Maximum Continuous Drain-Source Diode Forward Current			2.1	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.1\text{ A}$ (Note 2)		0.8	1.2	V

Notes:

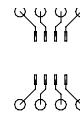
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50 $^\circ\text{C/W}$ when mounted on a 1in² pad of 2 oz copper



b) 105 $^\circ\text{C/W}$ when mounted on a 0.04 in² pad of 2 oz copper



c) 125 $^\circ\text{C/W}$ when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics

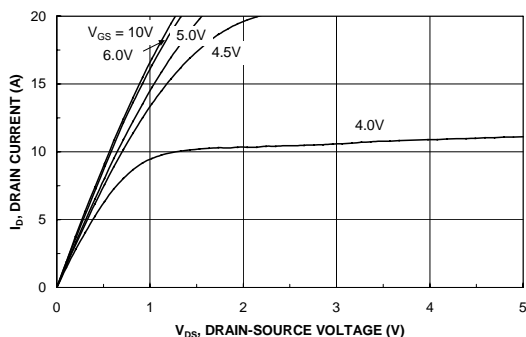


Figure 1. On-Region Characteristics.

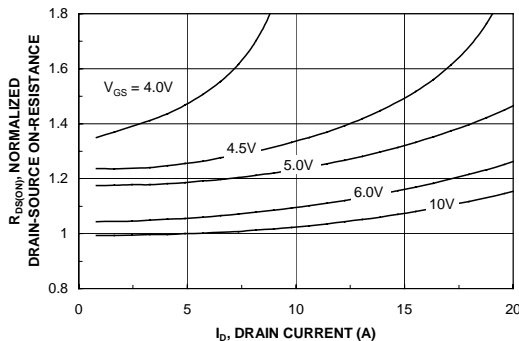


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

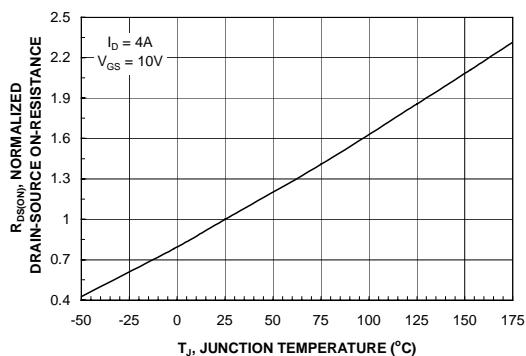


Figure 3. On-Resistance Variation with Temperature.

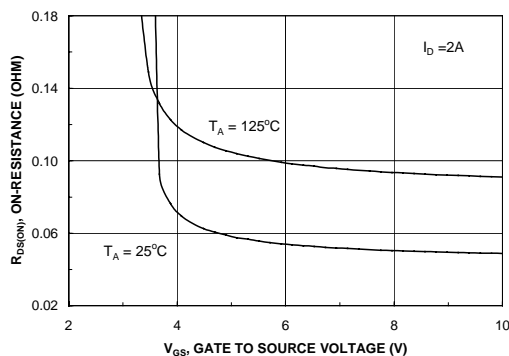


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

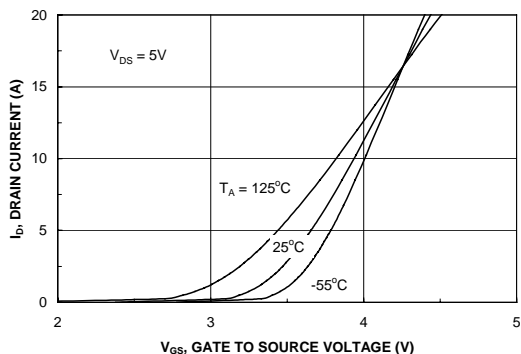


Figure 5. Transfer Characteristics.

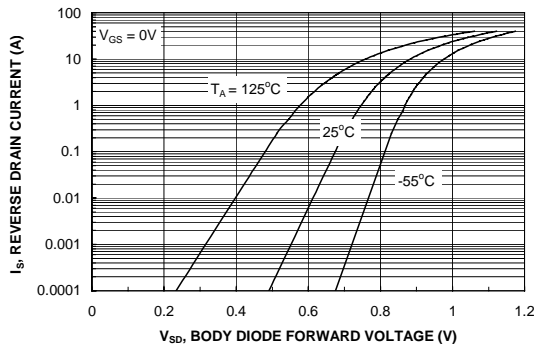


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

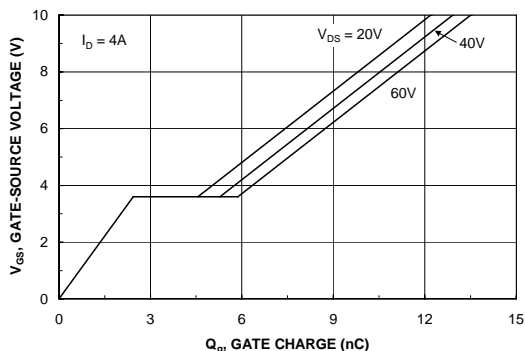


Figure 7. Gate Charge Characteristics.

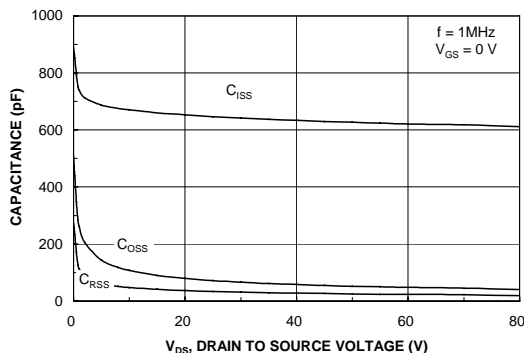


Figure 8. Capacitance Characteristics.

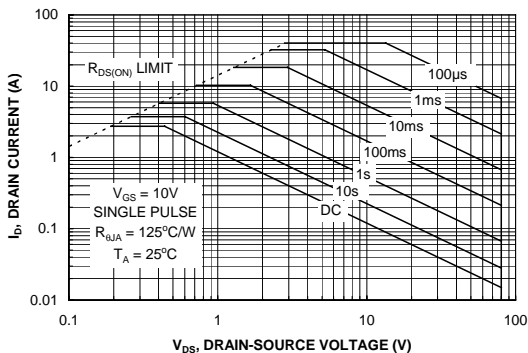


Figure 9. Maximum Safe Operating Area.

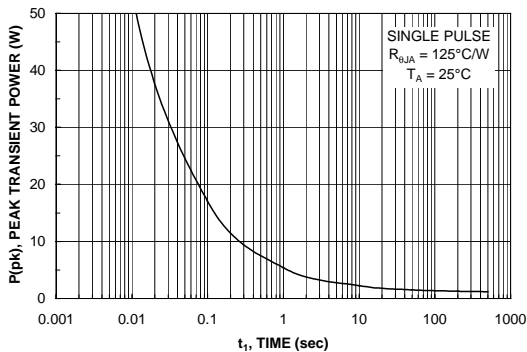


Figure 10. Single Pulse Maximum Power Dissipation.

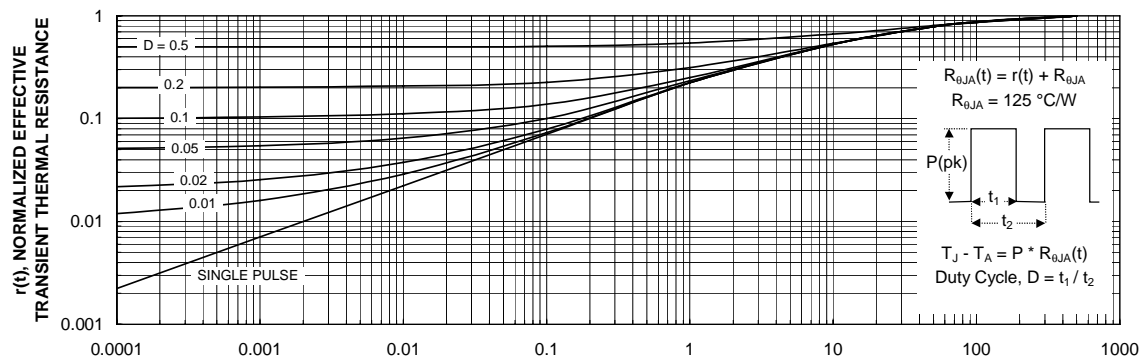


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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